

# NCS2005

## Operational Amplifier, Low Power, 8 MHz GBW, Rail-to-Rail Input-Output

The NCS2005 provides high performance in a wide range of applications. The NCS2005 offers beyond rail-to-rail input range, full rail-to-rail output swing, large capacitive load driving ability, and low distortion. The inputs can be driven by voltages that exceed both power supply rails, thus eliminating concerns over exceeding the common-mode voltage range. The rail-to-rail output swing capability provides the maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages.

Operating on supplies of 2.2 V to 32 V, the NCS2005 is excellent for a very wide range of applications in low power systems. With a supply current of 1.3 mA, the 8 MHz gain-bandwidth of this device supports applications where faster speeds are required. Placing the amplifier right at the signal source reduces board size and simplifies signal routing. The NCS2005 is available in a space-saving 5-pin SOT-23 package.

### Features

- Wide Power Supply Range: 2.2 V to 32 V
- Common Mode Voltage Range Wider than Rail-to-Rail:  
 $V_{CM} = -0.1 \text{ V to } 5.1 \text{ V @ } V_S = 5 \text{ V}$
- Wide Gain-bandwidth: 8 MHz typical
- Low Supply Current: 1.3 mA typical
- Stable with a 1 nF Capacitor Load with a Phase Margin over 25° @  
 $V_S = 10 \text{ V}$
- Available in a Space-saving 5-pin SOT23 Package
- These devices are Pb-free, Halogen free/BFR Free and are RoHS Compliant

### Typical Applications

- Active Filters
- Voltage Referenced Buffers
- Sensors and Instrumentation
- Microphone Amplifiers
- ASIC Input Drivers
- Portable Communications
- PCMCIA Cards



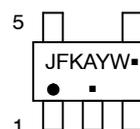
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SOT23-5  
SN SUFFIX  
CASE 483

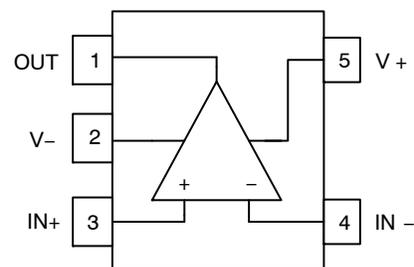
### MARKING DIAGRAM



JFK = Specific Device Code  
A = Assembly Location  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

### PIN DIAGRAM



(Top View)

### ORDERING INFORMATION

Device	Package	Shipping†
NCS2005SN1T1G	SOT-23 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

**Table 1. PIN DESCRIPTION**

Pin	Name	Type	Description
1	OUT	Output	Amplifier output
2	V-	Power	Negative power supply
3	IN+	Input	Non-inverting input of amplifier
4	IN-	Input	Inverting input of amplifier
5	V+	Power	Positive power supply

**Table 2. ABSOLUTE MAXIMUM RATINGS** (Note 1)

rating	Symbol	Value	Units
Supply Voltage Range (V+ - V-)	V <sub>S</sub>	0 to 35	V
Input Voltage Range	V <sub>CM</sub>	(V-) - 0.3 V to (V+) + 0.3 V	V
Differential Input Voltage Range	V <sub>diff</sub>	0 to 15	V
Input Pin Current	I <sub>IN</sub>	±10	mA
Output Pin Current (Note 2)	I <sub>OUT</sub>	±20	mA
Supply Current	I <sub>S</sub>	25	mA
Maximum Junction Temperature (Note 3)	T <sub>J(max)</sub>	+150	°C
Storage Temperature Range	T <sub>stg</sub>	-65 to +150	°C
ESD Capability (Note 4) Human Body Model Charged Device Model	HBM CDM	4000 400	V
Moisture Sensitivity Level (Note 5)	MSL	Level 1	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. Applies to both single supply and split supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.
3. The maximum power dissipation is a function of T<sub>J(MAX)</sub>, T<sub>JA</sub>, and T<sub>A</sub>. The maximum allowable dissipation at any ambient temperature is P<sub>d</sub> = (T<sub>J(max)</sub> - T<sub>A</sub>)/T<sub>JA</sub>. All numbers apply for packages soldered directly to a PC board.
4. This device series incorporates ESD protection and is tested by the following methods:  
ESD Human Body Model tested per JESD22-A114  
ESD Charged Device Model tested per ANSI/ESD S5.3.1-2009
5. Moisture Sensitivity Level tested per IPC/JEDEC standard: J-STD-020A

**Table 3. THERMAL CHARACTERISTICS**

Parameter	Symbol	Package	Single Layer Board	Multi Layer Board	Units
Thermal Resistance Junction-to-Ambient (Note 6)	θ <sub>JA</sub>	SOT-23-5	408 (Note 6)	355 (Note 7)	°C/W

6. Values based on a 1S standard PCB according to JEDEC51-3 with 1.0 oz copper and a 300 mm<sup>2</sup> copper area
7. Values based on a 1S2P standard PCB according to JEDEC51-7 with 1.0 oz copper and a 100 mm<sup>2</sup> copper area

**Table 4. OPERATING RANGES**

Parameter	Symbol	Min	Max	Units
Power Supply Voltage	V <sub>S</sub>	2.2	32	V
Common Mode Input Voltage	V <sub>CM</sub>	(V-) - 0.1	(V+) + 0.1	V
Ambient Temperature	T <sub>A</sub>	-40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

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**Table 5. ELECTRICAL CHARACTERISTICS AT 10 V SUPPLY** Unless otherwise noted, values are referenced to  $T_A = 25^\circ\text{C}$ ,  $V_+ = 10\text{ V}$ ,  $V_- = 0\text{ V}$ ,  $V_{CM} = V_+/2$ , and  $R_L > 1\text{ M}\Omega$  to  $V_+/2$ . **Boldface** limits apply from  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$ . (Notes 8, 9)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Units
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## SUPPLY CHARACTERISTICS

Quiescent Supply Current	No load	$I_S$		1.30	1.5	mA
					<b>1.7</b>	
Power Supply Rejection Ratio	$V_S = 2.7\text{ V to }30\text{ V}$	PSRR		113		dB
			<b>70</b>			

## INPUT CHARACTERISTICS

Input Offset Voltage		$V_{OS}$		0.2	6	mV
					<b>6</b>	
Input Offset Voltage Drift		$\Delta V/\Delta T$		1		$\mu\text{V}/^\circ\text{C}$
Input Bias Current	$V_{CM} = 0\text{ V}$	$I_{IB}$		50	200	nA
					<b>200</b>	
	$V_{CM} = 10\text{ V}$			50	200	
					<b>200</b>	
Input Offset Current	$V_{CM} = 0\text{ V}$	$I_{OS}$		2	70	nA
					<b>80</b>	
	$V_{CM} = 10\text{ V}$			2	70	
					<b>80</b>	
Input Resistance		$R_{IN}$		95		$\text{M}\Omega$
Input Capacitance		$C_{IN}$		3		pF
Common Mode Rejection Ratio	$V_{CM} = V_- \text{ to } V_+$	CMRR	73	84		dB

## OUTPUT CHARACTERISTICS

High-level output voltage	$I_L = 10\text{ mA}$	$V_{OH}$	9.65	9.80		V
Low-Level Output Voltage	$I_L = 10\text{ mA}$	$V_{OL}$		176	300	mV
Output Current Capability	Sourcing current	$I_{OUT}$		12		mA
	Sinking current			20		

## DYNAMIC PERFORMANCE

Open Loop Voltage Gain	$R_L = 10\text{ k}\Omega$	$A_{VOL}$	83	107		dB
Gain-Bandwidth Product	$R_L = 10\text{ k}\Omega$	GBWP		8.5		MHz
Gain Margin	$R_L = 10\text{ k}\Omega$	$A_M$		5.5		dB
Phase Margin	$R_L = 10\text{ k}\Omega$	$\psi_M$		65		$^\circ$
Slew Rate	$R_L = 10\text{ k}\Omega$	SR		2.8		$\text{V}/\mu\text{s}$
Total Harmonic Distortion Plus Noise	$f_{IN} = 1\text{ kHz}$ , $A_V = 2$ , $R_L = 2\text{ k}\Omega$	THD+n		0.0015		%

## NOISE PERFORMANCE

Voltage Noise Density	$f = 1\text{ kHz}$	$e_N$		45		$\text{nV}/\sqrt{\text{Hz}}$
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8. Refer to ABSOLUTE MAXIMUM RATINGS and APPLICATION INFORMATION for Safe Operating Area.

9. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at  $T_J = T_A = 25^\circ\text{C}$ .

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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**Table 6. ELECTRICAL CHARACTERISTICS AT 5 V SUPPLY** Unless otherwise noted, values are referenced to  $T_A = 25^\circ\text{C}$ ,  $V_+ = 5\text{ V}$ ,  $V_- = 0\text{ V}$ ,  $V_{CM} = V_+/2$ , and  $R_L \geq 1\text{ M}\Omega$  to  $V_+/2$ . **Boldface** limits apply from  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$ , unless otherwise noted. (Notes 10, 11)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Units
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### SUPPLY CHARACTERISTICS

Quiescent Supply Current	No load	$I_S$		1.25		mA
Power Supply Rejection Ratio	$V_S = 2.7\text{ V to }30\text{ V}$	PSRR		113		dB
			<b>70</b>			

### INPUT CHARACTERISTICS

Input Offset Voltage		$V_{OS}$		0.2	6	mV
			<b>6</b>			
Input Offset Voltage Drift		$\Delta V/\Delta T$		1		$\mu\text{V}/^\circ\text{C}$
Input Bias Current	$V_{CM} = 0\text{ V}$	$I_{IB}$		55		nA
	$V_{CM} = 5\text{ V}$			55		
Input Offset Current	$V_{CM} = 0\text{ V}$	$I_{OS}$		2		nA
	$V_{CM} = 5\text{ V}$			2		
Input Resistance		$R_{IN}$		45		$\text{M}\Omega$
Input Capacitance		$C_{IN}$		3		pF
Common Mode Rejection Ratio	$V_{CM} = V_- \text{ to } V_+$	CMRR	68	90		dB

### OUTPUT CHARACTERISTICS

High-level Output Voltage	$I_L = 5\text{ mA}$	$V_{OH}$	4.75	4.83		V
Low-level Output Voltage	$I_L = 5\text{ mA}$	$V_{OL}$		130	200	mV
Output Current Capability	Sourcing current	$I_{OUT}$		12		mA
	Sinking current			20		

### DYNAMIC PERFORMANCE

Open Loop Voltage Gain	$R_L = 10\text{ k}\Omega$	$A_{VOL}$	83	100		dB
Gain-Bandwidth Product	$R_L = 10\text{ k}\Omega$	GBWP		8.5		MHz
Gain Margin	$R_L = 10\text{ k}\Omega$	$A_M$		5.5		dB
Phase Margin	$R_L = 10\text{ k}\Omega$	$\psi_M$		65		$^\circ$
Slew Rate	$R_L = 10\text{ k}\Omega$	SR		2.7		$\text{V}/\mu\text{s}$
Total Harmonic Distortion Plus Noise	$f_{IN} = 1\text{ kHz}$ , $A_V = 2$ , $R_L = 2\text{ k}\Omega$	THD+n		0.002		%

### NOISE PERFORMANCE

Voltage Noise Density	$f = 1\text{ kHz}$	$e_N$		45		$\text{nV}/\sqrt{\text{Hz}}$
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10. Refer to ABSOLUTE MAXIMUM RATINGS and APPLICATION INFORMATION for Safe Operating Area.

11. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at  $T_J = T_A = 25^\circ\text{C}$ .

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**Table 7. ELECTRICAL CHARACTERISTICS AT 2.7 V SUPPLY** Unless otherwise noted, values are referenced to  $T_A = 25^\circ\text{C}$ ,  $V_+ = 2.7\text{ V}$ ,  $V_- = 0\text{ V}$ ,  $V_{CM} = V_+/2$ , and  $R_L \geq 1\text{ M}\Omega$  to  $V_+/2$ . **Boldface** limits apply from  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$ , unless otherwise noted. (Notes 12, 13)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Units
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### SUPPLY CHARACTERISTICS

Quiescent Supply Current	No load	$I_S$		1.25		mA
Power Supply Rejection Ratio	$V_S = 2.7\text{ V to }30\text{ V}$	PSRR	<b>70</b>	113		dB

### INPUT CHARACTERISTICS

Input Offset Voltage		$V_{OS}$		0.2	<b>6</b>	mV
					<b>6</b>	
Input Offset Voltage Drift		$\Delta V/\Delta T$		1		$\mu\text{V}/^\circ\text{C}$
Input Bias Current	$V_{CM} = 0\text{ V}$	$I_{IB}$		45		nA
	$V_{CM} = 2.7\text{ V}$			45		
Input Offset Current	$V_{CM} = 0\text{ V}$	$I_{OS}$		2		nA
	$V_{CM} = 2.7\text{ V}$			2		
Input Resistance		$R_{IN}$		90		$\text{M}\Omega$
Input Capacitance		$C_{IN}$		3		pF
Common Mode Rejection Ratio	$V_{CM} = V_- \text{ to } V_+$	CMRR	58	96		dB

### OUTPUT CHARACTERISTICS

High-Level Output Voltage	$I_L = 2.7\text{ mA}$	$V_{OH}$	2.50	2.60		V
Low-Level Output Voltage	$I_L = 2.7\text{ mA}$	$V_{OL}$		100	130	mV
Output Current Capability	Sourcing current	$I_{OUT}$		12		mA
	Sinking current			20		

### DYNAMIC PERFORMANCE

Open Loop Voltage Gain	$R_L = 10\text{ k}\Omega$	$A_{VOL}$	73	114		dB
Gain-Bandwidth Product	$R_L = 10\text{ k}\Omega$	GBWP		8.5		MHz
Gain Margin	$R_L = 10\text{ k}\Omega$	$A_M$		6		dB
Phase Margin	$R_L = 10\text{ k}\Omega$	$\psi_M$		60		$^\circ$
Slew Rate	$R_L = 10\text{ k}\Omega$	SR		2.6		$\text{V}/\mu\text{s}$
Total Harmonic Distortion Plus Noise	$f_{IN} = 1\text{ kHz}$ , $A_V = 2$ , $R_L = 2\text{ k}\Omega$	THD+n		0.05		%

### NOISE PERFORMANCE

Voltage Noise Density	$f = 1\text{ kHz}$	$e_N$		45		$\text{nV}/\sqrt{\text{Hz}}$
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12. Refer to ABSOLUTE MAXIMUM RATINGS and APPLICATION INFORMATION for Safe Operating Area.

13. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at  $T_J = T_A = 25^\circ\text{C}$ .

TYPICAL CHARACTERISTICS

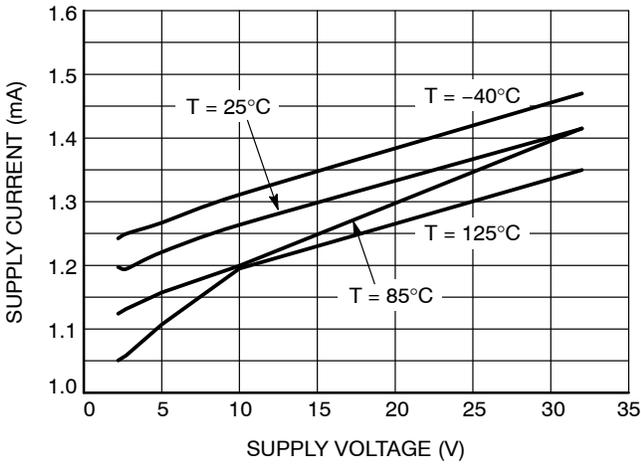


Figure 1. Quiescent Current Per Channel vs. Supply Voltage

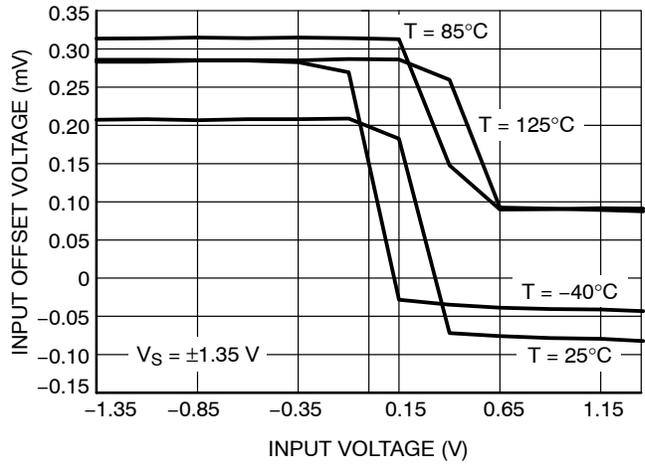


Figure 2. Input Offset Voltage vs. Common Mode Input Voltage

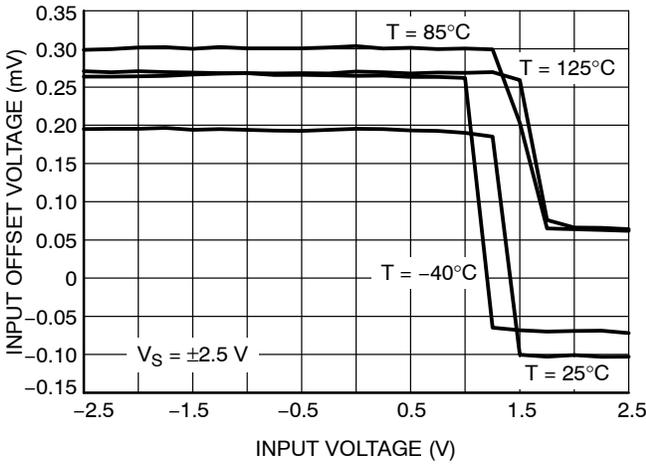


Figure 3. Input Offset Voltage vs. Common Mode Input Voltage

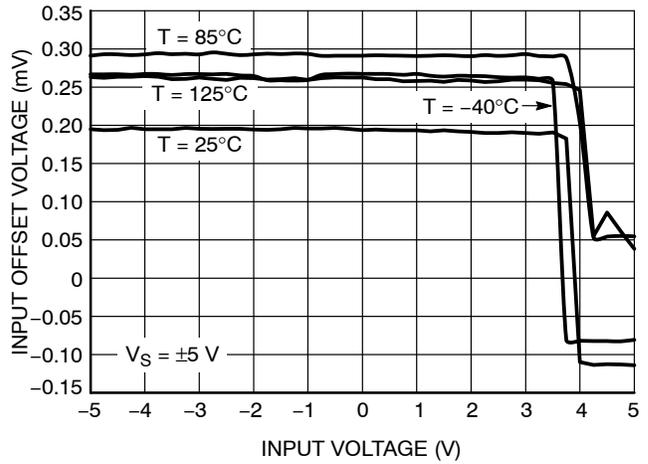


Figure 4. Input Offset Voltage vs. Common Mode Voltage

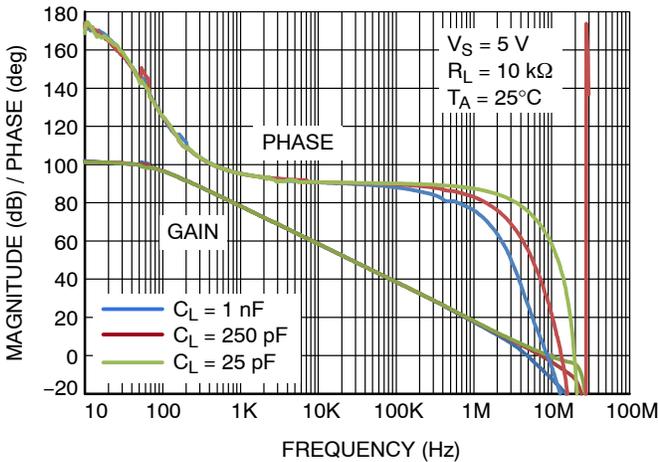


Figure 5. Gain and Phase vs. Frequency

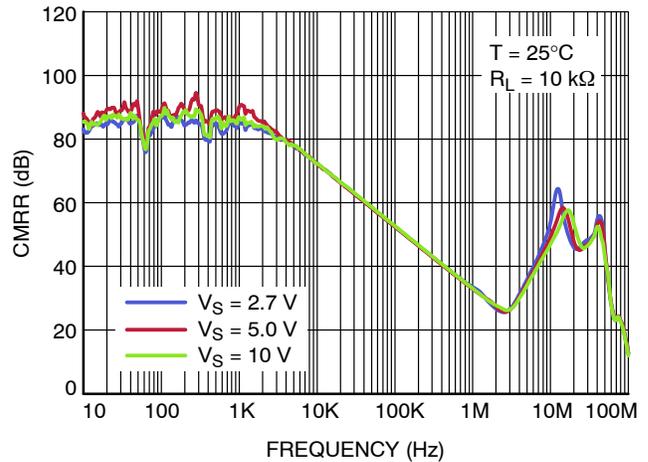


Figure 6. CMRR vs. Frequency

TYPICAL CHARACTERISTICS

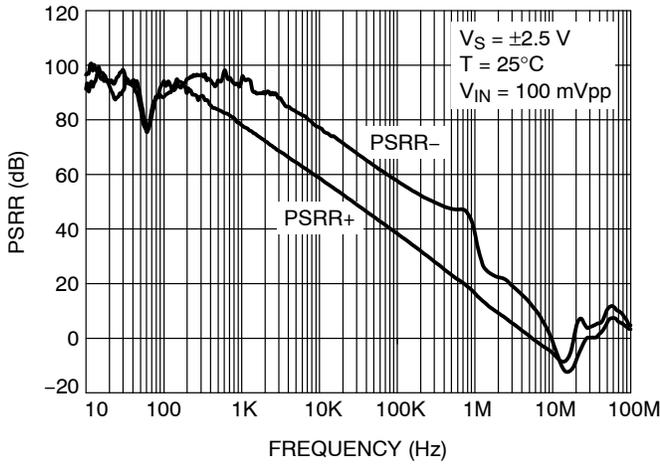


Figure 7. PSRR vs. Frequency

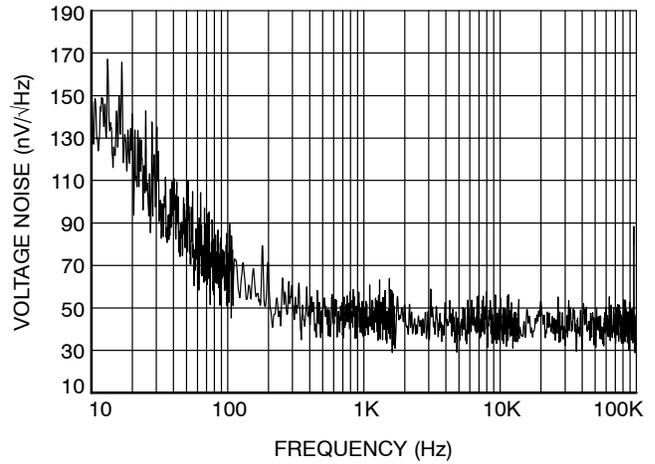


Figure 8. Input Voltage Noise vs. Frequency

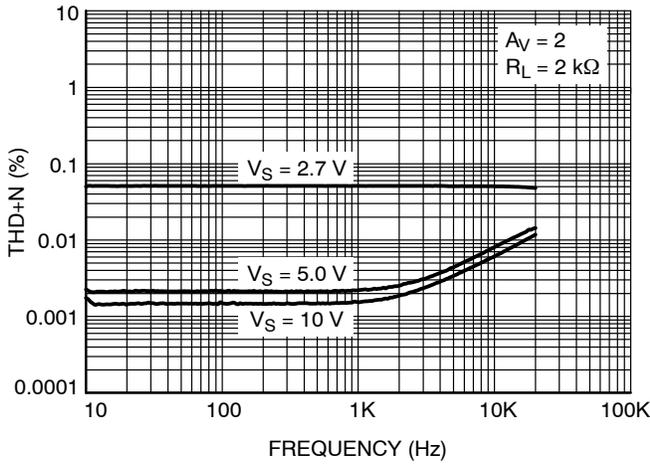


Figure 9. THD+N vs. Frequency

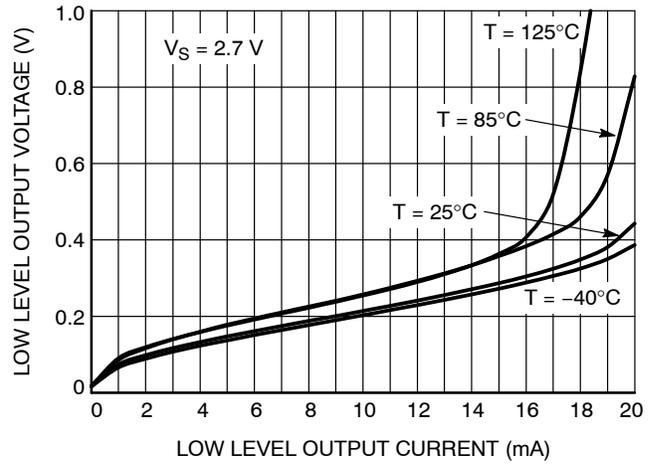


Figure 10. Low Level Output Voltage vs. Output Current @  $V_S = 2.7 V$

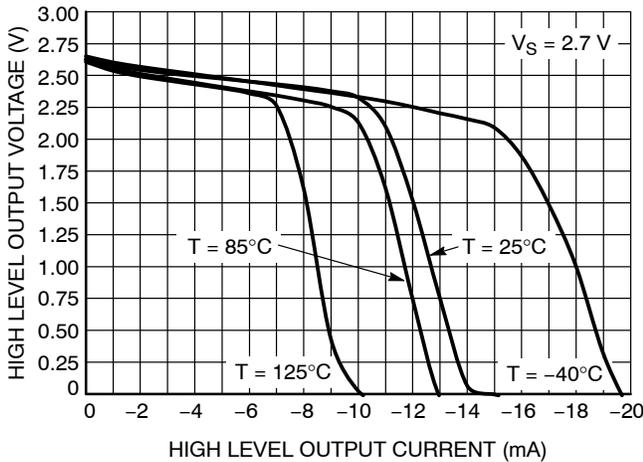


Figure 11. High Level Output Voltage vs. Output Current @  $V_S = 2.7 V$

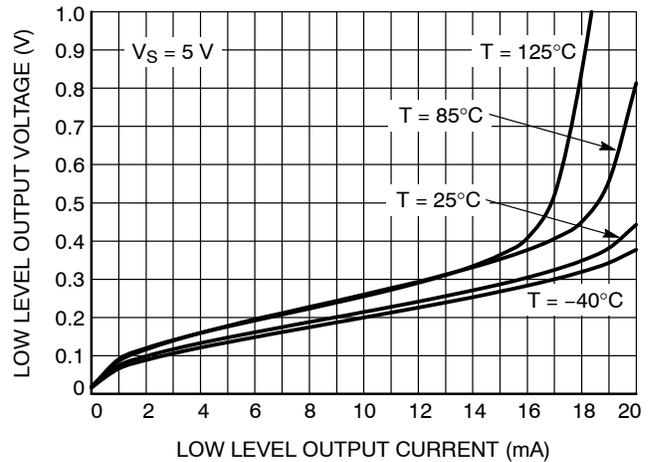


Figure 12. Low Level Output Voltage vs. Output Current @  $V_S = 5 V$

TYPICAL CHARACTERISTICS

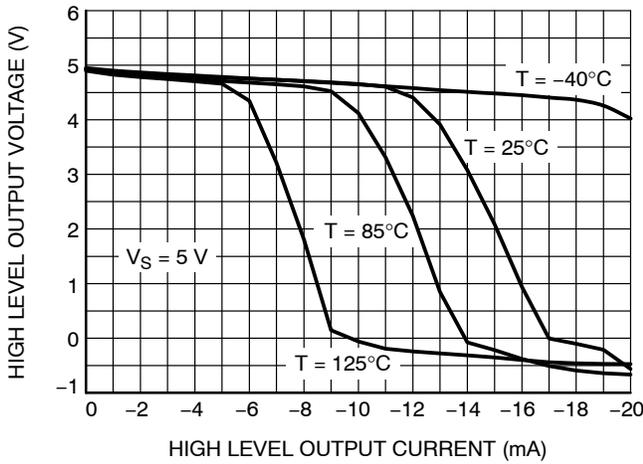


Figure 13. Low Level Output Voltage vs. Output Current

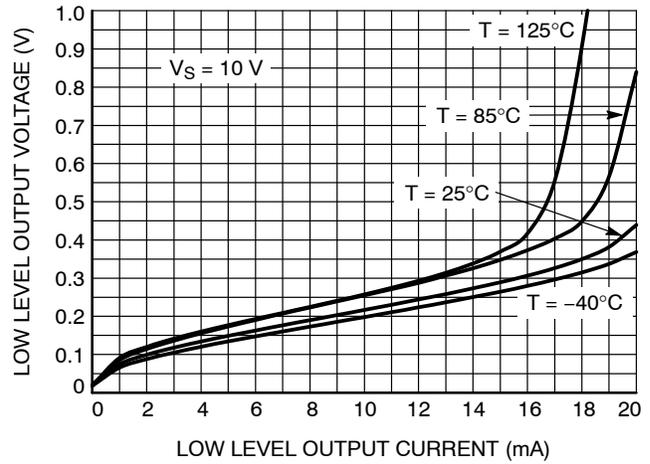


Figure 14. High Level Output Voltage vs. Output Current

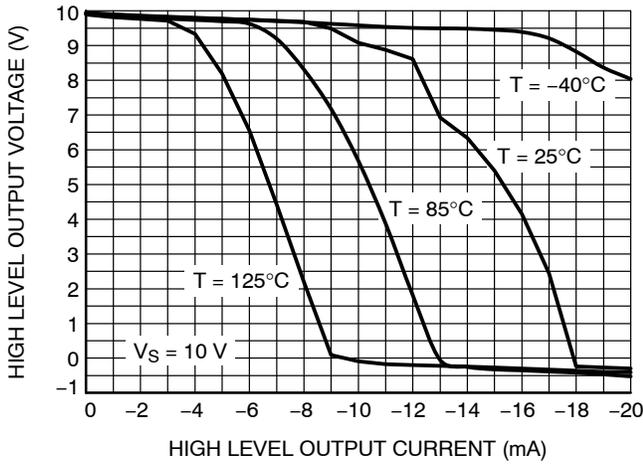


Figure 15. Low Level Output Voltage vs. Output Current

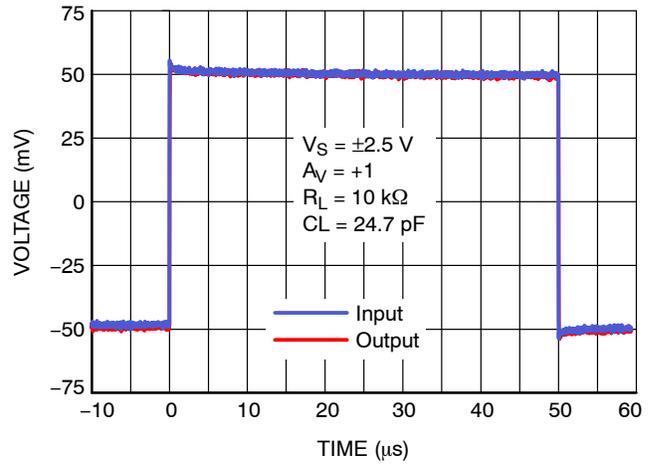


Figure 16. Non-inverting Small Signal Transient Response

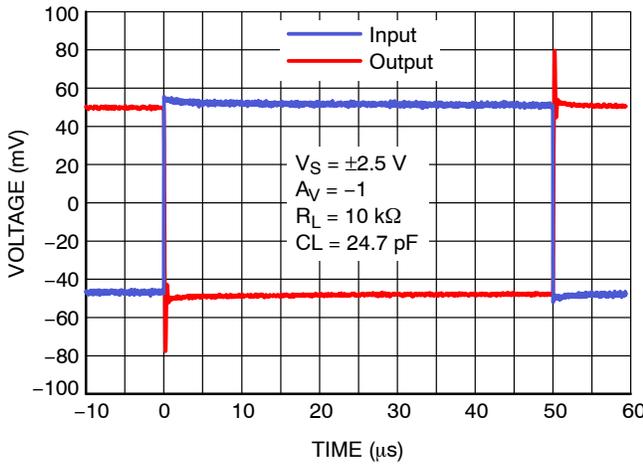


Figure 17. Inverting Small Signal Transient Response

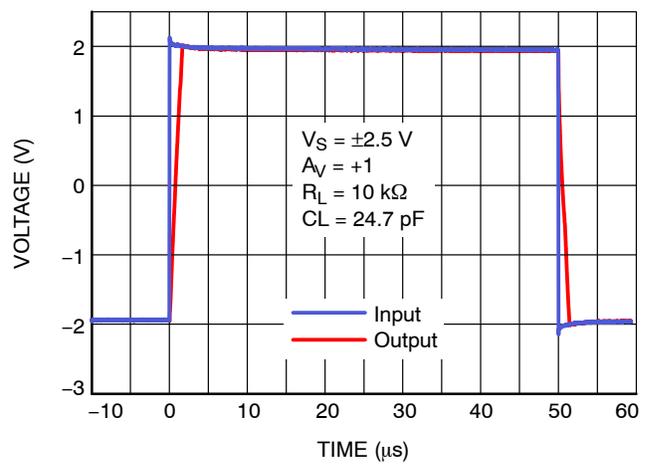


Figure 18. Non-Inverting Large Signal Transient Response

TYPICAL CHARACTERISTICS

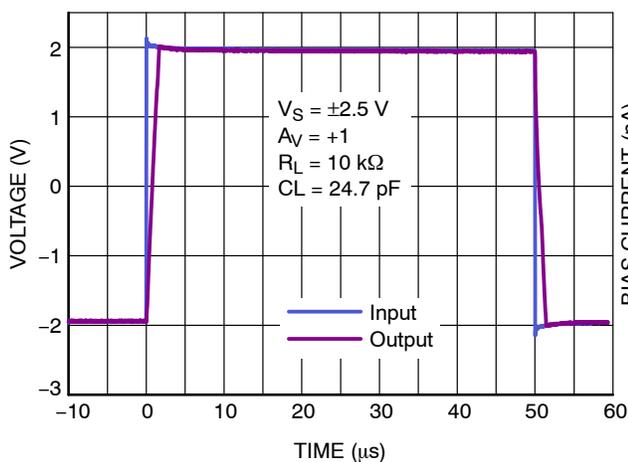


Figure 19. Inverting Large Signal Transient Response

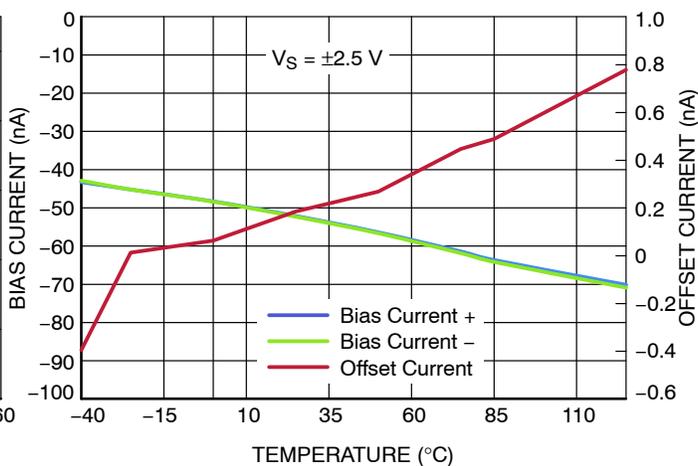


Figure 20. Input Bias and Offset Current vs. Temperature

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

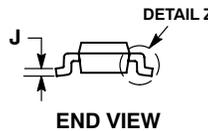
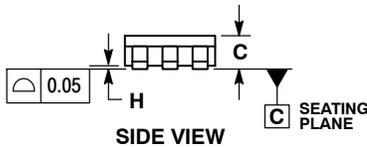
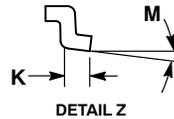
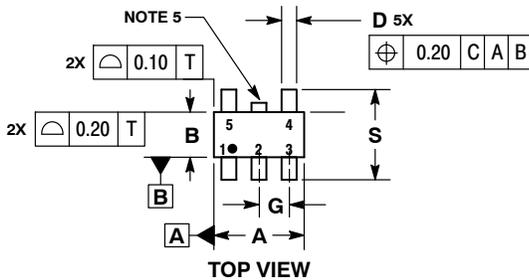
ON Semiconductor®



SCALE 2:1

## TSOP-5 CASE 483 ISSUE N

DATE 12 AUG 2020

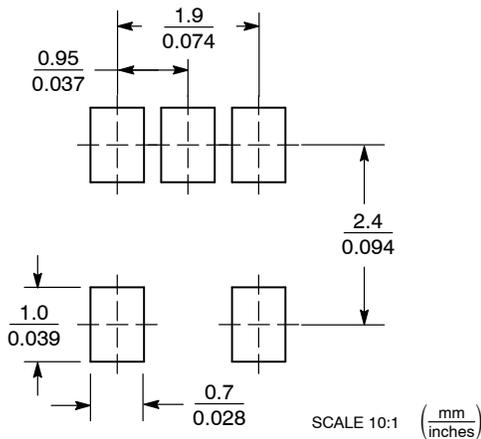


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION A.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

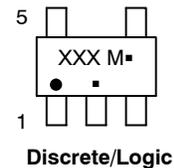
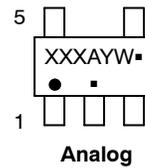
DIM	MILLIMETERS	
	MIN	MAX
A	2.85	3.15
B	1.35	1.65
C	0.90	1.10
D	0.25	0.50
G	0.95 BSC	
H	0.01	0.10
J	0.10	0.26
K	0.20	0.60
M	0°	10°
S	2.50	3.00

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### GENERIC MARKING DIAGRAM\*



- XXX = Specific Device Code  
 A = Assembly Location  
 Y = Year  
 W = Work Week  
 ■ = Pb-Free Package
- XXX = Specific Device Code  
 M = Date Code  
 ■ = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present.

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