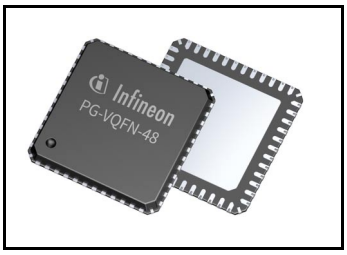
OPTIREG™ SBC TLE9272QXV33

High-End System Basis Chip Family



1 Overview

Features

- Very low quiescent current consumption in SBC Stop and Sleep mode
- SMPS 750 mA (DC/DC buck) voltage regulator 3.3 V to supply high current load with high efficiency
- DC/DC boost converter for low battery supply voltage
- Low-drop voltage regulator 5 V/100 mA, protected for off-board usage
- High-speed CAN FD transceiver compliant to ISO11898-2:2016 supporting communication up to 5 Mbps
- Up to 3 LIN transceivers LIN2.2, SAE J2602 with programmable TXD timeout feature and LIN Flash mode
- Compliant with “Hardware requirements for LIN, CAN and FlexRay interfaces in automotive applications” Revision 1.3, 2012-05-04
- One universal high-voltage wake input for voltage level monitoring
- Configurable wake-up sources including periodic cyclic wake in SBC Normal and Stop mode
- Configurable timeout and window watchdog and reset output
- Fail-safe input to monitor MCU hardware functionality
- Up to three fail-safe outputs (depending on configurations) to activate external loads in case of system malfunctions are detected
- Overtemperature and short circuit protection feature
- Software compatible with latest Infineon SBC families
- PG-VQFN-48 leadless exposed-pad power package with Lead Tip Inspection (LTI)
- Green Product (RoHS compliant)

Potential applications

- Body control modules
- Gateway
- HVAC ECU and control panel

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100.

Description

The TLE9272QXV33 is a monolithic integrated circuit in an exposed pad PG-VQFN-48 (7 mm × 7 mm) leadless package with Lead Tip Inspection (LTI) feature supporting Automatic Optical Inspection (AOI).

The device is designed for various CAN-LIN automotive applications as the main supply for the microcontroller and as the interface for LIN and CAN bus networks.

The System Basis Chip (SBC) provides the main functions for supporting these applications, such as a Switch mode power supply regulator (SMPS) for on-board 3.3 V supply, another 5 V low-dropout voltage regulator with off-board protection, e.g. sensor supply, a DC/DC boost converter for low supply voltage, an HS-CAN transceiver supporting CAN FD, a LIN transceiver for data transmission and a 16-bit Serial Peripheral Interface (SPI) to control and monitor the device. Additional feature include a timeout/window watchdog circuit with a reset feature, fail-safe input and fail-safe outputs and undervoltage reset features.

The device offers low-power modes in order to minimize current consumption on applications that are connected permanently to the battery. A wake-up from the low-power mode is possible via a message on the buses, via the bi-level sensitive monitoring/wake-up input as well as via cyclic wake.

The device is designed to withstand the severe conditions of automotive applications.

Scalable System Basis Chip (SBC) family

- Product family with various products for complete scalable application coverage
- Dedicated datasheets are available for the different product variants
- Complete compatibility (hardware and software) across the family
- TLE9274 with 4 LIN transceivers, SMPS boost with 3 output voltage configurations
- TLE9273 with 4 LIN transceivers, SMPS boost with 2 output voltage configurations
- TLE9272 with 3 LIN transceivers, SMPS boost with 2 output voltage configurations
- TLE9271 with 2 LIN transceivers, SMPS boost with 2 output voltage configurations
- Product variants for 5 V (TLE927xQX) and 3.3 V (TLE927xQXV33) output voltage for main voltage regulator

Sales Product Name	OPN SP number	Package	Marking
TLE9272QXV33	TLE9272QXV33XUMA2 SP005729516	PG-VQFN-48	TLE9272QXV33

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2 Block diagram

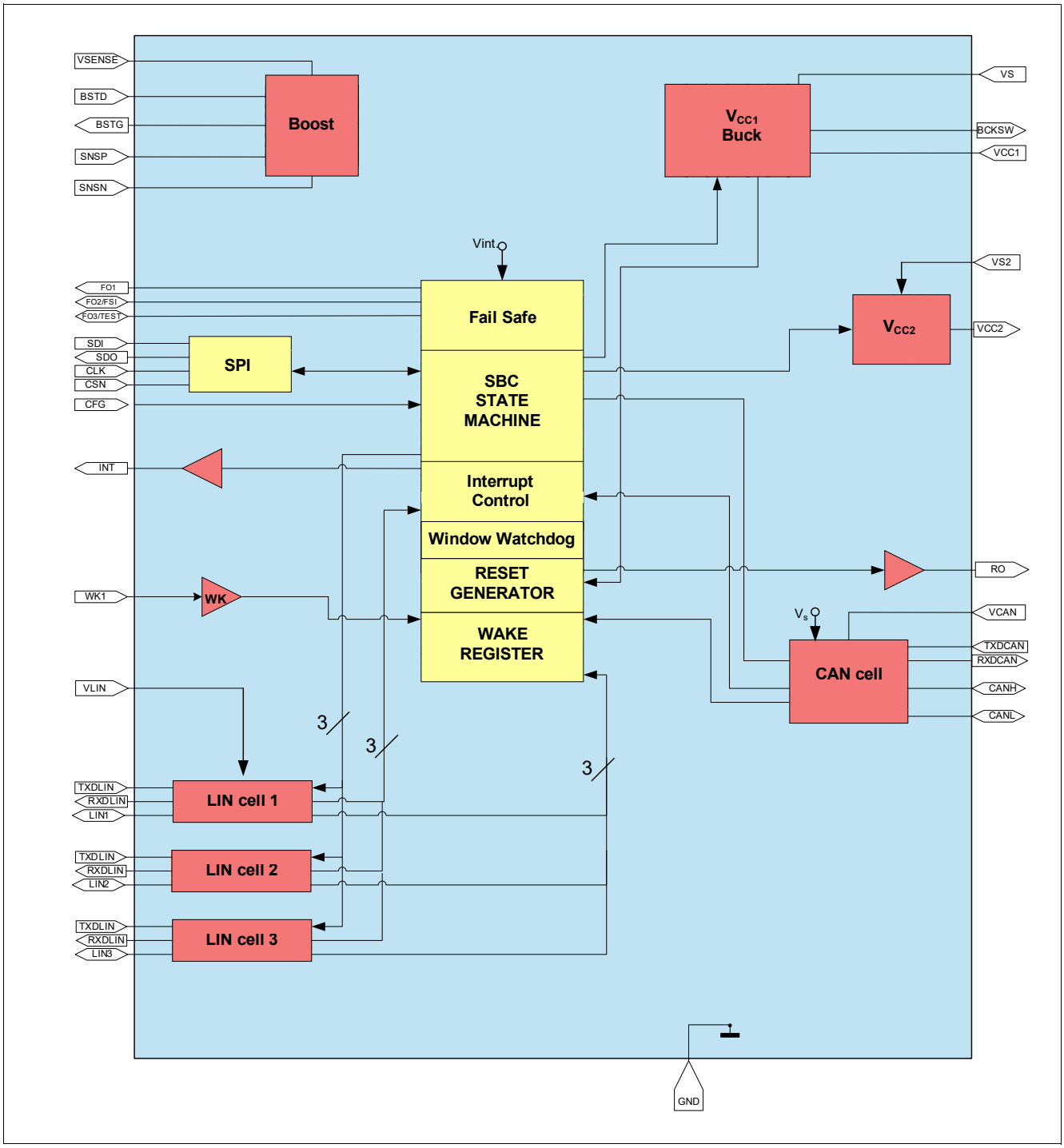

Figure 1 Block diagram

3 Pin configuration

3.1 Pin assignment

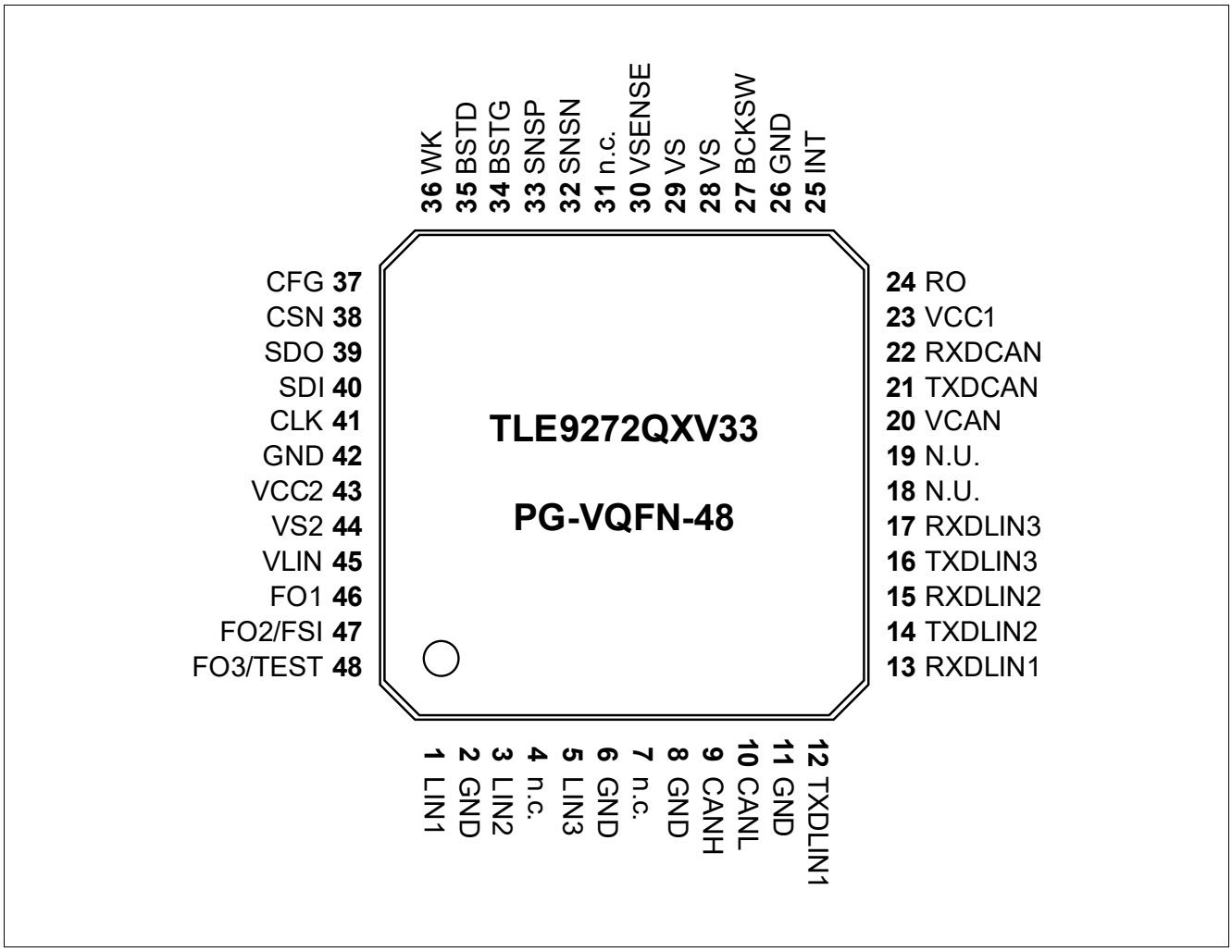

Figure 2 Pin assignment

3.2 Pin definitions and functions

Table 1 Pin definitions and functions

Pin	Symbol	Function
1	LIN1	**LIN bus 1** Bus line for the LIN interface, according to ISO 9141 and LIN specification 2.1 as well as SAE J2602-2
2	GND	**Ground** LIN1 and LIN2 common ground
3	LIN2	**LIN bus 2** Bus line for the LIN interface, according to ISO 9141 and LIN specification 2.1 as well as SAE J2602-2
4	N.C.	**Not connected** Not bonded internally
5	LIN3	**LIN bus 3** Bus line for the LIN interface, according to ISO 9141 and LIN specification 2.1 as well as SAE J2602-2
6	GND	**Ground** LIN3 and LIN4 common ground
7	N.C.	**Not connected** Not bonded internally
8	GND	**Ground**
9	CANH	**CAN high bus pin**
10	CANL	**CAN low bus pin**
11	GND	**Ground** CAN common ground
12	TXDLIN1	**Transmit LIN1**
13	RXDLIN1	**Receive LIN1**
14	TXDLIN2	**Transmit LIN2**
15	RXDLIN2	**Receive LIN2**
16	TXDLIN3	**Transmit LIN3**
17	RXDLIN3	**Receive LIN3**
18	N.U.	**Not used** Used for internal testing purpose. Do not connect, leave open
19	N.U.	**Not used** Used for internal testing purpose. Do not connect, leave open
20	VCAN	**Supply input for internal HS-CAN module**
21	TXDCAN	**Transmit CAN**
22	RXDCAN	**Receive CAN**
23	VCC1	**Buck regulator** Input feedback for buck regulator

Pin configuration

Table 1 Pin definitions and functions

Pin	Symbol	Function
24	RO	**Reset output** Active LOW, internal pull-up
25	INT	**Interrupt output** Active LOW output
26	GND	**Ground** Buck regulator ground
27	BCKSW	**Buck regulator switch node output**
28	VS	**Buck supply voltage** Connected to battery voltage or boost output voltage with reverse protection diode. Use a filter for EMC in case the boost is not used
29	VS	**Buck supply voltage** Connected to battery voltage or boost output voltage with reverse protection diode. Use a filter for EMC in case the boost is not used
30	VSENSE	**Sense input voltage for boost** Boost regulator feedback input. Connect with VS
31	N.C.	**Not connected** Not bonded internally
32	SNSN	**Ground** Boost regulator ground
33	SNSP	**Boost transistor source** Source connection for external MOSFET, sense resistor connection. Connect to GND if boost regulator is not used
34	BSTG	**Boost transistor gate** Gate connection for external MOSFET. Connect to GND or leave open if boost regulator is not used
35	BSTD	**Boost transistor drain** Drain connection for external MOSFET. Connect to VS if boost regulator is not used
36	WK	**Wake input**
37	CFG	**Hardware initialization pin** External pull-up to VCC1 needed. Refer to **Chapter 15**
38	CSN	**SPI Chip select not input**
39	SDO	**SPI Data output** Out of SBC (=MISO)
40	SDI	**SPI Data input** Into SBC (=MOSI)
41	CLK	**SPI Clock input**
42	GND	**Ground**
43	VCC2	**Voltage regulator output 2**

Pin configuration

Table 1 Pin definitions and functions

Pin	Symbol	Function
44	VS2	**Supply voltage for VCC2** Connected to battery voltage with reverse protection diode and filter against EMC.
45	VLIN	**Reference voltage for LIN** Connected to battery voltage with reverse protection diode and filter against EMC
46	FO1	**Fail output 1** Active LOW, open drain
47	FO2/FSI	**Fail output 2 - Side indicator** Side indicator 1.25 Hz 50% duty cycle output; active LOW, open drain **FSI** Fail-safe input (default configuration)**;** connect to GND if not used
48	FO3/TEST	**Fail output 3 - Pulsed lighted output** Break/rear light 100 Hz 20% duty cycle output; active LOW, open-drain **TEST** Connect to GND to activate SBC Development mode; integrated pull-up resistor. Connect to VS with a pull-up resistor or leave open for normal operation
Exposed pad	GND	Connect the exposed pad to GND. It is recommended to connect the exposed pad to a heat sink[1)]

1) The exposed die pad at the bottom of the package allows better power dissipation of heat from the SBC via the PCB. The exposed die pad is not connected to any active part of the IC. However it should be connected to GND for the best EMC performance.

3.3 Hints for unused pins

It must be ensured that the correct configurations are also selected, i.e. in case functions are not used that they are disabled via SPI:

- WK: connected to GND and disable the WK input via SPI
- LINx, RXDLINx, TXDLINx, RXDCAN, TXDCAN, CANH, CANL: leave all pins open
- BSTD: connect to VS in case the boost regulator is not used and keep disabled
- BSTG: connect to GND or leave open in case the boost regulator is not used and keep disabled
- SNSP, SNSN: connect to GND in case the boost regulator is not used
- RO / FOx: leave open
- INT: leave open
- TEST: connect to GND during power-up to activate SBC Development mode; connect to VS or leave open for normal user mode operation
- VCC2: leave open and keep disabled
- VCAN: connect to VCC1
- N.C.: not connected, not bonded internally, leave open
- Unused pins routed to an external connector which leaves the ECU should feature a zero ohm jumper (depopulated if unused) or ESD protection

4 General product characteristics

4.1 Absolute maximum ratings

Table 2 Absolute maximum ratings[1)]

T_j = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltages							
Supply voltage VS pin	$V_{S, max}$	-0.3	–	28	V	–	P_4.1.1
Supply voltage VS2 pin	$V_{S2, max}$	-0.3	–	28	V	–	P_4.1.25
Supply voltage VS pin	$V_{S, max}$	-0.3	–	40	V	Load dump, max. 400 ms	P_4.1.2
Supply voltage VS2 pin	$V_{S2, max}$	-0.3	–	40	V	Load dump, max. 400 ms	P_4.1.26
LIN supply voltage VLIN pin	$V_{LIN, max}$	-0.3	–	40	V	–	P_4.1.12
Boost drain voltage BSTD pin	$V_{BSTD, max}$	-0.3	–	28	V	–	P_4.1.19
Boost drain voltage BSTD pin	$V_{BSTD, max}$	-0.3	–	40	V	Load dump, max. 400 ms	P_4.1.20
Boost gate voltage BSTG pin	$V_{BSTG, max}$	-0.3	–	40	V	–	P_4.1.21
Supply voltage SNSP pin	$V_{SNSP, max}$	-0.3	–	40	V	–	P_4.1.22
Sense voltage VSENSE pin	$V_{SENSE, max}$	-0.3	–	40	V	–	P_4.1.23
Buck switch BCKSW pin	$V_{BCKSW, max}$	-0.3	–	V_S + 0.3	V	–	P_4.1.24
Buck regulator feedback, pin VCC1	$V_{CC1, max}$	-0.3	–	5.5	V	–	P_4.1.3
Voltage regulator 2 output, pin VCC2	$V_{CC2, max}$	-0.3	–	40	V	–	P_4.1.5
Wake input	$V_{WK, max}$	-0.3	–	40	V	–	P_4.1.6
Fail pins FO1, FO2/FSI, FO3/TEST	$V_{FOx, max}$	-0.3	–	40	V	–	P_4.1.7
Configuration pin CFG	$V_{CFG, max}$	-0.3	–	V_{CC1} + 0.3	V	–	P_4.1.8
LINx, CANH, CANL	$V_{BUS, max}$	-27	–	40	V	–	P_4.1.9
V_{diff} = CANH - CANL	V_{DIFF}	-5	–	10	V	–	P_4.1.28
Logic input voltage	$V_{I, max}$	-0.3	–	V_{CC1} + 0.3	V	–	P_4.1.10

Table 2 Absolute maximum ratings[1)] (cont'd)

T_j = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Logic output voltage	$V_{O, max}$	-0.3	–	V_{CC1} + 0.3	V	–	P_4.1.27
VCAN Input voltage	$V_{VCAN, max}$	-0.3	–	5.5	V	–	P_4.1.11
Temperatures							
Junction temperature	T_j	-40	–	150	°C	–	P_4.1.13
Storage temperature	T_{stg}	-55	–	150	°C	–	P_4.1.14
ESD susceptibility							
ESD resistivity to GND	V_{ESD}	-2	–	2	kV	HBM[2)]	P_4.1.15
ESD resistivity to GND, CANH, CANL, LINx	V_{ESD}	-8	–	8	kV	HBM[3)2)]	P_4.1.16
ESD resistivity to GND	V_{ESD}	-500	–	500	V	CDM[4)]	P_4.1.17
ESD resistivity pin 1, 12, 13, 24, 25, 36, 37, 48 (corner pins) to GND	$V_{ESD1,12,13,24,25,36,37,48}$	-750	–	750	V	CDM[4)]	P_4.1.18

1) Not subject to production test, specified by design.

2) ESD susceptibility, "HBM" according to ANSI/ESDA/JEDEC JS-001 (1.5 kΩ, 100 pF).

3) For ESD GUN resistivity, tested at 6 kV (according to IEC61000-4-2 "gun test" (330 Ω, 150 pF)), it is shown in application information and test report, provided from IBEE, is available.

4) ESD susceptibility, Charged Device Model "CDM" according to ANSI/ESDA/JEDEC JS-002.

Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the datasheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*

4.2 Functional range

Table 3 Functional range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply voltage	$V_{S,func}$	V_{POR}	–	28	V	[1] V_{POR} see **Chapter 13.9**	P_4.2.1
LIN supply voltage (VLIN pin)	$V_{REF,LIN}$	5.5	–	18	V		P_4.2.2
CAN supply voltage	V_{CAN}	4.75	–	5.25	V	–	P_4.2.3
CFG external pull-up	R_{CFG}	10	–	22	kΩ	–	P_4.2.6
SPI frequency	f_{SPI}	–	–	4	MHz	see **Chapter 14.7** for $f_{SPI,max}$	P_4.2.4
Junction temperature	T_j	-40	–	150	°C	–	P_4.2.5

1) Including power-on reset, overvoltage and undervoltage protection.

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

Device behavior outside of specified functional range

- 28 V < $V_{S,func}$ < 40 V: Device will still be functional; the specified electrical characteristics may not be ensured anymore. The buck and VCC2 will work, however, a thermal shutdown may occur due to high power dissipation. The specified SPI communication speed is ensured. The absolute maximum ratings are not violated, however the device is not intended for continuous operation of V_S > 28 V. Operating the device at high junction temperatures for prolonged periods of time may reduce the life of the device
- 18 V < V_{LIN} < 28 V: The LIN transceiver is still functional. However, the communication may fail due to out-of-LIN-spec operation
- **$V_{LIN,UVD}$** < V_{LIN} < 5.5 V: The LIN transceiver is still functional. However, the communication may fail due to out-of-LIN-spec operation
- V_{CAN} < 4.75 V: The undervoltage bit **VCAN_UV** will be set in the SPI register **BUS_STAT_1** and the transmitter will be disabled as long as the UV condition is present
- 5.25 V < V_{CAN} < 5.50 V: CAN transceiver still functional. However, the communication may fail due to out-of-spec operation
- **$V_{POR,f}$** < V_S < 5.5 V: Device will be still functional; the specified electrical characteristics may not be ensured anymore:
  - The voltage regulators will enter the low-drop operation mode
  - A **VCC1_UV** reset could be triggered depending on the Vrtx settings
  - The LIN transmitter will be disabled if V_{LIN} < **$V_{LIN,UVD}$** is reached and **VLIN_UV** bit on **SUP_STAT** is set
  - FOx outputs will remain ON if they were enabled
  - The specified SPI communication speed is ensured

4.3 Thermal resistance

Table 4 Thermal resistance[1)]

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to soldering point	R_{thJSP}	–	6	–	K/W	Exposed Pad	P_4.3.1
Junction to ambient	R_{thJA}	–	33	–	K/W	[2)]	P_4.3.2

1) Not subject to production test, specified by design.

2) According to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board for 1.5 W. Board: 76.2 x 114.3 x 1.5 mm^3 with 2 inner copper layers (35 µm thick), with a thermal via array under the exposed pad contacting the first inner copper layer and 300 mm^2 cooling area on the bottom layer (70 µm). For more details, refer to **Chapter 15.4**.

4.4 Current consumption

Table 5 Current consumption

Current consumption values are specified at T_j = 25°C, V_S = 13.5 V, all outputs open (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
SBC Normal mode							
Normal mode current consumption	I_{Normal}	–	5	10	mA	5.5 V < V_S < 28 V no load on VCC1 T_j = -40°C to +150°C VCC2 / CAN / LIN / BOOST = OFF	P_4.4.1
SBC Stop mode							
Stop mode current consumption	$I_{Stop,25}$	–	50	65	µA	1)2) T_j = 25°C Buck module in PFM no load on VCC1 VCC2 = OFF; CAN / LINx = OFF Watchdog = OFF WK enabled BOOST = OFF	P_4.4.2
Stop mode current consumption	$I_{Stop,85}$	–	95	–	µA	1)2)3) T_j = 85°C; Buck module in PFM no load on VCC1 VCC2 = OFF; CAN / LINx = OFF Watchdog = OFF WK enabled BOOST = OFF	P_4.4.3
Stop mode current consumption, VCC2 enabled	$I_{Stop,VCC2,25}$	–	70	95	µA	1)2) T_j = 25°C Buck module in PFM no load on VCC1 VS2 = VS VCC2 = ON (no load); CAN / LINx = OFF Watchdog = OFF WK enabled BOOST = OFF	P_4.4.4

Table 5 Current consumption (cont'd)

Current consumption values are specified at T_j = 25°C, V_S = 13.5 V, all outputs open (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Stop mode current consumption, cyclic wake	$I_{Stop,C25}$	–	65	85	µA	1)2) T_j = 25°C Buck module in PFM no load on VCC1 VCC2 = OFF; CAN / LINx = OFF Watchdog = ON WK enabled BOOST = OFF	P_4.4.5
SBC Sleep mode							
Sleep mode current consumption	$I_{Sleep,25}$	–	30	50	µA	1) T_j = 25°C VCC1,VCC2 = OFF CAN / LINx = OFF, WK enabled	P_4.4.6
Sleep mode current consumption	$I_{Sleep,85}$	–	80	–	µA	1)3) T_j = 85°C VCC1,VCC2 = OFF CAN / LINx = OFF WK enabled	P_4.4.13
Sleep mode current consumption, VCC2 enabled	$I_{Sleep,VCC2,25}$	–	50	75	µA	1) T_j = 25°C VCC1= OFF VS2 = VS VCC2 = ON (no load) CAN / LINx = OFF WK enabled	P_4.4.7
Incremental current consumption							
Current consumption for CAN, recessive state	$I_{CAN,rec}$	–	2	3	mA	VCAN = VCC2 SBC Normal mode CAN Normal mode VTXDCAN = 5 V no RL on CAN	P_4.4.8
Current consumption for CAN, dominant state	$I_{CAN,dom}$	–	3	4.5	mA	3)VCAN = 5V SBC Normal mode CAN Normal mode VTXDCAN = GND no RL on CAN	P_4.4.14
Current consumption for CAN module, Receive-Only mode	$I_{CAN,RevOnly}$	–	1	2	mA	1) VCAN = VCC2 SBC Normal / Stop mode CAN Receive-Only mode VTXDCAN = 5 V no RL on CAN	P_4.4.9

Table 5 Current consumption (cont'd)

Current consumption values are specified at T_j = 25°C, V_S = 13.5 V, all outputs open (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current consumption for CAN module wake capability	$I_{CAN,wake}$	–	4.5	6	µA	[1] SBC Stop/Sleep/Fail-Safe mode; CAN wake capable; LIN1…4 = OFF	P_4.4.10
Current consumption per LIN module, recessive state	$I_{LIN,rec}$	–	0.1	1.0	mA	SBC Normal mode LIN Normal mode; VTXDLIN = VCC1; no RL on LIN	P_4.4.15
Current consumption per LIN module, dominant state	$I_{LIN,dom}$	–	1.0	1.5	mA	[3] SBC Normal mode LIN Normal mode; VTXDLIN = GND; no RL on LIN	P_4.4.16
Current consumption per LIN module, Receive-Only mode	$I_{LIN,RcVOnly}$	–	0.1	0.2	mA	[3] SBC Normal / Stop mode LIN Receive-Only mode; VTXDLIN = VCC1; no RL on LIN	P_4.4.17
Current consumption per LIN module wake capability	$I_{LIN,wake}$	–	0.2	2	µA	[1] SBC Stop/Sleep/Fail-Safe mode; CAN wake capable; LIN wake capable	P_4.4.11
WK pin current consumption wake capable	$I_{WK,wake}$	–	0.2	2	µA	SBC Normal/Stop/ Sleep/Fail-Safe mode; WK wake capable; LIN1…4, CAN = OFF	P_4.4.12
Additional VS current consumption with boost module active	$I_{BOOST,ON}$	–	5	10	mA	[3] SBC Normal/Stop mode VBSTx < VS < VBST,thx BOOST = ON	P_4.4.18

1) Current consumption for CAN,LIN transceivers and WK input to be added if set to be wake capable or receiver only.
2) If the buck regulator is working in PWM, the P_4.4.1 has to be added.
3) Specified by design; not subject to production test.

5 System features

This chapter describes the system features and behavior of the TLE9272QXV33:

- State machine and SBC mode control
- Device configurations
- State of supply and peripherals
- Wake features
- Supervision and diagnosis functions

The System Basis Chip (SBC) offers six operating modes:

- SBC Init mode: power-up of the device and after soft reset
- SBC Normal mode: the main operating mode of the device
- SBC Stop mode: the first-level power saving mode with the main voltage regulator VCC1 enabled
- SBC Sleep mode: the second-level power saving mode with VCC1 disable
- SBC Restart mode: an intermediate mode after a wake event from SBC Sleep or SBC Fail-Safe mode or after a failure (e.g. WD failure, VCC1 undervoltage reset) to bring the microcontroller into a defined state via a reset. Once the failure condition is not present anymore, the device will automatically change to SBC Normal mode after a delay time (t_{RD1})
- SBC Fail-Safe mode: a safe-state mode after critical failures (e.g. TSD2 thermal shutdown, VCC1 short to GND) to bring the system into a safe state and to ensure a proper restart of the system. VCC1 is disabled. This is a permanent state until either a wake event (via CAN, LINx or WK pin) occurs and the overtemperature condition is not present anymore

A special mode called SBC Development mode is available during software development or debugging of the system. All of the operating modes mentioned above can be accessed in this mode. However, the watchdog counter is stopped and does not need to be triggered. This mode can be accessed by setting the TEST pin to GND during SBC Init mode.

The System Basis Chip is controlled via a 16-bit SPI interface. A detailed description can be found in **Chapter 14**. The configuration as well as the diagnosis is handled via the SPI. The SPI mapping of the high-end SBC family TLE927xQX is compatible with the latest Infineon SBC devices.

5.1 State machine description and SBC mode control

The different SBC modes are selected via SPI by setting the respective SBC **MODE** bits in the register **M_S_CTRL**. The SBC **MODE** bits are cleared when going trough SBC Restart mode, so the current SBC mode is always shown.

The **Figure 3** shows the SBC state diagram.

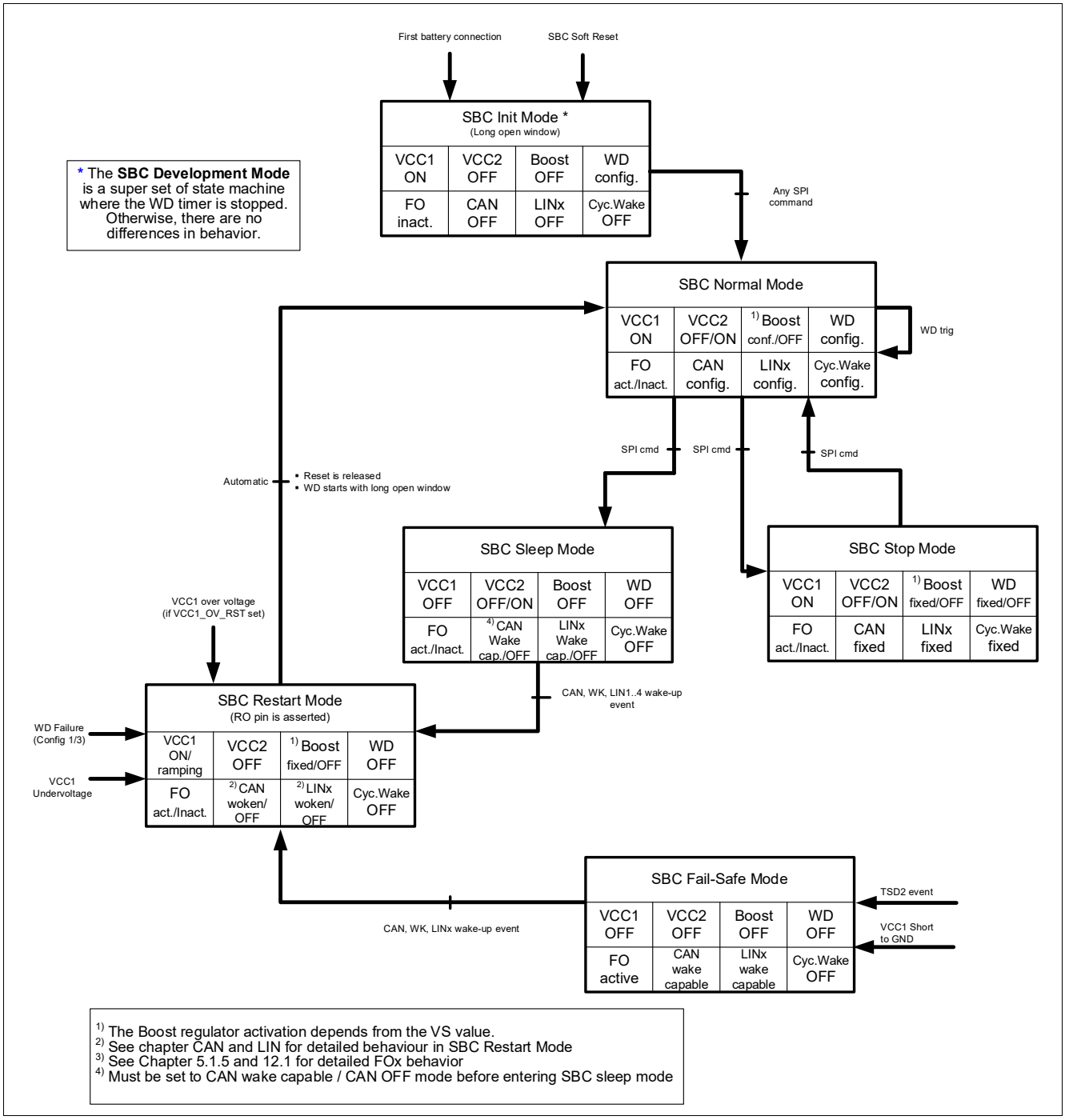

Figure 3 State diagram showing the SBC operating modes

5.1.1 SBC Init mode and device configuration

The SBC Init mode is the mode where the hardware configuration of the SBC is stored and where the microcontroller finishes the initialization phase. During the SBC Init mode, the SBC can be configured in normal operation or in SBC Development mode (see also **Chapter 5.1.7**).

The hardware configuration is done monitoring the level of FO3/TEST pin. The pin FO3/Test is set as an input and one internal pull-up resistor is activated (R_{TEST}). The **Table 6** shows possible hardware configurations.

Table 6 SBC configuration

Configuration	Description	FO3/Test pin	TEST	CFG2_ STATE
Config 0	SBC Development mode: no reset is triggered in case of a watchdog trigger failure. After the power-up, one arbitrary SPI command must be sent	0	1	X
Config 1	After missing the WD trigger for the first time, the state of V_{CC1} remains unchanged, FOx pins are active, SBC Restart mode	Open or > $V_{TEST,H}$	0	1
Config 3	After missing the WD trigger for the second time, the state of V_{CC1} remains unchanged, FOx pins are active, SBC Restart mode	Open or > $V_{TEST,H}$	0	0

An external pull-up resistor on CFG pin (R_{CFG}) is needed for proper SBC configuration. The config 1 or 3 is selectable via SPI using **CFG2** bit on **HW_CTRL** register.

The timing diagram for hardware configuration is shown in **Figure 4**.

The SBC starts up in SBC Init mode after crossing the $V_{POR,r}$ threshold (see also **Chapter 13.3**) or after a software reset command. As soon as the VCC1 voltage reaches the rising reset threshold $V_{RT1,r}$, the configuration selection monitoring period starts for t_{RD1} (Reset delay time). After this time, the reset pin is released and the window watchdog starts with a long open window t_{LW}.

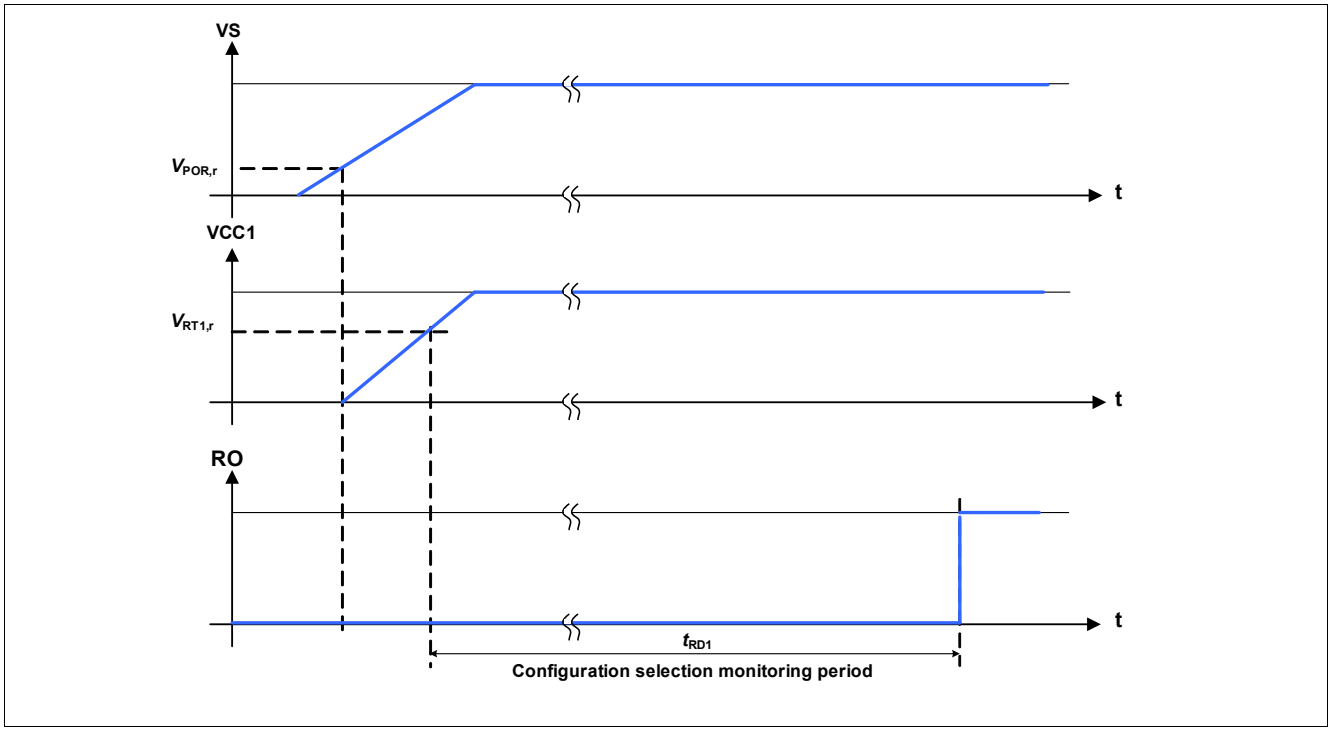

Figure 4 Hardware configuration selection timing diagram

During the long open window, the microcontroller needs to finish its startup and initialization sequence. From this transition mode, the SBC can be set, via SPI command, to SBC Normal mode.

Any SPI command will bring the SBC to SBC Normal mode even if it is an illegal SPI command (**Chapter 14.2**).

No watchdog trigger during the long open window, will cause a watchdog failure and the device will enter in SBC Restart mode as shown in **Table 6** and one reset event is generated.

In case of 3 consecutive reset events due to WD failures, it is possible not to generate additional reset by setting the **MAX_3_RST** on **WD_CTRL** and the SBC will remain in SBC Normal or Stop mode (SBC Restart mode not entered anymore). If the **MAX_3_RST** is set to 0, one reset event is generated for each missing watchdog trigger.

Wake-up events are ignored during SBC Init mode and will therefore be lost.

Notes

1. *Any SPI command will bring the SBC to SBC Normal mode even if it is an illegal SPI command (see **Chapter 14.2**).*
2. *For a safe start-up, it is recommended to use the first SPI commands to trigger and to configure the watchdog.*
3. *At power up no **VCC1_UV** will be issued nor will the FOx be triggered as long as VCC1 is below $V_{RT1,r}$ threshold and below the VS threshold for VS under voltage time out V_{S,UV_TO}. The RO pin will be kept low as long as VCC1 is below the selected $V_{RT1,r}$ threshold. When VCC1 is above the $V_{RT1,r}$ threshold, the RO is released after t_{RD1} (Reset delay time).*

5.1.2 SBC Normal mode

The SBC Normal mode is the standard operating mode for the SBC. All configurations have to be done in SBC Normal mode before entering a low-power mode. A wake-up event on CAN LIN1, LIN2, LIN3 and WK will create an interrupt on pin INT however, no changes of SBC mode will occur. The configuration options are listed below:

- VCC1 is active (buck regulator in PWM mode)
- Boost regulator can be configured and enabled or disabled. The module will start to work as soon as the VS value is dropping below the selected threshold. For additional information, refer to **Chapter 6.3**
- VCC2 can be switched ON or OFF (default off)
- CAN is configurable (OFF coming from SBC Init mode; OFF or wake capable coming from SBC Restart mode, see also **Chapter 5.1.5**)
- LIN is configurable (OFF coming from SBC Init mode; OFF or wake capable coming from SBC Restart mode, see also **Chapter 5.1.5**)
- Wake pin shows the input level and can be selected to be wake capable
- Cyclic wake can be configured with timer1
- Watchdog is configurable
- FO1 and FO3 are OFF and FSI is active by default. FSI can be configured to be fail-safe output (see also **Chapter 12.2**). Coming from SBC Restart mode, the FOx can be active or inactive (see also **Chapter 12.1**)

In SBC Normal mode, there is the possibility of testing the FO outputs, i.e. to verify if setting the FOx pins to low will create the intended behavior within the system. The FO outputs can be enabled and then disabled again by the microcontroller by setting the **FO_ON** SPI bit. The feature is only intended for testing purposes.

5.1.3 SBC Stop mode

The SBC Stop mode is the first level technique to reduce the overall current consumption. In this mode VCC1 regulator is still active and supplying the microcontroller, which can enter into a power down mode.

The VCC2 could be enabled or disabled, CAN and LIN can be configured as Receive-Only mode, or wake capable or disable. All kind of settings have to be done before entering SBC Stop mode. In SBC Stop mode any kind of SPI WRITE commands are ignored and the **SPI_FAIL** bit is set, except for changing to SBC Normal mode, triggering a SBC soft reset, refreshing the watchdog, write the SYS_STAT_CTRL register as well as reading and clearing the SPI status registers. A wake-up event on CAN, LIN1, LIN2, LIN3 and WK will create an interrupt on pin INT - however, no change of SBC mode will occur. The configuration options are listed below:

- VCC1 is ON (buck regulator in PFM mode)
- Boost regulator is fixed as configured in SBC Normal mode. The module will start to work as soon as the VS value drops below the selected threshold
- VCC2 is fixed as configured in SBC Normal mode
- CAN is fixed as configured in SBC Normal mode
- LIN is fixed as configured in SBC Normal mode
- WK is fixed as configured in SBC Normal mode
- Cyclic wake is fixed as configured in SBC Normal mode

*Note: It is not possible to switch directly from SBC Stop mode to SBC Sleep mode. Doing so will also set the **SPI_FAIL** flag and will bring the SBC into Restart mode.*

5.1.4 SBC Sleep mode

The SBC Sleep mode is the second level technique to reduce the overall current consumption to a minimum needed to react on wake-up events. In this mode, VCC1 regulator is OFF and not supplying the microcontroller anymore.The VCC2 supply can be configured to stay enabled. A wake-up event on CAN, LIN1, LIN2, LIN3 or WK pin return the device to SBC Normal mode via SBC Restart mode and signal the wake source.

The configuration options are listed below:

- VCC1 is OFF
- Boost regulator is OFF
- VCC2 is fixed as configured in SBC Normal mode
- Can must be set to CAN wake capable / CAN off before entering SBC Sleep mode
- LIN is fixed as configured in SBC Normal mode
- WK is fixed as configured in SBC Normal mode

It is not possible to switch off all wake sources in SBC Sleep mode. When a CAN or LIN transceiver is in its Normal or Receive-Only mode, it counts as a wake source. In that case it changes automatically to wake capable when the SBC enters SBC Sleep mode.

All settings must be made before entering SBC Sleep mode. If SPI configurations were sent to the SBC in SBC Sleep mode, the commands are ignored and there is no response from the SBC.

In order to enter SBC Sleep mode successfully, all wake source signaling flags from **WK_STAT_1** and **WK_STAT_2** need to be cleared. Otherwise, the device will immediately wake-up from SBC Sleep mode by going via SBC Restart to Normal mode.

Note: As soon as the sleep command is sent, the reset will go low to avoid any undefined behavior between SBC and microcontroller.

5.1.5 SBC Restart mode

There are multiple reasons to enter the SBC Restart mode. The purpose of the SBC Restart mode is to reset the microcontroller:

- From SBC Normal and Stop mode:
  - Undervoltage on VCC1
  - Overvoltage on VCC1 (if **VCC1_OV_ RST** is set)
  - Incorrect Watchdog triggering
- From SBC Sleep and Fail-Safe mode:
  - Wake-up event on CAN or LINx or WK
  - After TDS2 (only from SBC Fail-Safe mode. See also **Chapter 13.8**)

Table 7 contains detailed descriptions of the reason to restart.

Table 7 Reasons for restart - state of SPI status bits after return to Normal mode

SBC mode	Event	DEV_STAT	WD_FAIL	VCC1_UV	VCC1_OV	VCC1_SC
Normal mode	Watchdog failure	01	01 or 10	0	x	x
Normal mode	VCC1 undervoltage reset	01	xx	1	0	x
Normal mode	VCC1 overvoltage reset	01	xx	0	1	x
Sleep mode	Wake-up event	10	00	0	x	x
Stop mode	Watchdog failure	01	01 or 10	0	x	x
Stop mode	VCC1 undervoltage reset	01	xx	1	0	x
Stop mode	VCC1 overvoltage reset	01	xx	0	1	x
Fail-Safe mode	Wake-up event	01	see “Reasons for Fail-safe, **Table 8**”			

It is possible to change the entering into SBC Restart mode due to watchdog trigger failure using **MAX_3_RST** on **WD_CTRL** register. If the **MAX_3_RST** is set, after three consecutive resets, no further reset events are generated in case of missing watchdog trigger (see also **Chapter 13.2**).

From SBC Restart mode, the SBC automatically enters to SBC Normal mode, i.e. the mode is left automatically by the SBC without any microcontroller influence once the reset condition is no longer present and when the reset delay time (t_{RD1}) has expired. The Reset output (RO) is released at the transition.

Entering or leaving SBC Restart mode will not disable the fail outputs.

The following functions are activated / deactivated in SBC Restart mode:

- VCC1 is ON or ramping up
- Boost regulator is fixed as configured in SBC Normal mode. The module will start to work as soon as the VS value drops below the selected threshold
- VCC2 will be disabled if it was activated
- CAN is “woken” due to a wake-up event or OFF depending on previous SBC and transceiver mode (see also **Chapter 8**). It is wake capable when it was in CAN Normal, Receive-Only or wake capable mode before SBC Restart mode
- LINx are “woken” due to a wake-up event or OFF depending on previous SBC and transceiver mode (see also **Chapter 9**). It is wake capable when it was in LINx Normal, Receive-Only or wake capable mode before SBC Restart mode

- RO is pulled low during SBC Restart mode
- SPI communication is ignored by the SBC, i.e. it is not interpreted
- SBC Restart mode is signalled in the SPI register **DEV_STAT** by **DEV_STAT** bits

*Note: The VCC1 overvoltage reset is by default disabled. To enable it, the **VCC1_OV_ RST** has to be set. For additional information, refer to **Chapter 13.5.2**.*

5.1.6 SBC Fail-Safe mode

The purpose of this mode is to bring the system in a safe status after a failure condition by turning off the VCC1 regulator and the RO will be LOW. After a wake-up event, the system can restart.

The Fail-Safe mode is automatically reached in case of following events:

- Overtemperature (TSD2) (see also **Chapter 13.8**)
- VCC1 is shorted to GND (see also **Chapter 13.5.3**)

In this case, the default wake sources are activated and the voltage regulators are switched OFF.
The mode will be maintained for at least typical 1s (t_{TSD2}) for a TSD2 event and typical 100 ms ($t_{FS,min}$) for the other failure events to avoid any fast toggling behavior. All wake sources will be disabled during this time but wake-up events will be stored. Stored wake-up events and wake-up events after this minimum waiting time will lead to SBC Restart mode. Leaving the SBC Fail-Safe mode will not result in deactivation of the FOx pins.

The following functions are influenced during SBC Fail-Safe mode:

- FO outputs are activated (see also **Chapter 12**)
- VCC1 is OFF
- Boost regulator is OFF
- VCC2 is OFF
- CAN is wake capable
- LINx are wake capable
- WK is wake capable
- Cyclic wake is disabled, static sense is active with default filter time
- SPI communication is disabled because VCC1 is OFF

Table 8 Reasons for fail-safe - state of SPI status bits after return to Normal mode

Mode	Config	Event	DEV_STAT	TSD2	WD_FAIL	VCC1_UV	VCC1_SC
Normal	1, 3	TSD2	01	1	xx	x	0
Normal	1, 3, 4	VCC1 short to GND	01	x	xx	1	1
Stop mode	1, 3	TSD2	01	1	xx	x	0
Stop mode	1, 3	VCC1 short to GND	01	x	xx	1	1

5.1.7 SBC Development mode

The SBC Development mode is used during development phase of the application, especially for software development. The mode is reached by setting the FO3/TEST pin to LOW when the device is in SBC Init mode and by sending an arbitrary SPI command. The SBC Init mode is reached after the power-up.

When sending a software reset, it is no longer possible to enter SBC Development mode.

The software reset is the SPI command that set the **MODE** bits in **M_S_CTRL** register.

SBC Development mode can only be left by a power-down while FO3/TEST pin is high or open, or by setting the **MODE** bits on **M_S_CTRL** SBC Software Reset regardless of the state of FO3/TEST.

In this mode, the watchdog does not need to be triggered. No reset is triggered because of watchdog failure.

When the FO3/TEST pin is left open, or connected to VS during the start-up, the SBC starts into normal operation. The FO3 pin has an integrated pull-up resistor, **R_{TEST}**, (switched ON only during SBC Init mode) to prevent the SBC device from starting in SBC Development mode during normal life of the vehicle.

5.2 Wake features

The following wake sources are implemented in the device:

- Static Sense: WK input is permanently active (see **Chapter 10**)
- Cyclic Wake: internal wake source controlled via internal timer (see **Chapter 5.2.1**)
- CAN wake: wake-up via CAN pattern (see **Chapter 8**)
- LIN wake: wake-up via LIN bus (see **Chapter 9**)

The wake source must be set before entering in SBC Sleep mode. In case of critical situation when the device will be set into SBC Fail-Safe mode, all default wake sources will be activated.

5.2.1 Cyclic wake

The cyclic wake feature is intended to reduce the quiescent current of the device and application.

For the cyclic wake feature, timer 1 is configured as internal wake-up source and will periodically trigger an interrupt in SBC Normal and Stop mode based on the setting of **TIMER1_CTRL**.

The correct sequence to configure the cyclic wake is shown in **Figure 5**.

The sequence is as follows:

- Configure the respective period of timer1 in the register **TIMER1_CTRL**
- Enable timer1 as a wake-up source in the register **WK_CTRL_1**

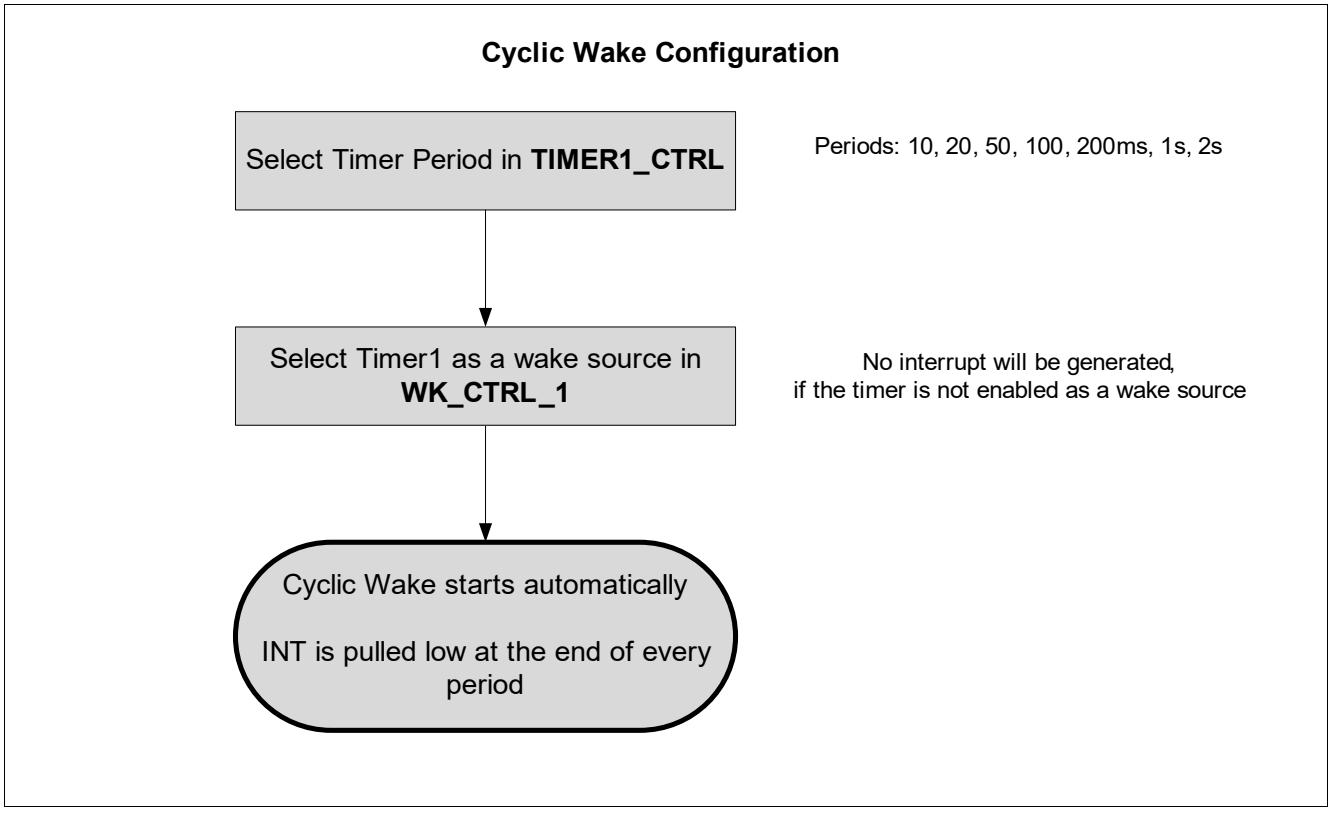

Figure 5 Cyclic wake: configuration and sequence

The cyclic wake function will start as soon as the timer1 is enabled as wake-up source. An interrupt is generated at the end of every period.

5.2.2 Internal timer

The integrated timer is typically used to wake up the microcontroller periodically (cyclic wake).

The following periods can be selected via the register **TIMER1_CTRL**:

- Period: 10 ms / 20 ms / 50 ms / 100 ms / 200 ms / 1 s / 2 s

5.3 Supervision features

The device offers various supervision features to support functional safety requirements. Refer to **Chapter 13** for more information.

6 DC/DC regulators

6.1 Block description

The SMPS module in the TLE9272QXV33 is implemented as a cascade of a step-up pre-regulator followed by a step-down post-regulator. The step-up pre-regulator (DC/DC boost converter) provides a VS level which permits the step-down post-regulator (DC/DC buck converter) to regulate without entering a low-drop condition.

The SMPS module is active in SBC Normal, Stop and Restart mode. In SBC Sleep and Fail-Safe mode, the SMPS module is disabled.

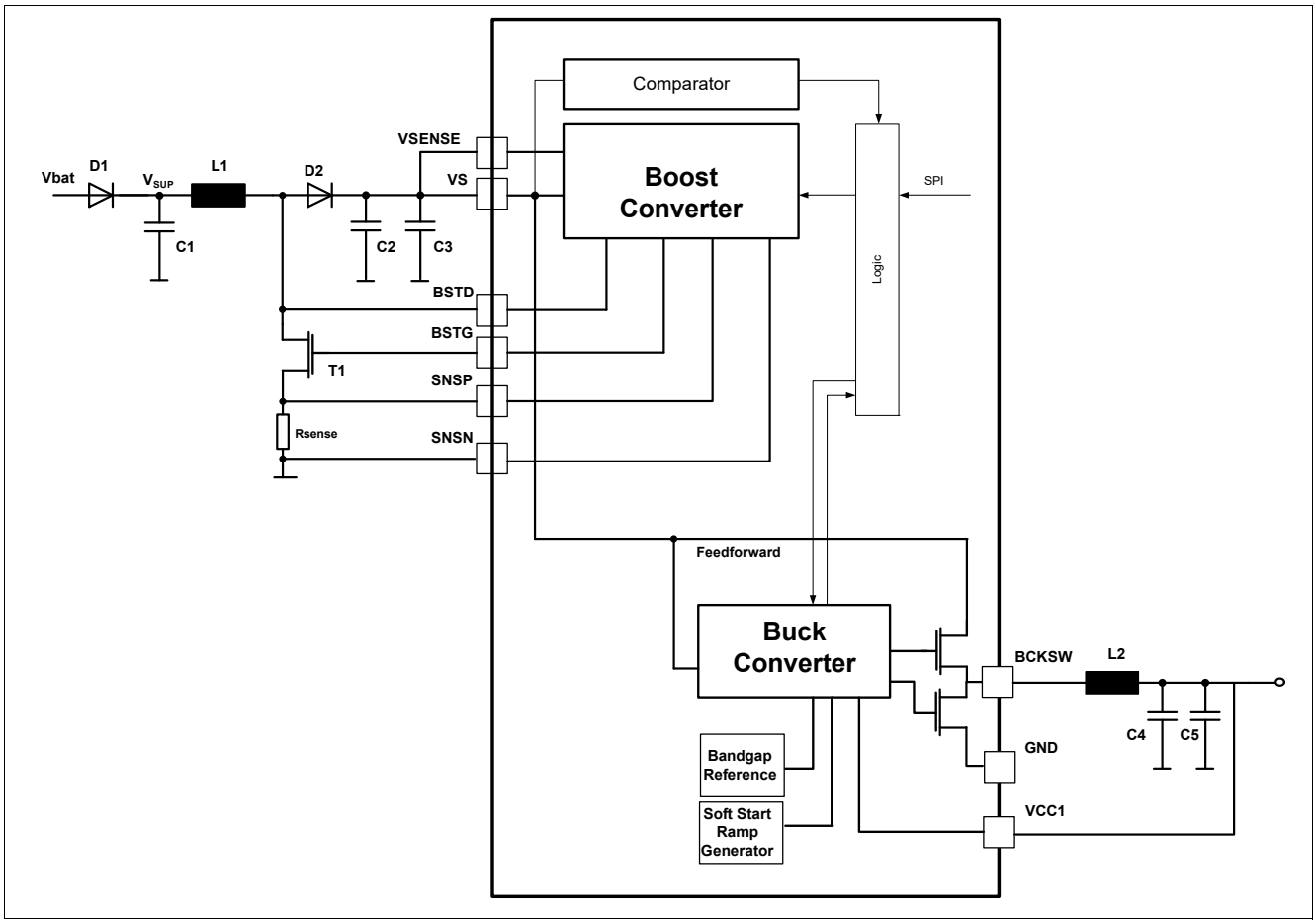

Figure 6 DC/DC block diagram

Functional features

- 3.3 V SMPS (DC/DC) buck converter with integrated high-side and low-side power switching transistor
- SMPS (DC/DC) boost converter as pre-regulator for low VSUP supply voltage (down to 3 V) with configurable output voltage via SPI
- Fixed switching frequency for buck and boost converter in SBC Normal mode in PWM (Pulse Width Modulation)
- PFM (Pulse Frequency Modulation) for buck converter in SBC Stop mode to reduce the quiescent current

- Automatic transition PFM to PWM in SBC Stop mode
- Soft start-up
- Edge shaping for better EMC performances for buck and boost regulator
- Undervoltage monitoring on V_{CC1} with adjustable reset level (refer to **Chapter 13.5.1**)
- Overvoltage detection on V_{CC1} (refer to **Chapter 13.5.2**)
- Buck short circuit detection
- Boost current peak detection with external shunt resistor

6.2 Functional description buck converter

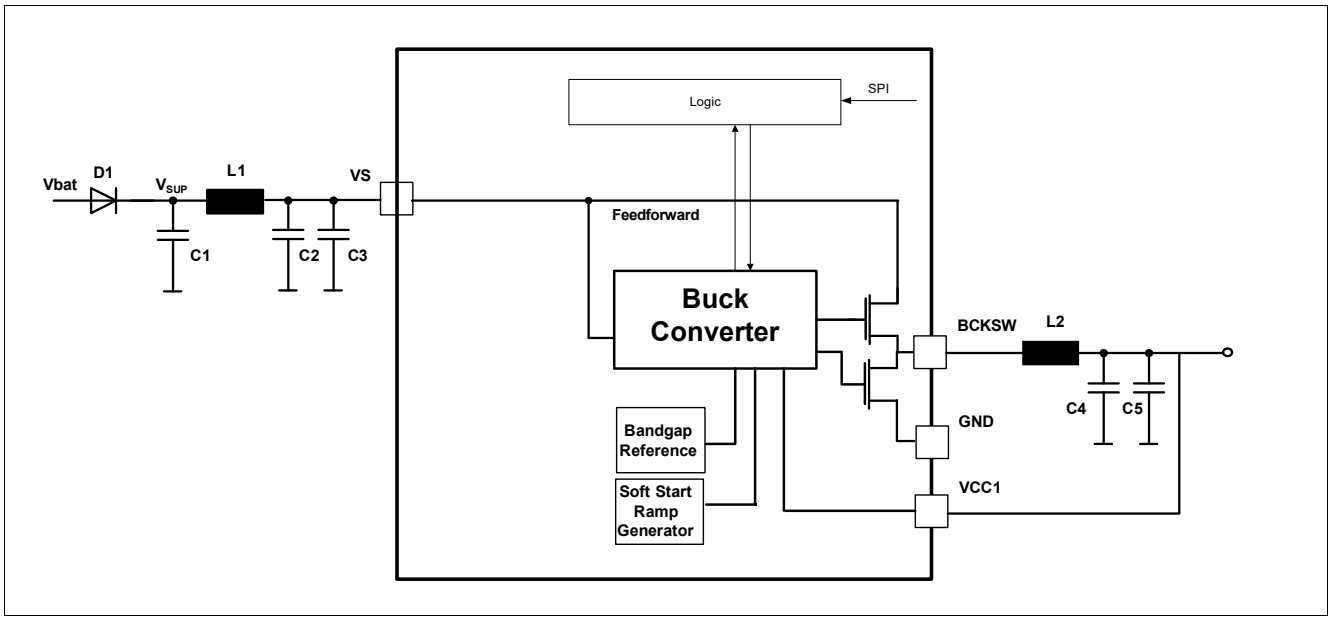

Figure 7 Buck block diagram

The DC/DC buck converter is intended as post-regulator (VCC1) and it provides a step down converter function transferring energy from VS to a lower output voltage with high efficiency (typically more than 80%). The output voltage is 3.3 V in a current range up to 750 mA. It is regulated via a digital loop with a precision of ±2%.

It requires an external inductor and capacitor filter on the output switching pin (BCKSW). The buck regulator has two integrated power switches. The compensation of the regulation loop is done internally and no additonal external components are needed.

A typical application example and external components proposal is available in **Chapter 15**.

The buck converter is active in SBC Normal, Stop and Restart mode and it is disabled in SBC Sleep and Fail-Safe mode.

Depending on the SBC mode, the buck converter works in two different modes:

- PWM mode (Pulse Width Modulation): This mode is available in SBC Normal mode, SBC Restart mode and SBC Stop mode (only for automatic or manual PFM to PWM transitions. Please refer to **Chapter 6.4.2**). In PWM, the buck converter operates with a fix switching frequency (f_{BCK}). The duty cycle is calculated internally based on input voltage, output voltage and output current. The precision is ±2% or ±3% based

on input supply and output current range (refer to **Figure 13** for more information). In PWM mode, the buck converter is capable of a 100% duty cycle in case of low VS conditions. In order to reduce EMC, edge shaping feature has been implemented to control the activation and deactivation of the two power switches

- PFM mode (Pulse Frequency Modulation): This mode is activated automatically when the SBC Stop mode is entered. The PFM mode is an asynchronous mode. PFM mode does not have a controller switching frequency. The switching frequency depends on conditions of the buck regulator such as the following: input supply voltage, output voltage, output current and external components. A typical timing diagram is shown in **Figure 8**. The buck converter in PFM mode has a tolerance of ±4%. The transition from PFM mode to PWM mode is described in **Chapter 6.4.2**

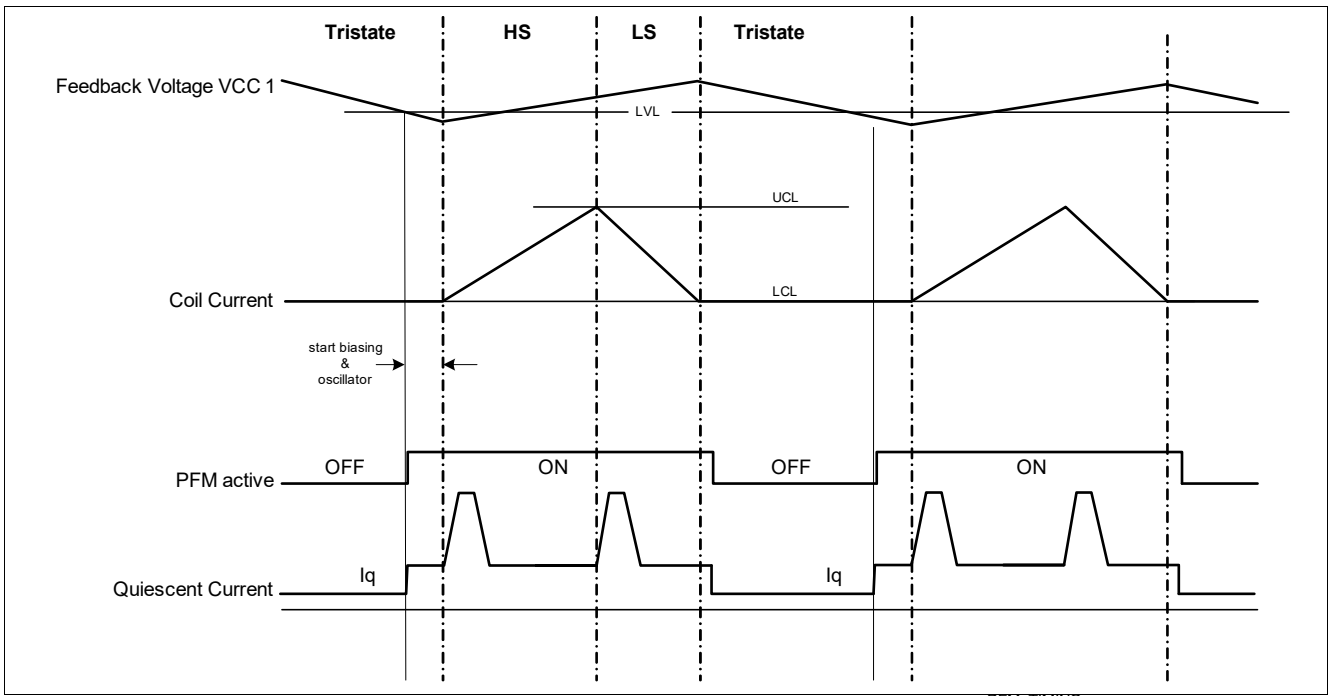

Figure 8 Typical PFM timing diagram

6.2.1 Startup procedure (soft start)

The startup procedure (soft start) permits to achieve the buck regulator output voltage avoiding large overshoot on the output voltage. This feature is activated during the power-up, from SBC Sleep to Restart mode and from SBC Fail-Safe to SBC Restart mode.

When the buck regulator is activated, it starts with a minimum duty cycle and the regulation loop maintains it for a limited number of switching periods. After this first phase, the duty cycle is increased by a fixed value and kept for a limited number of switching periods. This procedure is repeated until the target output voltage value of the buck regulator is reached. As soon as the buck regulator output voltage is reached, the regulation loop starts to operate normally using PWM mode adjusting the duty cycle according the buck input and output voltages and the buck regulator output current.

6.2.2 Buck regulator status register

The register **SMPS_STAT** contains information about the open or short conditions on BCKSW pin and if the buck regulator is outside the 12% nominal output voltage range. No SBC mode or configuration is triggered if one bit is set in the **SMPS_STAT** register.

6.2.3 External components

The buck converter needs one inductor and output capacitor filter. The inductor has a fixed value of 47 µH. Secondary parameter such as saturation current must be selected based on the maximum current capability needed in the application.

The output capacitors filter are 47 µF (typically, an electrolytic capacitor) in parallel with 10 µF (ceramic capacitor). This configuration is intended for buck regulator functionality and keeps the total ESR lower than 1 Ω in all temperature range. For additional information, refer to **Chapter 15.1**.

6.3 Functional description boost

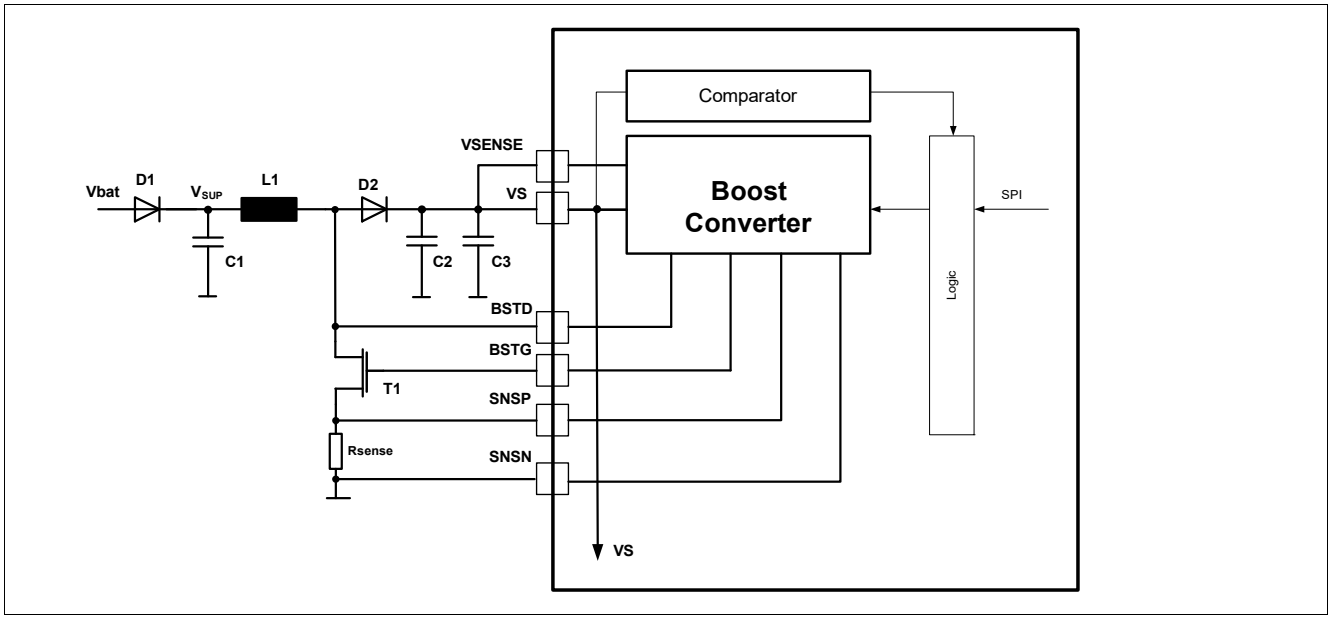

Figure 9 Boost block diagram

The boost converter is intended as pre-regulator and it provides a step up converter function. It transfers energy from an input supply VSUP (battery voltage after the reverse protection circuit) to a higher output voltage (VS) with high efficiency (typically more than 80%).

The regulator integrates the gate driver for external power switching and external passive components are necessary in particular: input buffer capacitor on the battery voltage, inductor, power switching transistor, sense resistor for overcurrent detection, freewheeling diode and filter capacitor. A typical application example is available in **Chapter 15**.

In SBC Normal mode and in SBC Stop mode, the boost regulator can be enabled via SPI (register **HW_CTRL**, bit **BOOST_EN**). The boost output voltage has to be selected using **BOOST_V** bit. The **BOOST_V** on **HW_CTRL** permits to select the minimum V_{BST1_1} or the output voltage V_{BST2_1}.

The activation thresholds vary according to the output voltage selected. **Table 9** shows the possible activation thresholds and the hysteresis including the respective SPI setting.

Table 9 Boost activation thresholds

Boost output voltage	Activation threshold	Hysteresis	SPI setting
V_{BST1_1}	$V_{BST,TH1}$	$V_{BST,HYS1}$	**BOOST_V** = 1
V_{BST2_1}	$V_{BST,TH2}$	$V_{BST,HYS2}$	**BOOST_V** = 0

If the boost regulator is enabled, it switches ON automatically when VSENSE falls below the threshold voltage $V_{BST,TH1}$ or $V_{BST,TH2}$ and switches OFF when crossing the threshold plus respective hysteresis. The bit **BST_ACT** is set and can be cleared only if VSENSE is above the $V_{BST,TH1}$ or $V_{BST,TH2}$.

Figure 10 shows the typical timing for enabling the boost converter.

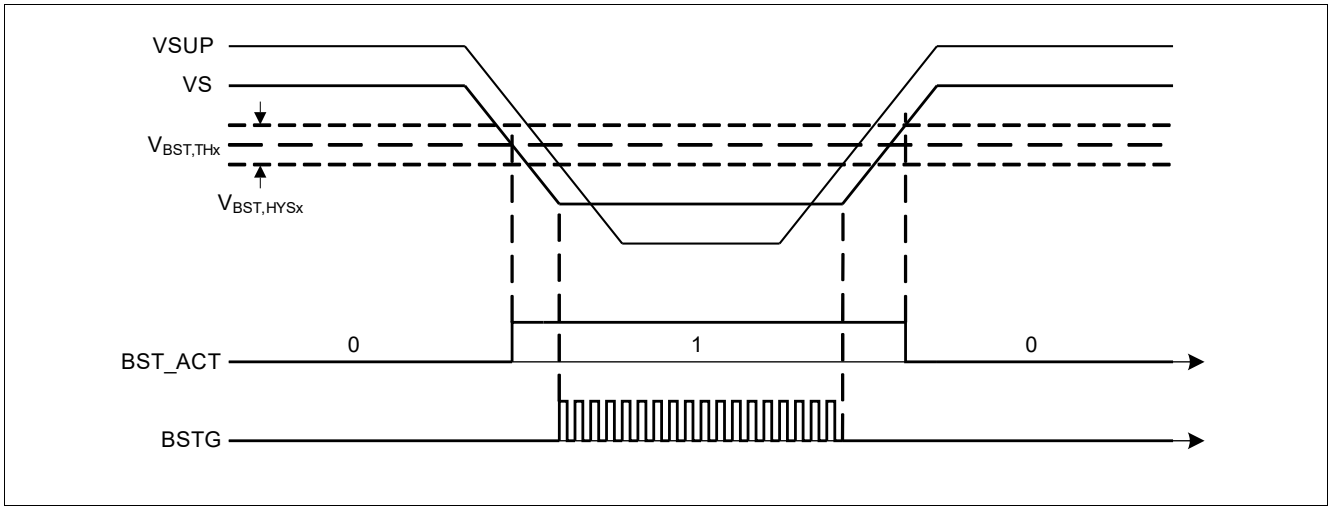

Figure 10 Boost converter activation

The boost regulator works in PWM mode with a fixed frequency (**f_{BST}**) and a tolerance of ±5%.

If the boost is enabled in SBC Stop mode, the SBC quiescent current is increased.

6.3.1 Boost regulator status register

The register **SMPS_STAT** contains information about the open or short conditions on boost pin's including loss of GND detection. No SBC mode or configuration is triggered if one bit is set on **SMPS_STAT** register.

6.3.2 External components

The boost converter requires a number of external components such as the following: input buffer capacitor on the battery voltage, inductor, power switching transistor, sense resistor for overcurrent detection, freewheeling diode and filter capacitors.

For recommend devices and values, refer to **Chapter 15.1**.

The recommended inductor value is 22 µH. The secondary parameters (e.g. saturation current) have to be selected according to the maximum current capability required by the application.

The characterization is performed with the suggested external power MOSFET Infineon BSS606N. Other MOSFETs can be used. However, the functionality has to be checked in the application considering the gate driver current capability (**Chapter 6.3.3** and **Chapter 6.3.4**) and maximum output current requirements.

6.3.2.1 Peak overcurrent detection

The boost converter implement one peak overcurrent detection using one external shunt resistor. For typical application, refer to **Chapter 15.1**.

As soon as the boost converter detects one peak overcurrent, the regulation loop reduces the duty cycle in order to reduce the peak current on the external MOSFET.

The shunt resistor can be calculated based on **$V_{TH,SNS}$** and using **Equation (6.1)**.

$$R_{SENSE} = \frac{V_{TH,SNS}}{I_{OC,peak}} \tag{6.1}$$

Example: for an overcurrent peak detection of 2.1 A, the resistor is typically 0.1 Ω.

6.3.3 Boost switch gate driver

The gate driver for the external boost switch is implemented with several phases with different characteristics.

Charging: Phases PH1 and PH2 uses a current source to charge the gate in a controlled way. The following phases PH3 and PH4 involve a pull up resistor to an internal 5 V supply to bring the gate voltage to the final value and keep it there during the whole ON-phase of the PWM cycle.

Discharging: Phases PH5 and PH6 uses current sources to discharge the gate in a controlled way. The following phases PH7 and PH0 involve a pull down resistor to GND.

The current sources are optimized for operation with the MOSFET BSS606N.

Due to the phases which involve the pull up/down resistors it is possible to use also MOSFETs with higher gate charge compared to BSS606N. The MOSFET selection is limited by the short circuit detection feature described in **Chapter 6.3.4**.

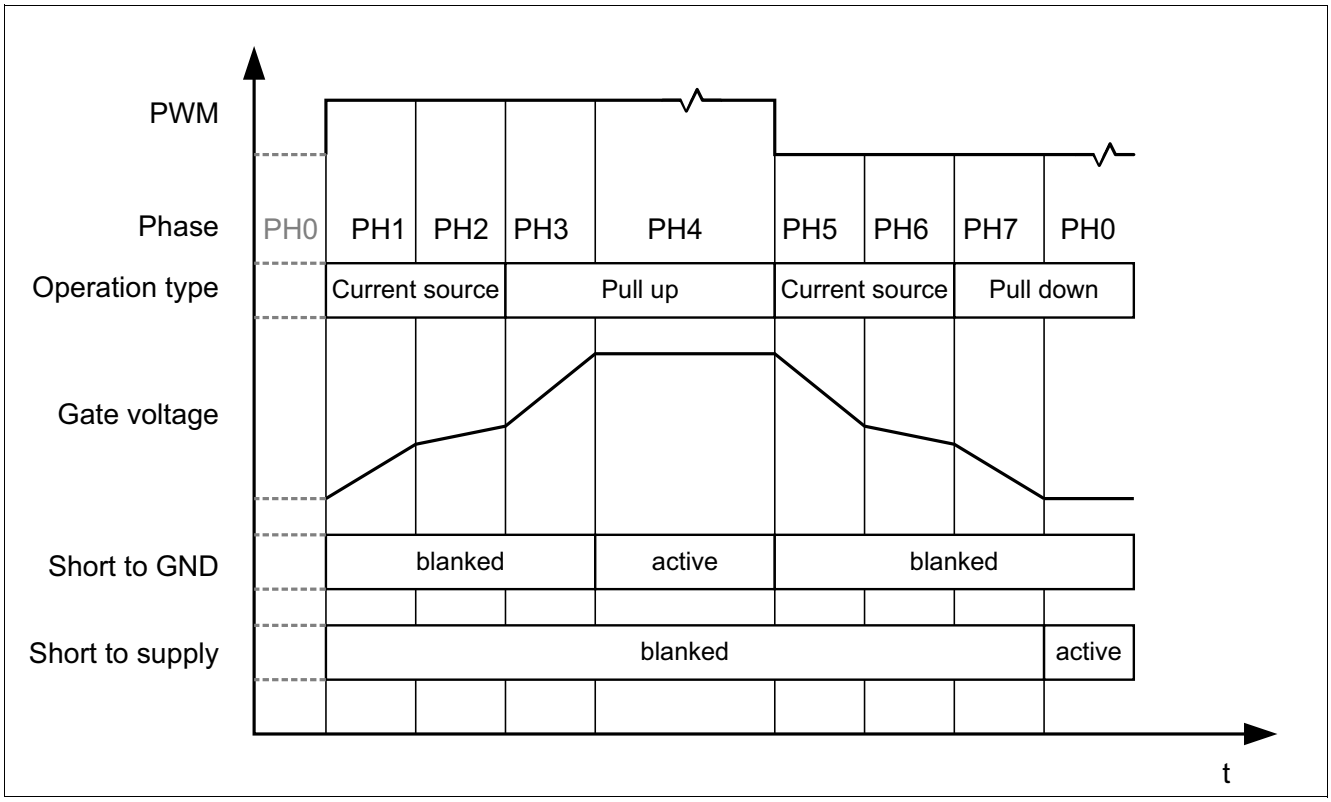

Figure 11 Phases of the boost switch gate driver

6.3.4 BSTG short circuit detection

If the gate driver is not able to charge / discharge the gate connected to pin BSTG within a certain time, a short at this pin is assumed and the driver is switched off for the current PWM cycle to protect the chip from damage.

For detecting short to GND (during PWM on) or short to supply (during PWM off) the following voltage threshold is used:

- Criteria for short to GND during PH4: $V_{BSTG} < V_{BSTG,sc}$
- Criteria for short to supply during PH0: $V_{BSTG} > V_{BSTG,sc}$

The short detection feature is blanked during the charging in PH1, PH2, PH3 and during discharging in phases PH5, PH6, PH7.

When a short is detected also the bit BST_GSH in the status register **SMPS_STAT** is set.

6.4 Power scenarios

The chapter describes the features and performance of the buck and boost regulators according to SBC mode.

6.4.1 Buck and boost in SBC Normal mode

In SBC Normal mode, the buck regulator operates in PWM mode with fixed switching frequency. The microcontroller and other loads on the ECU are typically supplied with a 3.3V output voltage. All supervision functions for buck regulator are available in SBC Normal mode (for more details, refer to **Chapter 13.5.1**, **Chapter 13.5.2**, **Chapter 13.5.3** and **Chapter 13.8**).

6.4.2 Buck and boost in SBC Stop mode operation

The SBC Stop mode operation is intended to reduce the total amount of quiescent current while still providing supply for microcontroller. In order to achieve this, the buck regulator automatically changes the modulation from PWM (Pulse Width Modulation) to PFM (Pulse Frequency Modulation) when entering SBC Stop mode. In case the boost regulator in SBC Stop mode is enabled and running, it operates only in PWM mode.

6.4.2.1 Automatic transition from PFM to PWM in SBC Stop mode

In SBC Stop mode, the buck converter operates in PFM mode by default to reduce current consumption. If more current is needed, an automatic transition from PFM to PWM modulation is implemented. When the buck regulator output current exceeds the $I_{PFM-PWM,TH}$ threshold, the buck module changes the modulation to PWM and an INT event is generated. In addition, the **PFM_PWM** bit on **WK_STAT_1** is set.

In order to set the buck modulation again in PFM, it is necessary to write a Stop mode command to **M_S_CTRL** register. This command has to be sent when the required buck output current is below the $I_{PFM-PWM,TH}$ threshold.

When entering SBC Stop mode, the automatic transition from PFM to PWM mode is activated after the time t_{lag}, which is the transition time where the buck regulator loop changes the modulation technique. Two possible values can be configured via SPI command.

The **Figure 12** shows the timing transition from SBC Normal to SBC Stop mode.

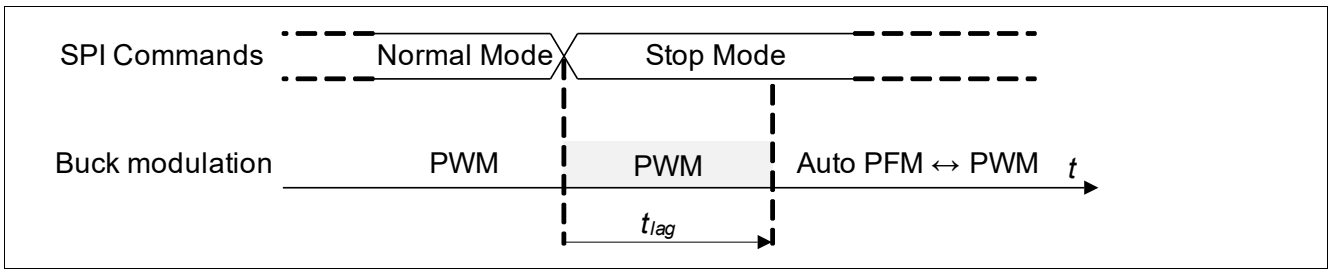

Figure 12 Transition from SBC Normal to SBC Stop mode

The t_{lag} is always present in case of PWM to PFM transition.

The automatic transition can be disabled by setting the bit **PWM_AUTO** to 0 in the **HW_CTRL** register.

6.4.2.2 Manual transition from PFM to PWM in SBC Stop mode

The PFM to PWM transition can also be controlled by the microcontroller or an external signal, directly by using the WK pin as a trigger signal if an additional current is required in SBC Stop mode.

When the **PWM_BY_ WK** bit is set to 1, the DC/DC regulator can be switched from PFM to PWM using the WK pin.

A LOW level at the WK pin will switch the buck converter to PFM mode, a HIGH level will switch it to PWM mode. In this configuration, the filter time is not taken into account because a defined signal from µC or external source is expected.

If the **PWM_BY_ WK** bit is set to 0, the PFM modulation is used.

6.4.2.3 SBC Stop to Normal mode transition

The microcontroller sends an SPI command to switch from SBC Stop mode to SBC Normal mode. In this transition, the buck regulator changes the modulation from PFM to PWM.

Once the SPI command for the SBC Normal mode transition is received the current is able to rise above the specified maximum Stop mode current ($I_{PFM-PWM,TH}$).

If the transition from SBC Stop mode to SBC Normal mode is carried out when the boost is enabled and operating, it will continue to operate without any changes.

6.4.3 Buck and boost in SBC Sleep and Fail-Safe mode

In SBC Sleep or Fail-Safe mode, the buck and boost converter are off and not operating. The lowest quiescent current is achievable.

6.4.3.1 SBC Sleep/Fail-Safe mode to Normal mode transition

In case of a wake-up event from WK pin or transceivers, the SBC will be set SBC Restart mode and as soon as the reset is released, into SBC Normal mode.

In SBC Restart mode, the buck regulator is activated and ramping. The boost regulator is activated and ramping again (in case the VS is below the selected threshold) in according the configuration selected in SBC Normal mode. As soon as the buck output voltage exceeds the reset threshold, the RO pin is released.

6.5 Electrical characteristics

Table 10 Electrical characteristics

T_j = -40°C to +150°C; V_S = 5.5 V to 28 V; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Buck regulator							
Output voltage SBC Normal mode	$V_{CC1,out1}$	3.23	3.3	3.36	V	Normal mode (PWM) 1 mA < I_{VCC1} < 750 mA 6.3 V < V_S < 28 V	P_6.5.12
Output voltage SBC Normal mode	$V_{CC1,out2}$	3.23	3.3	3.36	V	1) Normal mode (PWM) I_{VCC1} = 400 mA V_S = 4 V Boost disabled	P_6.5.24
Output voltage SBC Stop mode	$V_{CC1,out3}$	3.16	3.3	3.43	V	Stop mode (PFM) 1 mA < I_{VCC1} < $I_{PFM-PWM,TH}$ 6.3 V < V_S < 18 V	P_6.5.13
Output voltage SBC Stop mode	$V_{CC1,out4}$	3.18	3.3	3.39	V	Stop mode (PFM) 1 mA < I_{VCC1} < 50 mA 6.3 V < V_S < 18 V	P_6.5.41
Power Stage on-resistance High-Side	$R_{DSON1,HS}$	–	–	1.3	Ω	V_S = 6.5 V I_{VS}= 100 mA	P_6.5.3
Power Stage on-resistance Low-Side	$R_{DSON1,LS}$	–	–	1.3	Ω	I_{BCKSW}= 100 mA	P_6.5.20
Buck switching frequency	f_{BCK}	405	450	495	kHz	Normal mode (PWM)	P_6.5.5
Threshold automatic transition PFM to PWM	$I_{PFM-PWM,TH}$	80	110	150	mA	2) Stop mode 6.3 V < V_S < 18 V	P_6.5.14
Transition time from PWM to PFM	t_{lag}	–	1	–	ms	2) **PWM_TLAG**=1 (on **HW_CTRL**)	P_6.5.15
Transition time from PWM to PFM	t_{lag}	–	100	–	µs	2) **PWM_TLAG**=0 (on **HW_CTRL**)	P_6.5.16
Peak current limit of internal high-side switch	I_{BCK_LIM}	0.85	1.05	1.2	A	V_S = 13.5 V	P_6.5.4
Boost regulator							
Boost voltage 1	V_{BST1_1}	6.32	6.65	6.88	V	3) SBC Normal mode V_{SUP} = 3 V I_{VS} = 550 mA Boost enabled **BOOST_V** = 1	P_6.5.11

Table 10 Electrical characteristics (cont'd)

T_j = -40°C to +150°C; V_S = 5.5 V to 28 V; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Boost voltage 2	V_{BST2_1}	7.6	8	8.4	V	[3] SBC Normal mode V_{SUP} = 3 V I_{VS} = 450 mA Boost enabled **BOOST_V** = 0	P_6.5.6
Boost switch ON/OFF voltage 1 threshold	$V_{BST,TH1}$	6.35	7	7.5	V	Boost enabled V_S falling **BOOST_V** = 1	P_6.5.7
Boost switch ON/OFF hysteresis 1	$V_{BST,HYS1}$	300	500	600	mV	Boost enabled **BOOST_V** = 1	P_6.5.8
Boost switch ON/OFF voltage 2 threshold	$V_{BST,TH2}$	9.5	10	10.5	V	Boost enabled V_S falling; **BOOST_V** = 0	P_6.5.32
Boost switch ON/OFF hysteresis 2	$V_{BST,HYS2}$	0.9	1	1.2	V	Boost enabled; **BOOST_V** = 0	P_6.5.33
BSTG rise switching time	$t_{BSTG,rise}$	–	30	–	ns	[2] V_{SUP} > 3 V 20% - 80% C_{BSTG} = 470 pF	P_6.5.28
BSTG fall switching time	$t_{BSTG,fall}$	–	30	–	ns	[2] V_{SUP} > 3 V 20% - 80% C_{BSTG} = 470 pF	P_6.5.29
Overcurrent shunt voltage threshold	$V_{TH,SNS}$	199	210	221	mV	Boost enable V_{SUP} > 3 V	P_6.5.21
Boost switching frequency	f_{BST}	405	450	495	kHz	Normal mode (PWM)	P_6.5.10
Boost switch gate driver							
Duration of PH1	t_{PH1}	–	37.5	–	ns	[2]	P_6.5.17
Duration of PH2	t_{PH2}	–	25	–	ns	[2]	P_6.5.18
Duration of PH3	t_{PH3}	124	131	–	ns	[2]	P_6.5.19
Duration of PH5	t_{PH5}	–	62.5	–	ns	[2]	P_6.5.22
Duration of PH6	t_{PH6}	–	25	–	ns	[2]	P_6.5.25
Duration of PH7	t_{PH7}	29	31	–	ns	[2]	P_6.5.26
Current during PH1	I_{PH1}	–	-27	–	mA	[2]	P_6.5.31
Current during PH2	I_{PH2}	–	-7	–	mA	[2]	P_6.5.42
Pull up resistance during PH3	R_{PH3}	–	–	25	Ω	[4] to internal gate driver supply; V_{BSTG} = 4 V	P_6.5.34
Internal gate driver supply	V_{drv_sup}	4.75	5.0	–	V	no load;	P_6.5.35

Table 10 Electrical characteristics (cont'd)

T_j = -40°C to +150°C; V_S = 5.5 V to 28 V; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current during PH5	I_{PH5}	–	23	–	mA	2)	P_6.5.36
Current during PH6	I_{PH6}	–	15	–	mA	2)	P_6.5.37
Pull down resistance during PH7	R_{PH7}	–	–	15	Ω	–	P_6.5.38
BSTG short circuit detection threshold	$V_{BSTG,sc}$	3.23	3.4	3.57	V	–	P_6.5.39

1) Typical maximum current capability is given in **Figure 13**. The external components are in accordance with the application information (refer to **Chapter 15**).
2) Not subject to production test; specified by design.
3) Values verified in characterization with boost converter specified in **Chapter 15.1**. Not subject to production test; specified by design. Refer to **Figure 14** for additional information.
4) Calculated value based on other measurements.

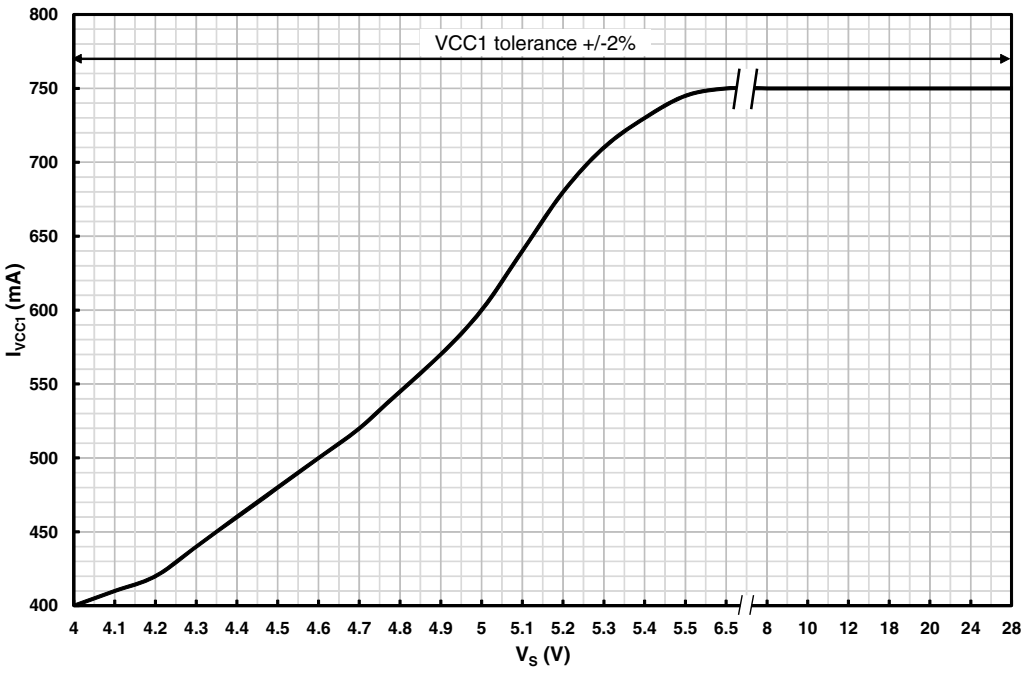

Figure 13 Maximum DCDC buck current capability versus VS.

*Note: The **Figure 13** is based on characterization results over temperature with external components specified in **Chapter 15.1**.*

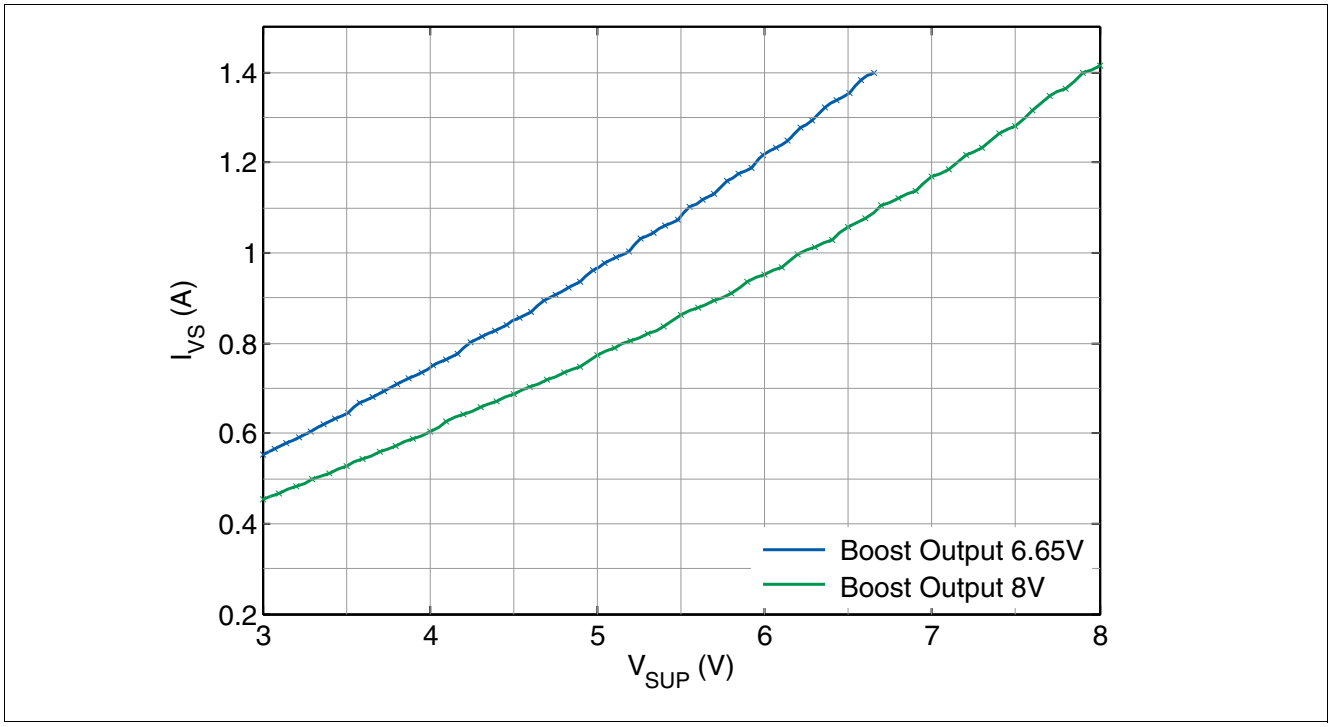

Figure 14 Maximum DCDC boost current capability versus VSUP.

*Note: **Figure 14** is based on simulation results (specified by design), with boost converter external components specified in **Chapter 15.1**.*

7 Voltage regulator 2

7.1 Block description

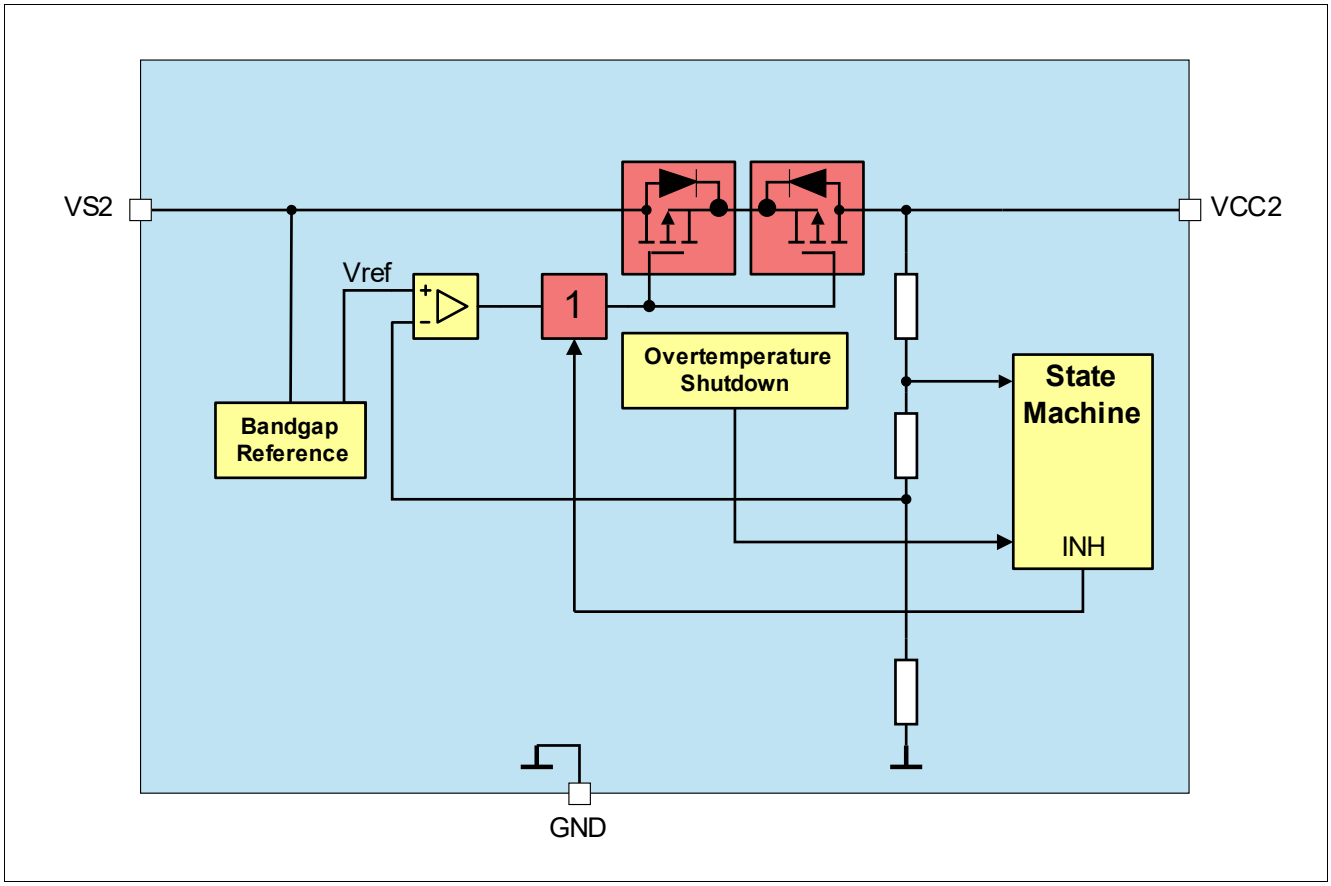

Figure 15 Module block diagram

Functional features

- 5 V low-drop voltage regulator
- Protected against short to supply voltage, e.g. for off-board sensor supply
- Can also be used for CAN supply
- VCC2 undervoltage monitoring. Please refer to **Chapter 13.6** for more information
- Can be active in SBC Normal, SBC Stop, and SBC Sleep mode (not SBC Fail-Safe mode)
- VCC2 switch off after entering SBC Restart mode. Switch off is latched, LDO must be enabled via SPI after shutdown
- Overtemperature protection
- ≥ 470 nF ceramic capacitor at output voltage for stability, with ESR < 1 Ω at f = 10 kHz, to achieve the voltage regulator control loop stability based on the safe phase margin (bode diagram)
- Output current capability up to $I_{VCC2,lim}$

7.2 Functional description

In SBC Normal mode, VCC2 can be switched on or off via SPI.

For SBC Stop mode or Sleep mode, the VCC2 has to be switched on or off before entering the respective SBC mode.

The output current of VCC2 is limited at $I_{VCC2,lim}$.

The VS2 pin is the dedicated supply pin for VCC2. VS2 can be connected to VS and therefore to the boost output, or directly from battery after the reverse protection input diode.

For low-quiescent current, the output voltage tolerance is decreased in SBC Stop mode because only a low-power mode regulator (with lower accuracy $V_{CC2,out5}$) will be active for small loads. If the load current on VCC2 increases (typ. more than 1.5 mA), then the high-power mode regulator will also be enabled to support an optimum dynamic load behavior. When both power mode regulators are active, the VCC2 quiescent current will the typical increase by 2.9 mA.

If the load current on VCC2 decreases (typically below 1.3 mA), then the low-quiescent current mode is resumed again disabling the high-power mode regulator.

Both regulators are active in SBC Normal mode.

Note: If the VCC2 output voltage is supplying external off-board loads, the application must consider the series resonance circuit built by cable inductance and decoupling capacitor at load. Sufficient damping must be provided.

7.3 Electrical characteristics

Table 11 Electrical characteristics

T_j = -40°C to +150°C; V_{S2} = 5.5 V to 28 V; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output voltage including line and load regulation	$V_{CC2,out1}$	4.9	5.0	5.1	V	1) SBC Normal mode 10 µA < I_{VCC2} < 100 mA 6.5 V < V_{S2} < 28 V	P_7.3.1
Output voltage including line and load regulation	$V_{CC2,out2}$	4.9	5.0	5.1	V	1) SBC Normal mode 10 µA < I_{VCC2} < 80 mA 6 V < V_{S2} < 28 V	P_7.3.2
Output voltage including line and load regulation	$V_{CC2,out3}$	4.85	5.0	5.15	V	1) 10 µA < I_{VCC2} < 60 mA SBC Normal mode	P_7.3.19
Output voltage including line and load regulation	$V_{CC2,out4}$	4.97	–	5.07	V	2) SBC Normal mode 8 V < V_{S2} < 18 V 10 µA < I_{VCC2} < 5 mA 25°C< T_j <125°C	P_7.3.18
Output voltage including line and load regulation	$V_{CC2,out5}$	4.9	5.05	5.2	V	SBC Stop, Sleep mode 1 mA < I_{VCC2} < 3 mA	P_7.3.3
Output voltage including line and load regulation	$V_{CC2,out6}$	4.9	5.05	5.25	V	SBC Stop, Sleep mode 10 µA < I_{VCC2} < 1 mA	P_7.3.20
Output drop	$V_{CC2,d1}$	–	–	500	mV	I_{VCC2} = 30 mA V_{S2} = 5 V	P_7.3.4
Overcurrent limitation	$I_{VCC2,lim}$	100	–	750 2)	mA	current flowing out of pin V_{CC2} = 0 V V_{S2} = 13.5 V	P_7.3.5

1) In SBC Stop mode, the specified output voltage tolerance applies from I_{CC2} > 3 mA but with increased current consumption.

2) Not subject to production test, specified by design.

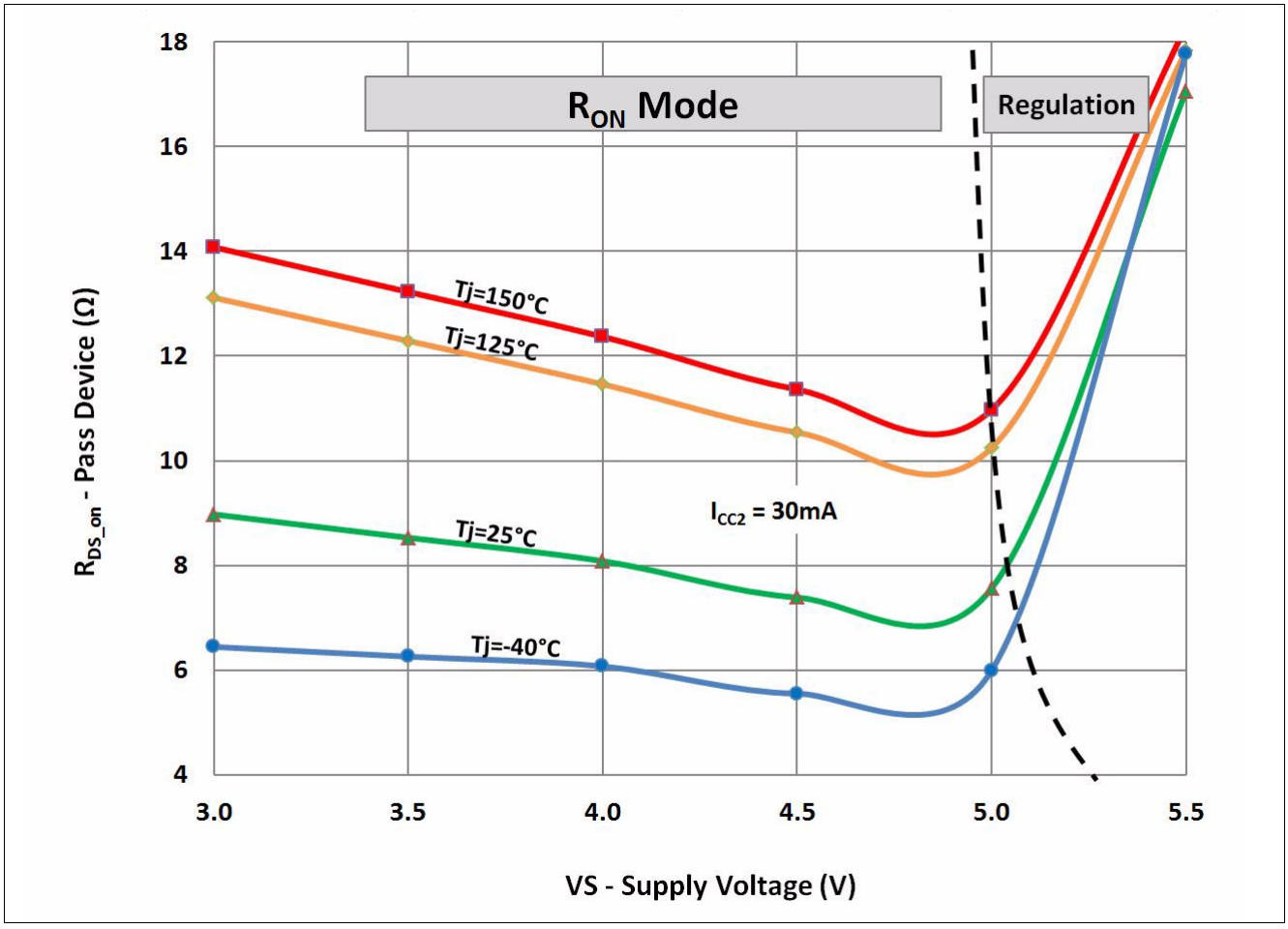

Figure 16 VCC2 pass device on-resistance during low drop operation for I_{CC2} = 30 mA

8 High-speed CAN transceiver

8.1 Block description

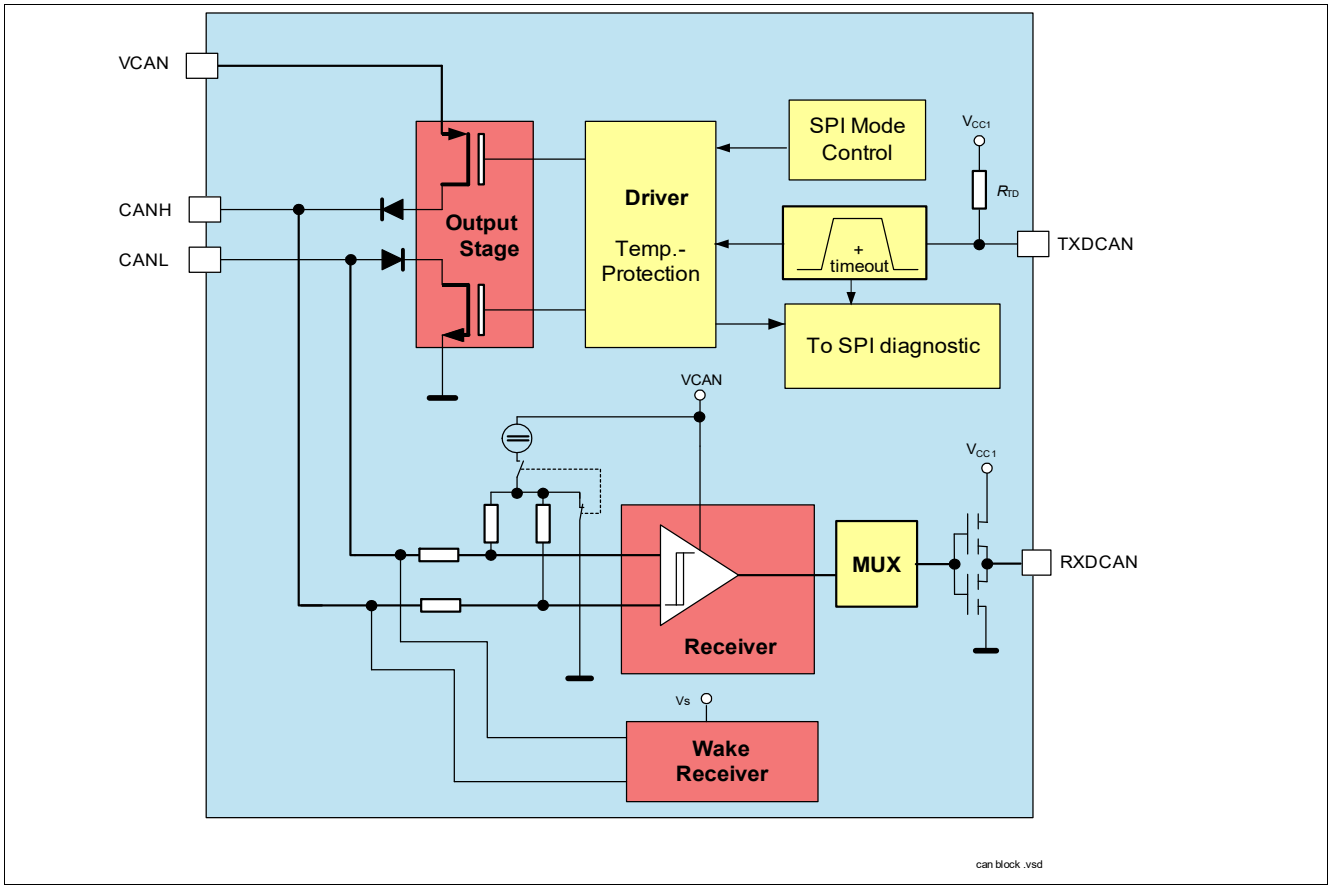

Figure 17 Functional block diagram

8.2 Functional description

The Controller Area Network (CAN) transceiver part of the SBC provides high-speed (HS) differential mode data transmission (up to 5 Mbaud) and reception in automotive and industrial applications. It works as an interface between the CAN protocol controller and the physical bus lines compatible with ISO 11898-2: 2016 as well as SAE J2284.

The CAN transceiver offers low power modes to reduce current consumption. This supports networks with partially powered down nodes. To support software diagnostic functions, a CAN Receive-Only mode is implemented.

It is designed to provide excellent passive behavior when the transceiver is switched off (mixed networks, clamp 15/30 applications).

A wake-up from the CAN Wake-Capable mode is possible via a message on the bus. Thus, the microcontroller can be powered down or idled and will be woken up by the CAN bus activities.

The CAN transceiver is designed to withstand the severe conditions of automotive applications and to support 12 V applications.

The transceiver can also be configured as wake-capable in order to save power and to ensure a safe transition from SBC Normal to Sleep mode (to avoid losing messages).

Figure 18 shows the possible transceiver mode transition when changing the SBC mode.

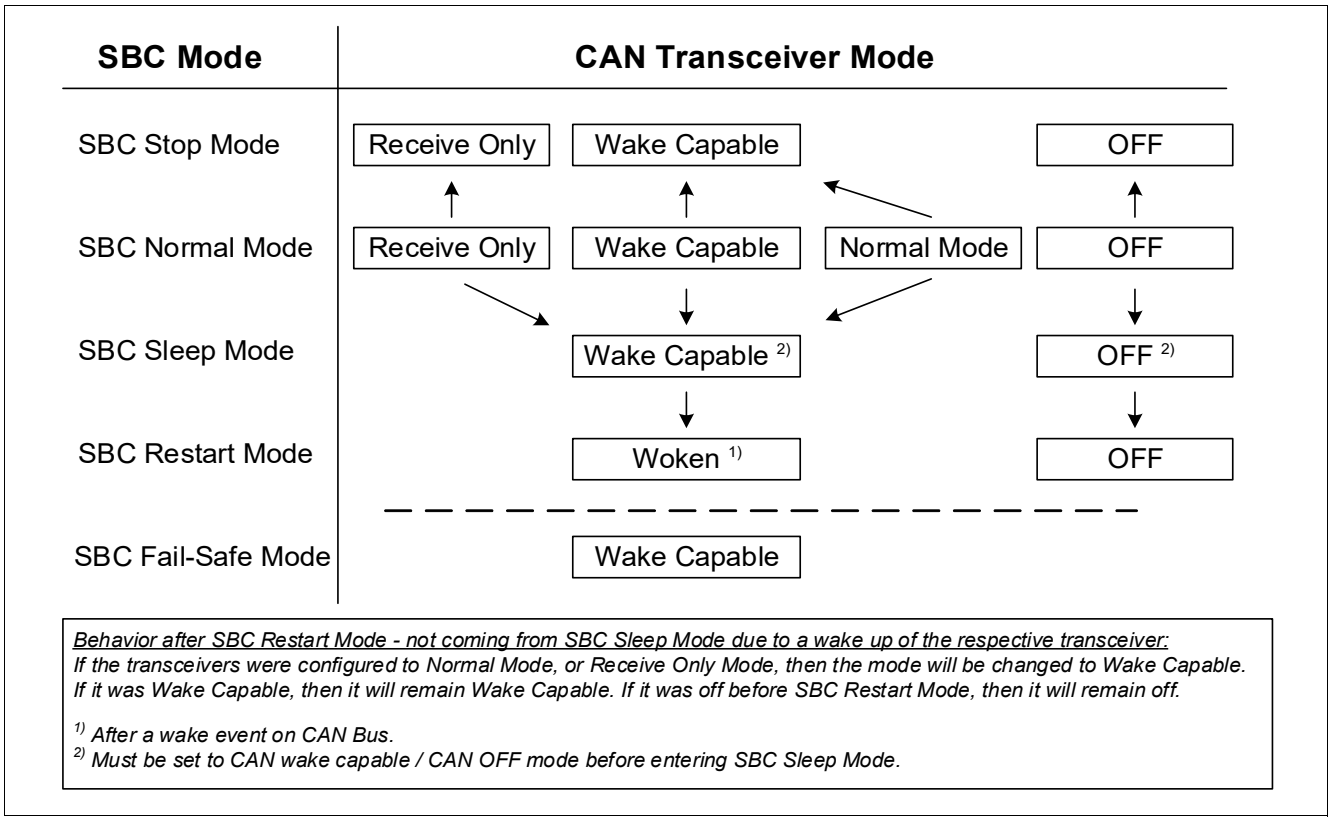

Figure 18 CAN mode control diagram

CAN FD support

CAN FD stands for 'CAN with Flexible Data Rate'. It is based on the well established CAN protocol as specified in ISO 11898-1. CAN FD still uses the CAN bus arbitration method. The benefit is that the bit rate can be increased by switching to a shorter bit time at the end of the arbitration process and then returning to the longer bit time at the CRC delimiter before the receivers transmit their acknowledge bits. See also **Figure 19**. In addition, the effective data rate is increased by allowing longer data fields. CAN FD allows the transmission of up to 64 data bytes compared to the 8 data bytes from the standard CAN.

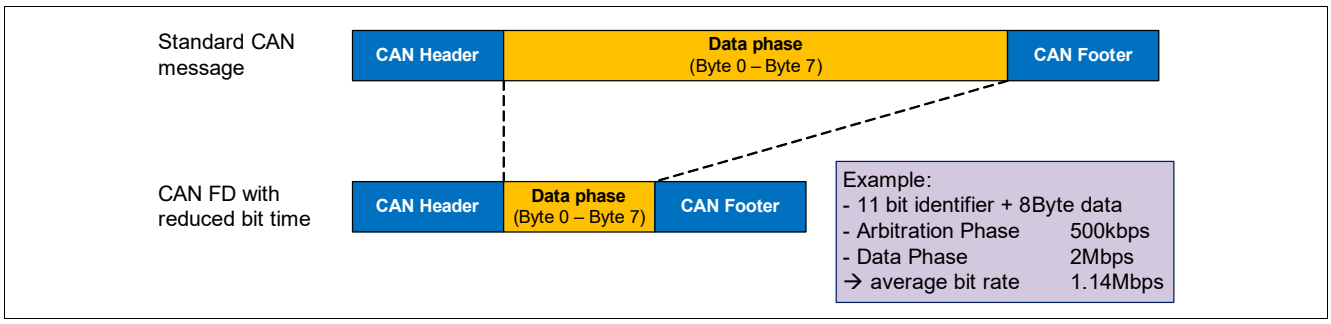

Figure 19 Bite rate increase with CAN FD vs. standard CAN

CAN FD has to be supported by both physical layer and the CAN controller. If the CAN controller cannot support CAN FD, then the respective CAN node must at least tolerate CAN FD communication. This CAN FD tolerant mode is implemented in the physical layer.

8.2.1 CAN OFF mode

The CAN OFF mode is the default mode after the SBC has powered up. It is available in all SBC modes and is used to completely stop CAN activities or when CAN communication is not needed. In CAN OFF mode, a wake-up event on the bus will be ignored.

8.2.2 CAN Normal mode

The CAN transceiver is enabled via SPI. CAN Normal mode is designed for normal data transmission/reception within the HS CAN network. This mode is available in SBC Normal mode.

Transmission

The signal from the microcontroller is applied to the TXDCAN input of the SBC. The bus driver switches the CANH/L output stages to transfer this input signal to the CAN bus lines.

Enabling sequence

The CAN transceiver requires an enabling time $t_{CAN,EN}$ before a message can be sent on the bus. This means that the TXDCAN signal can only be pulled LOW after the enabling time. If this is not ensured, then the TXDCAN needs to be set back to HIGH (= recessive) until the enabling time is over. Only the next dominant bit will be transmitted on the bus. **Figure 20** shows different scenarios and explanations for CAN enabling.

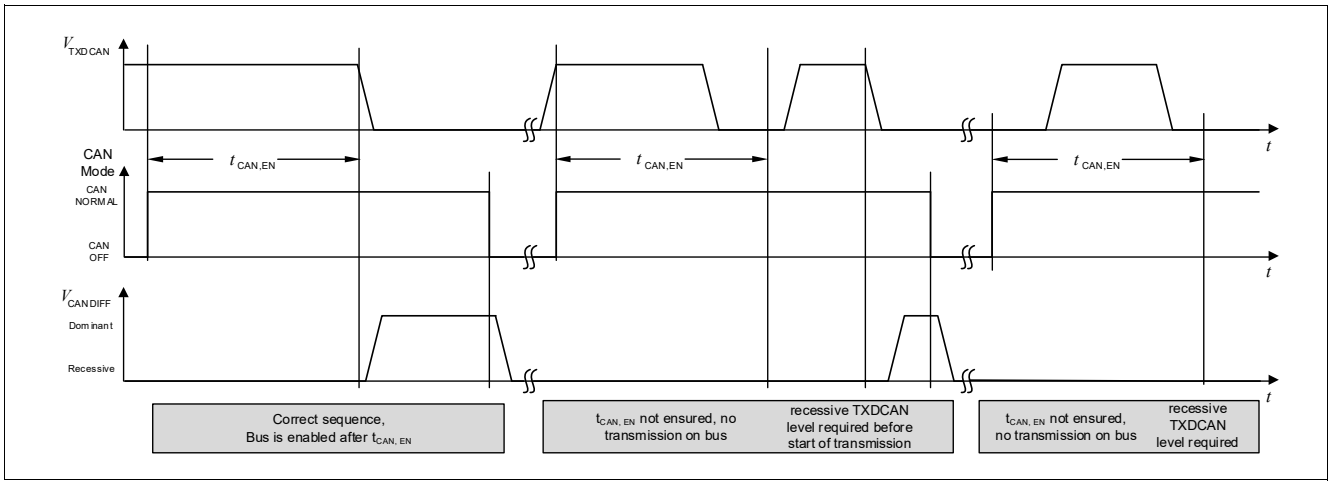

Figure 20 CAN transceiver enabling sequence

Reduced electromagnetic emission

To reduce electromagnetic emissions (EME), the bus driver controls CANH/L slopes symmetrically.

Reception

Analog CAN bus signals are converted into digital signals at RXDCAN via the differential input receiver.

8.2.3 CAN Receive-Only mode

In CAN Receive-Only mode (RX only), the driver stage is disabled but reception is still operational. This mode is accessible by an SPI command in SBC Normal mode and in SBC Stop mode.

Note: The transceiver is still working properly in Receive-Only mode even if VCAN is not available because of an independent receiver supply.

8.2.4 CAN Wake-capable mode (wake-up pattern)

This mode can be used in SBC Stop, Sleep, Restart and Normal mode by programming via SPI and it is used to monitor bus activities. It is automatically accessed in SBC Fail-Safe mode. A wake-up pattern on the bus results in a change of behavior of the SBC, as described in **Table 12**. As a signal to the microcontroller, the RXDCAN pin is set to low and will stay low until the CAN transceiver changes to a different mode. After a wake-up pattern event, the transceiver can be switched to CAN Normal mode via SPI for bus communication.

As shown in **Figure 21**, a wake-up pattern is signaled on the bus by two consecutive dominant bus levels for at least t_{Wake1} (filter time t > t_{Wake1}) and less than t_{Wake2}, each separated by a recessive bus level greater than t_{Wake1} and shorter than t_{Wake2}.

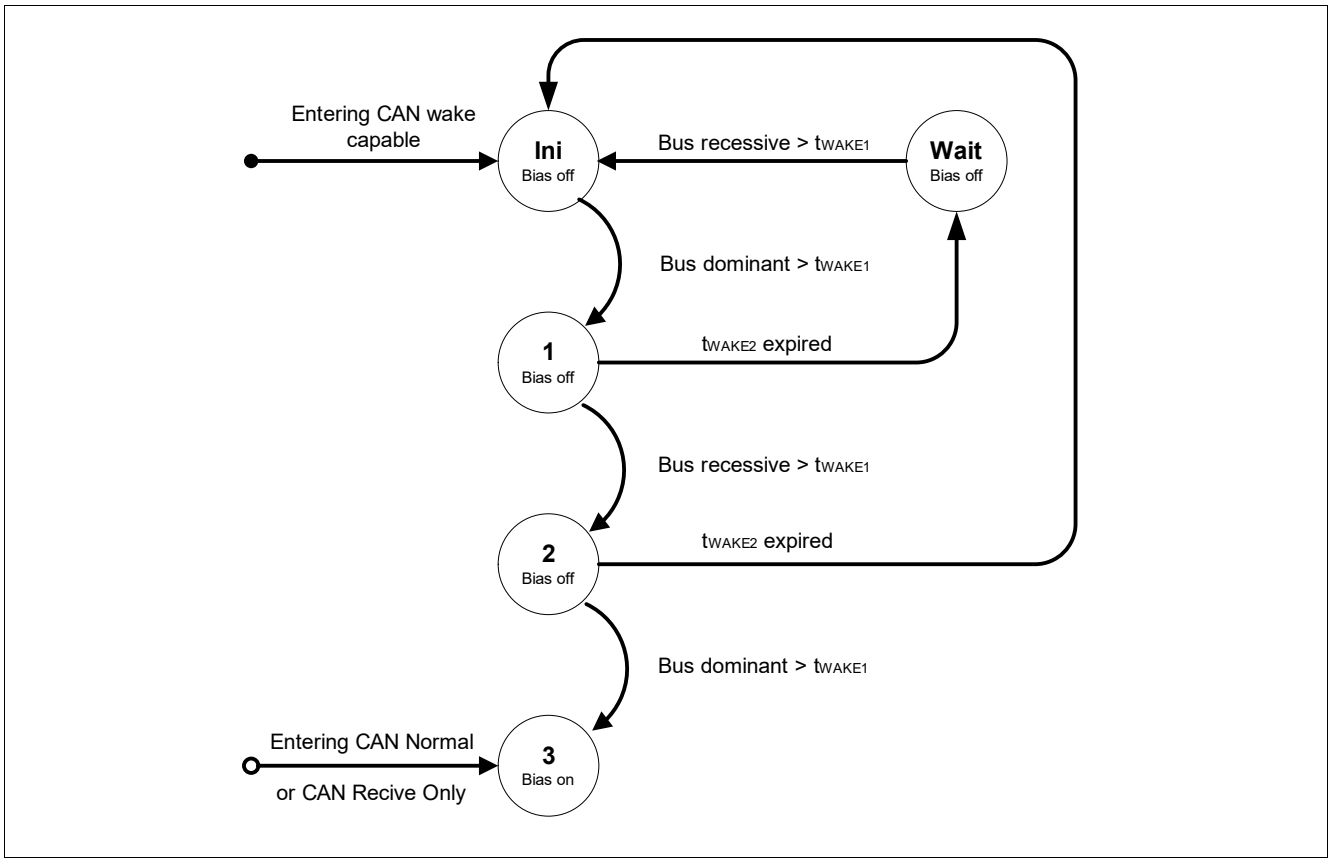

Figure 21 CAN wake-up pattern detection (WUP) according to the definition in ISO 11898-5

Rearming the transceiver for wake capability

After a BUS wake-up pattern event, the transceiver is woken. However, the **CAN** transceiver mode bits will still show wake capable (=‘01’) so the RXDCAN signal will be pulled LOW. There are two possibilities for enabling the CAN transceiver’s wake capable mode again after a wake-up event:

- The CAN transceiver mode must be toggled, i.e. switched from Wake-Capable mode to CAN Normal mode, CAN Receive-Only mode or CAN Off, before switching to CAN Wake-Capable mode again
- Rearming occurs automatically when the SBC changes to SBC Stop, or SBC Fail-Safe mode to ensure wake-up capability
- If the SBC is in SBC Stop mode, the CAN is rearmed automatically if the SBC is set again in SBC Stop mode
- CAN must be set to CAN Wake-Capable or CAN OFF mode before entering SBC Sleep mode

Notes

1. *It is necessary to clear the CAN wake-up bit **CAN_WU** to become wake capable again. It is sufficient to toggle the CAN mode.*
2. *The CAN module is supplied by an internal voltage when in CAN Wake-Capable mode, i.e. the module must not be supplied through the VCAN pin during this time. Before changing the CAN mode to Normal mode, the supply of VCAN has to be activated first.*

Wake-up in SBC Stop and Normal mode

In SBC Stop mode, if a wake-up pattern is detected, it is always signaled by the INT output and in the **WK_STAT_1** SPI register. It is also signaled by RXDCAN pulled to LOW. The same applies for the SBC Normal mode. The microcontroller should set the device from SBC Stop mode to SBC Normal mode; there is no automatic transition to Normal mode.

For functional safety reasons, the watchdog will be automatically enabled in SBC Stop mode after a bus wake-up event in case it was disabled before (if bit **WD_EN_WK_BUS** was configured to HIGH before).

Wake-up in SBC Sleep mode

Wake-up is possible via a CAN message. The wake-up pattern automatically transfers the SBC into the SBC Restart mode and from there to Normal mode the corresponding RXDCAN pin is set to LOW. The microcontroller is able to detect the LOW signal on RXDCAN and to read the wake source out of the **WK_STAT_1** register via SPI. No interrupt is generated when coming out of Sleep mode. The microcontroller can now, for example, switch the CAN transceiver into CAN Normal mode via SPI to start communication.

Table 12 Action due to CAN bus wake-Up

SBC mode	SBC mode after wake	VCC1	INT	RXDCAN
Normal mode	Normal mode	ON	LOW	LOW
Stop mode	Stop mode	ON	LOW	LOW
Sleep mode	Restart mode	Ramping up	HIGH	LOW
Restart mode	Restart mode	ON	HIGH	LOW
Fail-Safe mode	Restart mode	Ramping up	HIGH	LOW

8.2.5 TXDCAN time-out feature

If the TXDCAN signal is dominant for a time $t > t_{TXDCAN\_TO}$, in CAN Normal mode, the TXDCAN time-out function disables the transmission of the signal at the bus, setting the TXDCAN pin to recessive. This is implemented to prevent the bus from being blocked permanently due to an error. The transmitter is disabled and fixed to recessive. The CAN SPI control bits (**CAN** on **BUS_CTRL_1**) remain unchanged and the failure is stored in the SPI flag **CAN_FAIL**. The CAN transmitter stage is activated again after the dominant time-out condition is removed and the transceiver is automatically switched back to CAN Normal mode.

8.2.6 Bus dominant clamping

If the HS CAN bus signal is dominant for a time $t > t_{BUS\_CAN\_TO}$, in CAN Normal and Receiver-only mode, a bus dominant clamping is detected and the SPI bit **CAN_FAIL** is set. The transceiver configuration stays unchanged.

8.2.7 VCAN undervoltage detection

The voltage at the VCAN supply pin is monitored in CAN Normal and Receive-Only mode. If the HS CAN transceiver is set in CAN Wake-Capable mode, the VCAN supply pin is enable after that a valid WUP is detected. In case of VCAN undervoltage a signalization via SPI bit **VCAN_UV** is triggered and the TLE9272QXV33 disables the transmitter stage. If the CAN supply reaches a higher level than the under voltage detection threshold (VCAN > V_{CAN_UV}), the transceiver is automatically switched back to CAN Normal mode. The transceiver configuration stays unchanged.

8.3 Electrical characteristics

Table 13 Electrical characteristics

T_j = -40°C to +150°C; V_S = 5.5 V to 28 V; V_{CAN} = 4.75 V to 5.25 V; R_L = 60 Ω; CAN Normal mode; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
CAN supply voltage							
CAN supply undervoltage detection threshold	V_{CAN_UV}	4.45	–	4.85	V	CAN Normal mode, hysteresis included	P_8.3.1
CAN bus receiver							
Differential receiver threshold voltage, recessive to dominant edge	V_{diff,rd_N}	–	0.80	0.90	V	$V_{diff} = V_{CANH} - V_{CANL}$; -12 V ≤ V_{CM}(CAN) ≤ 12 V; CAN Normal mode	P_8.3.2
Dominant state differential input voltage range	$V_{diff\_D\_range}$	0.9	–	8.0	V	[1] $V_{diff} = V_{CANH} - V_{CANL}$; -12 V ≤ V_{CM}(CAN) ≤ 12 V; CAN Normal mode	P_8.3.50
Differential receiver threshold voltage, dominant to recessive edge	V_{diff,dr_N}	0.50	0.60	–	V	$V_{diff} = V_{CANH} - V_{CANL}$; -12 V ≤ V_{CM}(CAN) ≤ 12 V; CAN Normal mode	P_8.3.3
Recessive state differential input voltage range	$V_{diff\_R\_range}$	-3.0	–	0.5	V	[1] $V_{diff} = V_{CANH} - V_{CANL}$; -12 V ≤ V_{CM}(CAN) ≤ 12 V; CAN Normal mode	P_8.3.51
Common mode range	CMR	-12	–	12	V	[1]	P_8.3.4
CANH, CANL input resistance	R_i	20	40	50	kΩ	CAN Normal / Wake-capable mode; Recessive state -2 V ≤ $V_{CANH/L}$ ≤ +7 V	P_8.3.5
Differential input resistance	R_{diff}	40	80	100	kΩ	CAN Normal / Wake-capable mode; Recessive state -2 V ≤ $V_{CANH/L}$ ≤ +7 V	P_8.3.6
Input resistance deviation between CANH and CANL	DR_i	-3	–	3	%	[1] Recessive state V_{CANH} = V_{CANL} = 5 V	P_8.3.7
Input capacitance CANH, CANL versus GND	C_{in}	–	20	40	pF	[2] V_{TXDCAN} = 5 V	P_8.3.8
Differential input capacitance	C_{diff}	–	10	20	pF	[2] V_{TXDCAN} = 5 V	P_8.3.42

Table 13 Electrical characteristics (cont'd)

T_j = -40°C to +150°C; V_S = 5.5 V to 28 V; V_{CAN} = 4.75 V to 5.25 V; R_L = 60 Ω; CAN Normal mode; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Wake-up receiver threshold voltage, recessive to dominant edge	V_{diff, rd_W}	–	0.8	1.15	V	-12 V ≤ V_{CM}(CAN) ≤ 12 V; CAN Wake-capable mode	P_8.3.9
Wake-up receiver dominant state differential input voltage range	$V_{diff\_D\_range\_W}$	1.15	–	8.0	V	1) $V_{diff} = V_{CANH} - V_{CANL}$; -12 V ≤ V_{CM}(CAN) ≤ 12 V; CAN Wake-capable mode	P_8.3.52
Wake-up receiver threshold voltage, dominant to recessive edge	V_{diff, dr_W}	0.4	0.7	–	V	-12 V ≤ V_{CM}(CAN) ≤ 12 V; CAN Wake-capable mode	P_8.3.10
Wake-up receiver recessive state differential input voltage range	$V_{diff\_R\_range\_W}$	-3.0	–	0.4	V	1) $V_{diff} = V_{CANH} - V_{CANL}$; -12 V ≤ V_{CM}(CAN) ≤ 12 V; CAN Wake-capable mode	P_8.3.53
CAN bus transmitter							
CANH/CANL recessive output voltage (CAN Normal mode)	V_{CANL/H_NM}	2.0	–	3.0	V	CAN Normal mode $V_{TXDCAN} = V_{cc1}$; no load	P_8.3.11
CANH/CANL recessive output voltage (CAN Wake-capable mode)	V_{CANL/H_LP}	-0.1	–	0.1	V	CAN Wake-capable mode; $V_{TXDCAN} = V_{cc1}$; no load	P_8.3.43
CANH, CANL recessive output voltage difference $V_{diff} = V_{CANH} - V_{CANL}$ (CAN Normal mode)	$V_{diff\_r\_N}$	-500	–	50	mV	CAN Normal mode; $V_{TXDCAN} = V_{cc1}$; no load	P_8.3.12
CANH, CANL recessive output voltage difference $V_{diff} = V_{CANH} - V_{CANL}$ (CAN Wake-capable mode)	$V_{diff\_r\_W}$	-200	–	200	mV	CAN Wake-capable mode; $V_{TXDCAN} = V_{cc1}$; no load	P_8.3.44
CANL dominant output voltage	V_{CANL}	0.5	–	2.25	V	3) CAN Normal mode; V_{TXDCAN} = 0 V; V_{CAN} = 5 V; 50 Ω ≤ R_L ≤ 65 Ω	P_8.3.13

Table 13 Electrical characteristics (cont'd)

T_j = -40°C to +150°C; V_S = 5.5 V to 28 V; V_{CAN} = 4.75 V to 5.25 V; R_L = 60 Ω; CAN Normal mode; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
CANH dominant output voltage	V_{CANH}	2.75	–	4.5	V	[3] CAN Normal mode; V_{TXDCAN} = 0 V; V_{CAN} = 5 V; 50 Ω ≤ R_L ≤ 65 Ω	P_8.3.14
CANH, CANL dominant output voltage difference $V_{diff} = V_{CANH} - V_{CANL}$	$V_{diff\_d\_N}$	1.5	2.0	2.5	V	[3] CAN Normal mode; V_{TXDCAN} = 0 V; V_{CAN} = 5 V; 50 Ω ≤ R_L ≤ 65 Ω	P_8.3.15
CANH, CANL output voltage difference slope, recessive to dominant	$V_{diff\_slope\_rd}$	–	–	70	V/us	[1] 30% to 70% of measured differential bus voltage, C_L = 100 pF, R_L = 60 Ω	P_8.3.54
CANH, CANL output voltage difference slope, dominant to recessive	$V_{diff\_slope\_dr}$	–	–	70	V/us	[1] 70% to 30% of measured differential bus voltage, C_L = 100 pF, R_L = 60 Ω	P_8.3.55
CANH, CANL dominant output voltage difference $V_{diff} = V_{CANH} - V_{CANL}$ on extended bus load range	$V_{diff\_d\_N\_ext}$	1.5	–	5.0	V	[1] CAN Normal mode; V_{TXDCAN} = 0 V; V_{CAN} = 5 V; R_L = 2240 Ω	P_8.3.58
CANH short circuit current	I_{CANHsc}	-100	-80	-50	mA	CAN Normal mode; $V_{CANHshort}$ = -3 V	P_8.3.16
CANL short circuit current	I_{CANLsc}	50	80	100	mA	CAN Normal mode; $V_{CANLshort}$ = 18 V	P_8.3.17
Leakage current	$I_{CANH,lk}$ $I_{CANL,lk}$	–	5	7.5	µA	$V_S = V_{CAN}$ = 0 V; 0 V ≤ $V_{CANH,L}$ ≤ 5 V; [4] R_{test} = 0 / 47 kΩ	P_8.3.18
Receiver output RXDCAN							
HIGH level output voltage	$V_{RXDCAN,H}$	0.8 × V_{CC1}	–	–	V	CAN Normal mode; I_{RXDCAN} = -2 mA	P_8.3.19
LOW level output voltage	$V_{RXDCAN,L}$	–	–	0.2 × V_{cc1}	V	CAN Normal mode; I_{RXDCAN} = 2 mA	P_8.3.20
Transmission input TXDCAN							
HIGH level input voltage threshold	$V_{TXDCAN,H}$	–	–	0.7 × V_{cc1}	V	CAN Normal mode; recessive state	P_8.3.21

Table 13 Electrical characteristics (cont'd)

T_j = -40°C to +150°C; V_S = 5.5 V to 28 V; V_{CAN} = 4.75 V to 5.25 V; R_L = 60 Ω; CAN Normal mode; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
LOW level input voltage threshold	$V_{TXDCAN,L}$	0.3 × V_{cc1}	–	–	V	CAN Normal mode; dominant state	P_8.3.22
TXDCAN input hysteresis	$V_{TXDCAN,hys}$	–	0.12 × V_{cc1}	–	mV	1)	P_8.3.23
TXDCAN pull-up resistance	R_{TXDCAN}	20	40	80	kΩ	-	P_8.3.24
CAN transceiver enabling time	$t_{CAN,EN}$	8	13	18	µs	7) CSN = HIGH to first valid transmitted TXDCAN dominant	P_8.3.25
Dynamic CAN transceiver characteristics							
Driver symmetry $V_{SYM} = V_{CANH} + V_{CANL}$	V_{SYM}	4.5	–	5.5	V	5) CAN Normal mode; V_{TXDCAN} = 0 V / 5 V; V_{CAN} = 5 V; C_{SPLIT} = 4.7 nF; 50 Ω ≤ R_L ≤ 60 Ω	P_8.3.45
Min. dominant time for bus wake-up	t_{Wake1}	0.5	–	3.5	µs	-12 V ≤ V_{CM}(CAN) ≤ 12 V; V_{diff} ≤ 3 V CAN Wake-capable mode	P_8.3.26
Wake-up time-out, recessive bus	t_{Wake2}	0.5	–	10	ms	7) CAN Wake-capable mode	P_8.3.27
BUS bias reaction time	t_{bias}	–	–	250	µs	7) CAN Wake-capable mode V_{CAN} = 5 V; C_L = 100 pF; C_{GND} = 100 pF; R_L = 60 Ω	P_8.3.57
Loop delay (recessive to dominant)	$t_{LOOP,f}$	–	150	255	ns	5) CAN Normal mode; C_L = 100 pF; R_L = 60 Ω; V_{CAN} = 5 V; C_{RXDCAN} = 15 pF	P_8.3.28
Loop delay (dominant to recessive)	$t_{LOOP,r}$	–	150	255	ns	5) CAN Normal mode; C_L = 100 pF; R_L = 60 Ω; V_{CAN} = 5 V; C_{RXDCAN} = 15 pF	P_8.3.29

Table 13 Electrical characteristics (cont'd)

T_j = -40°C to +150°C; V_S = 5.5 V to 28 V; V_{CAN} = 4.75 V to 5.25 V; R_L = 60 Ω; CAN Normal mode; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Propagation delay TXDCAN LOW to bus dominant	$t_{d(L),T}$	–	50	–	ns	CAN Normal mode; C_L = 100 pF; R_L = 60 Ω; V_{CAN} = 5 V	P_8.3.30
Propagation delay TXDCAN HIGH to bus recessive	$t_{d(H),T}$	–	50	–	ns	CAN Normal mode; C_L = 100 pF; R_L = 60 Ω; V_{CAN} = 5 V	P_8.3.31
Propagation delay bus dominant to RXDCAN LOW	$t_{d(L),R}$	–	100	–	ns	CAN Normal mode; C_L = 100 pF; R_L = 60 Ω; V_{CAN} = 5 V; C_{RXDCAN} = 15 pF	P_8.3.32
Propagation delay bus recessive to RXDCAN HIGH	$t_{d(H),R}$	–	100	–	ns	CAN Normal mode; C_L = 100 pF; R_L = 60 Ω; V_{CAN} = 5 V; C_{RXDCAN} = 15 pF	P_8.3.33
Received recessive bit width	$t_{bit(RXD)}$	400	–	550	ns	CAN Normal mode; C_L = 100 pF; R_L = 60 Ω; V_{CAN} = 5 V; C_{RXD} = 15 pF; $t_{bit(TXD)}$ = 500 ns; Parameter definition in according to **Figure 23**.	P_8.3.39
Transmitted recessive bit width	$t_{bit(BUS)}$	435	–	530	ns	CAN Normal mode; C_L = 100 pF; R_L = 60 Ω; V_{CAN} = 5 V; C_{RXD} = 15 pF; $t_{bit(TXD)}$ = 500 ns; Parameter definition in according to **Figure 23**.	P_8.3.40

Table 13 Electrical characteristics (cont'd)

T_j = -40°C to +150°C; V_S = 5.5 V to 28 V; V_{CAN} = 4.75 V to 5.25 V; R_L = 60 Ω; CAN Normal mode; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Receiver timing symmetry[6]	Δt_{Rec}	-65	–	40	ns	CAN Normal mode; C_L = 100 pF; R_L = 60 Ω; V_{CAN} = 5 V; C_{RXD} = 15 pF; $t_{bit(TXD)}$ = 500 ns; Parameter definition in according to **Figure 23**.	P_8.3.41
Received recessive bit width	$t_{bit(RXD)}$	120	–	220	ns	CAN Normal mode; C_L = 100 pF; R_L = 60 Ω; V_{CAN} = 5 V; C_{RXD} = 15 pF; $t_{bit(TXD)}$ = 200 ns; Parameter definition in according to **Figure 23**.	P_8.3.46
Transmitted recessive bit width	$t_{bit(BUS)}$	155	–	210	ns	CAN Normal mode; C_L = 100 pF; R_L = 60 Ω; V_{CAN} = 5 V; C_{RXD} = 15 pF; $t_{bit(TXD)}$ = 200 ns; Parameter definition in according to **Figure 23**.	P_8.3.47
Receiver timing symmetry[6]	Δt_{Rec}	-45	–	15	ns	CAN Normal mode; C_L = 100 pF; R_L = 60 Ω; V_{CAN} = 5 V; C_{RXD} = 15 pF; $t_{bit(TXD)}$ = 200 ns; Parameter definition in according to **Figure 23**.	P_8.3.48
TXDCAN permanent dominant time-out	t_{TXDCAN_TO}	–	1.85	–	ms	[7] CAN Normal mode	P_8.3.34
BUS permanent dominant time-out	$t_{BUS\_CAN\_TO}$	–	1.85	–	ms	[7] CAN Normal mode	P_8.3.35

1) Not subject to production test, specified by design.
2) Not subject to production test, specified by design, S2P - Method; f = 10 Mhz.
3) Voltage value valid for time < t_{TXDCAN_TO}.
4) R_{tests} between (V_S/V_{CAN}) and 0 V (GND).
5) V_{SYM} shall be observed during dominant and recessive state and also during the transition dominant to recessive and vice versa while TxD is simulated by a square signal (50% duty cycle), a frequency of 1 MHz.
6) t_{Rec}=$t_{bit(RXD)}$ -$t_{bit(BUS)}$.
7) Not subject to production test, tolerance defined by internal oscillator tolerance.

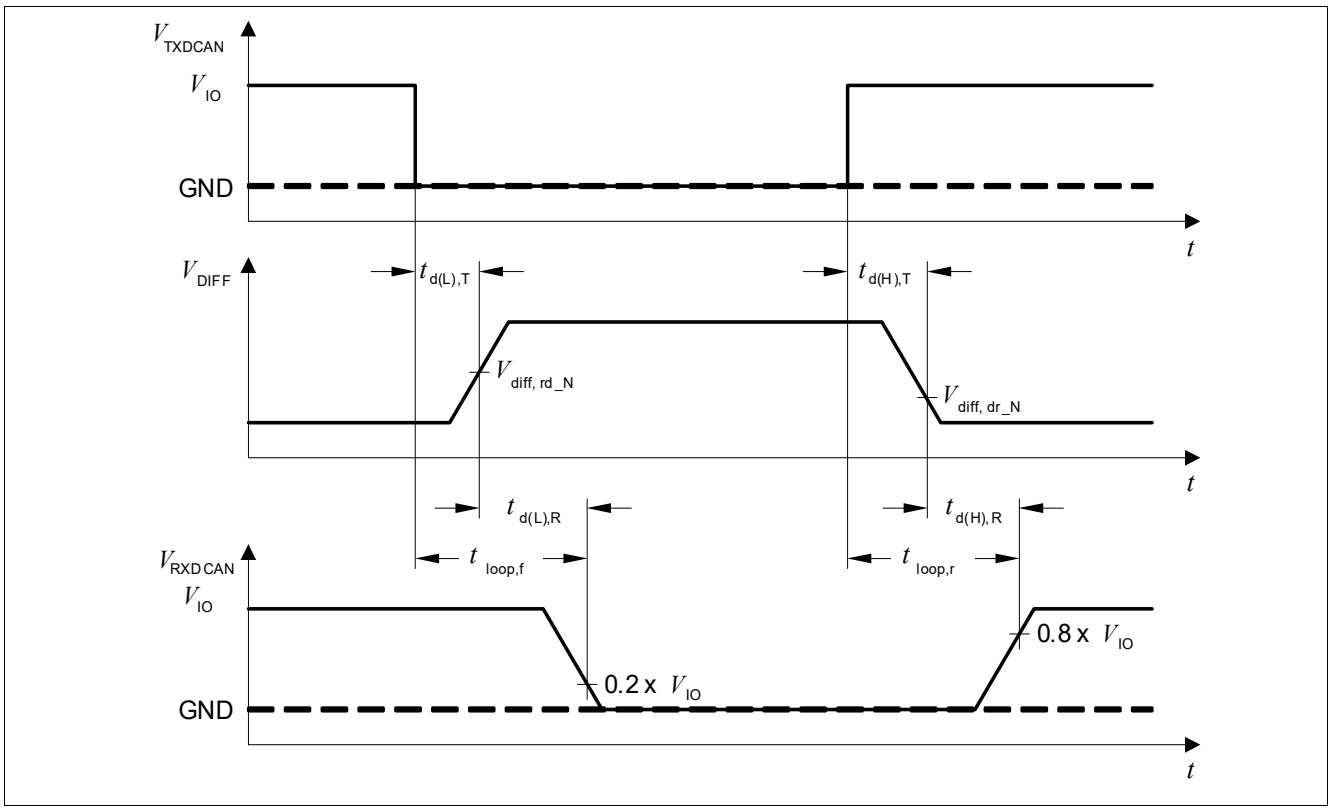

Figure 22 Timing diagrams for dynamic characteristics

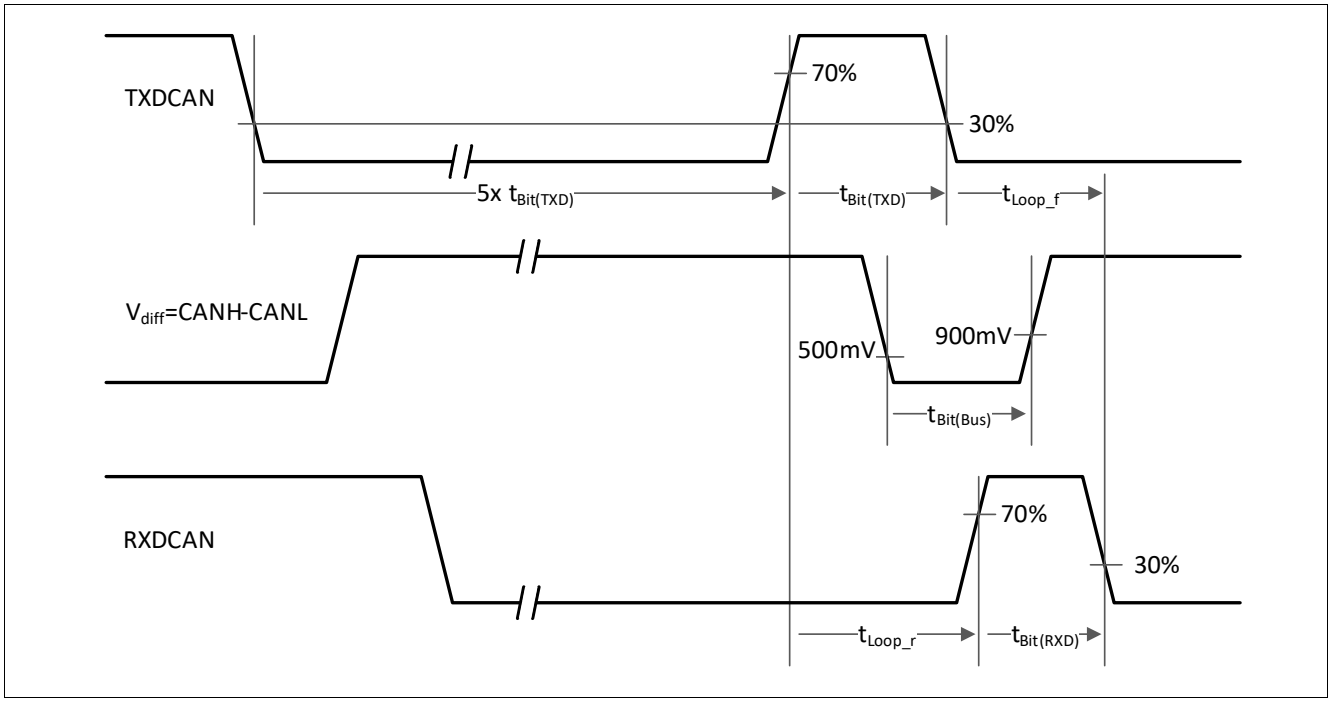

Figure 23 From ISO 11898-2: tloop, tbit(TXD), tbit(Bus), tbit(RXD) definitions

9 LIN transceiver

9.1 Block description

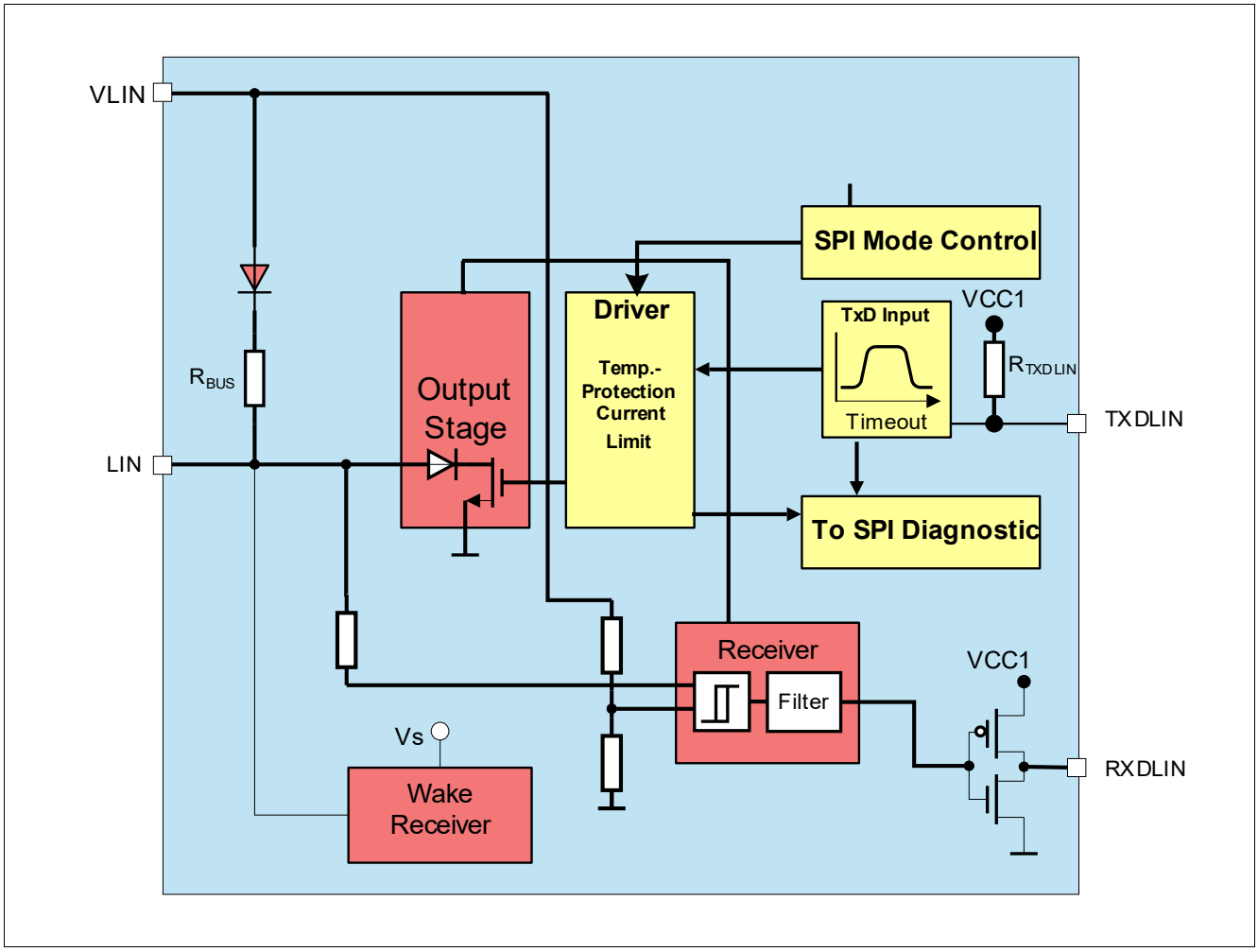

Figure 24 Block diagram

9.1.1 LIN specifications

The LIN network is standardized by international regulations. The device is compliant with the LIN2.2 specification. The physical layer specification LIN2.2 is a superset of the previous LIN specifications, like LIN2.0, LIN2.1 or LIN1.3. The integrated LIN transceivers are according to the LIN2.2 standard.

The device is compliant to the physical layer standard SAE-J2602-2. The SAE-J2602-2 standard differs from the LIN2.2 standard mainly by the lower data rate (10.4 kbps).

9.2 Functional description

The LIN bus is a single wire, bidirectional bus, used for in-vehicle networks. The LIN transceivers implemented inside the TLE9272QXV33 are the interface between the microcontroller and the physical LIN bus. The digital output data from the microcontroller are driven to the LIN bus via the TXDLIN input pin on the TLE9272QXV33. The transmit data stream on the TXDLIN input is converted to a LIN bus signal with an optimized slew rate to minimize the EME level of the LIN network. The RXDLIN output sends back the information from the LIN bus to the microcontroller. The receiver has an integrated filter network to suppress noise on the LIN bus and to increase the EMI (Electromagnetic Immunity) level of the transceiver.

Two logical states are possible on the LIN bus according to the LIN Specification 2.2.

Every LIN network consists of a master node and one or more slave nodes. To configure the TLE9272QXV33 for master node applications, a resistor in the range of 1 kΩ and a reverse diode must be connected between the LIN bus and the power supply VS.

The different transceiver modes can be controlled using the SPI **LIN2**, **LIN3**, bits.

The transceiver can also be configured to wake capable in order to save current and to ensure a safe transition from SBC Normal to Sleep mode (to avoid losing messages).

Figure 25 shows the possible transceiver mode transitions when changing the SBC mode.

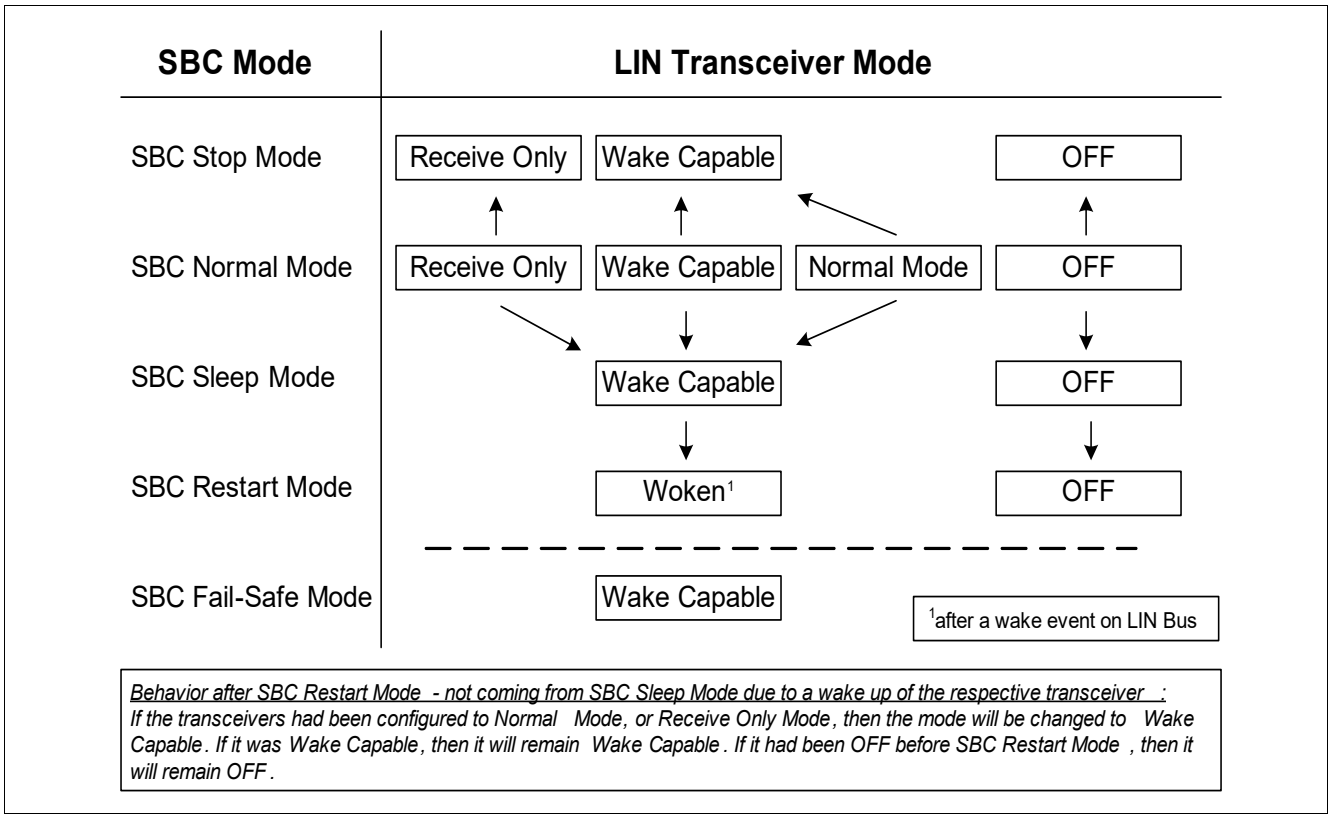

Figure 25 LIN mode control diagram

9.2.1 LIN OFF mode

The LIN OFF mode is the default mode after power-up of the SBC. It is available in all SBC modes and is intended to completely stop LIN activities or when LIN communication is not needed. In LIN OFF mode, a wake-up event on the bus will be ignored.

9.2.2 LIN Normal mode

The LIN transceiver is enabled via SPI in SBC Normal mode. LIN Normal mode is designed for normal data transmission/reception within the LIN network. The mode is available only in SBC Normal mode.

Transmission

The signal from the microcontroller is applied to the TXDLIN input of the SBC. The bus driver switches the LIN output stage to transfer this input signal to the LIN bus line.

Enabling sequence

The LIN transceiver requires an enabling time $t_{LIN,EN}$ before a message can be sent on the bus. This means that the TXDLIN signal can only be pulled LOW after the enabling time. If this is not ensured, then the TXDLIN needs to be set back to HIGH (= recessive) until the enabling time is completed. Only the next dominant bit will be transmitted on the bus. **Figure 26** shows different scenarios and explanations for LIN enabling.

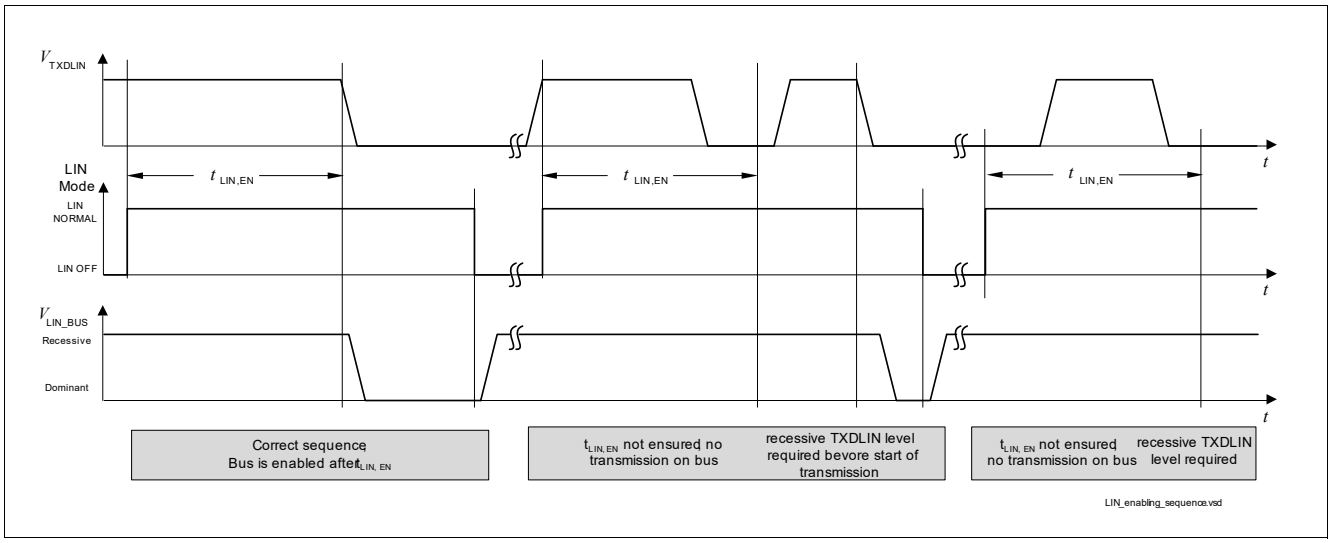

Figure 26 LIN transceiver enabling sequence

Reduced electromagnetic emission

To reduce electromagnetic emissions (EME), the bus driver controls LIN slopes symmetrically. The configuration of the different slopes is described in **Chapter 9.2.8**.

Reception

Analog LIN bus signals are converted into digital signals at RXDLIN via the input receiver.

9.2.3 LIN Receive-Only mode

In LIN Receive-Only mode (RX only), the driver stage is disabled but reception is still possible. This mode is accessible by an SPI command and is available in SBC Normal and SBC Stop mode.

9.2.4 LIN Wake-Capable mode

This mode can be used in SBC Stop, Sleep, Restart and Normal mode by programming via SPI and it is used to monitor bus activities. It is automatically accessed in SBC Fail-Safe mode. A wake up is detected, if a recessive to dominant transition on the LIN bus is followed by a dominant level of longer than $t_{WK,Bus}$, followed by a dominant to recessive transition. The dominant to recessive transition will cause a wake up of the LIN transceiver. A wake-up results different behavior of the SBC, as described in **Table 14**. As a signalization to the microcontroller, the RXDLIN pin is set LOW and will stay LOW until the LIN transceiver is changed to any other mode. After a wake-up event, the transceiver can be switched to LIN Normal mode for communication.

Table 14 Action due to a LIN bus wake-up

SBC mode	SBC mode after wake	VCC1	INT	RXDLIN
Normal mode	Normal mode	ON	LOW	LOW
Stop mode	Stop mode	ON	LOW	LOW
Sleep mode	Restart mode	Ramping up	HIGH	LOW
Restart mode	Restart mode	ON	HIGH	LOW
Fail-Safe mode	Restart mode	Ramping up	HIGH	LOW

Rearming the transceiver for wake capability

After a bus wake-up event, the transceiver is woken. However, the **LIN1**, **LIN2 LIN3** transceiver mode bits will still show wake capable (=‘01’) so that the RXDLIN signal will be pulled low. The Wake-Capable mode of the LIN transceiver can be reenabled in one of two ways after a wake-up event:

- By toggling the LIN transceiver mode, i.e. switched to LIN Normal mode, LIN Receive-Only mode or LIN Off, before switching to LIN Wake-Capable mode again
- Occurs automatically when the SBC changes to SBC Stop, SBC Sleep, or SBC Fail-Safe mode to ensure wake-up capability
- if the SBC is in SBC Stop mode, the LIN’s are rearmed automatically if the SBC is set again in SBC Stop mode

Wake-up in SBC Stop and SBC Normal mode

In SBC Stop mode, if a wake-up is detected, it is signaled by the INT output and in the **WK_STAT_2** SPI register. It is also signaled by RXDLIN put to LOW. The same applies for the SBC Normal mode. The microcontroller should set the device to SBC Normal mode; there is no automatic transition to Normal mode.

For functional safety reasons, the watchdog will be automatically enabled in SBC Stop mode after a bus wake-up event in case it was disabled before (if bit **WD_EN_WK_BUS** was configured to HIGH before).

Wake-up in SBC Sleep mode

Wake-up is possible via a LIN message (filter time t > $t_{WK,Bus}$). The wake-up automatically transfers the SBC to SBC Restart mode and from there to Normal mode. The corresponding RXDLIN pin in set to LOW. The microcontroller is able to detect the low signal on RXDLIN and to read the wake source out of the **WK_STAT_2**

register via SPI. No interrupt is generated when coming out of Sleep mode. The microcontroller can now switch the LIN transceiver into LIN Normal mode via SPI to start communication.

9.2.5 TXDLIN Time-out feature

If the TXDLIN signal is dominant for the time t > **$t_{BUS\_LIN\_TO}$**, the TXDLIN time-out function deactivates the LIN transmitter output stage temporarily. The transceiver remains in recessive state. The TXDLIN time-out function prevents the LIN bus from being blocked by a permanent LOW signal on the TXDLIN pin caused by a failure. The failure is stored in the SPI flag **LIN1_FAIL**, , **LIN3_FAIL** and on **BUS_STAT_1** and **BUS_STAT_2** registers. The LIN transmitter stage is activated again after the dominant time-out condition is removed.

The TXDLIN time-out feature can be disabled with SPI bit **LIN_TXD_ TO** for all LINs at the same time.

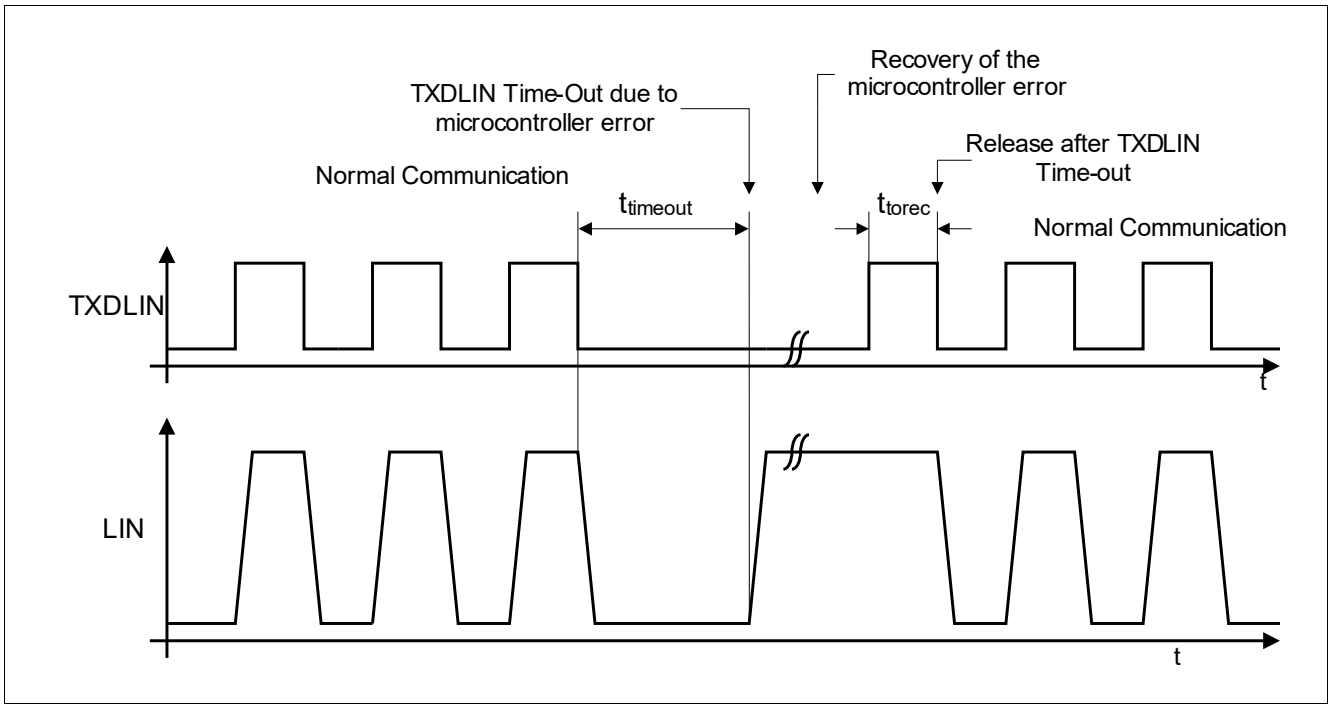

Figure 27 TXDLIN time-out function

9.2.6 Bus dominant clamping

If the LIN bus signal is dominant for a time $t > t_{BUS\_LIN\_TO}$ in LIN Normal or Receive-Only mode, then a bus dominant clamping is detected and the SPI bits **LIN1_FAIL**, **LIN3_FAIL** and are set. The transceiver configuration stays unchanged.

9.2.7 Undervoltage detection

In case the supply voltage VLIN is dropping below the VLIN undervoltage detection threshold (VLIN < **$V_{LIN,UVD}$**), the TLE9272QXV33 will set the LINx in Receive-Only mode (the transmitter is disabled). The receiver stage is active. If the power supply VLIN reaches a higher level than the VLIN undervoltage detection threshold (VLIN > **$V_{LIN,UVD}$**), the TLE9272QXV33 continues with normal operation.

9.2.8 Slope selection

The LIN transceiver offers a LIN Low-Slope mode for 10.4 kBaud communication and a LIN Normal-Slope mode for 20 kBaud communication. The only difference is the behavior of the transmitter. In LIN Low-Slope mode, the transmitter uses a lower slew rate to further reduce the EME compared to Normal-Slope mode. This complies with SAE J2602 requirements.

By default, the device works in LIN Normal-Slope mode. The selection of LIN Low-Slope mode is done by an SPI bit **LIN_LSM** and will become effective as soon as CSN goes HIGH for all LINx. Only the LIN slope is changed. The selection is accessible in SBC Normal mode only.

9.2.9 Flash programming via LIN

The device allows LIN flash programming, e.g. of another LIN slave with a communication of up to 115 kbps. This feature is enabled by de-activating the slope control mechanism via a SPI command (bit LIN_FLASH) and will become effective as soon as CSN goes HIGH' for all LINx. The SPI bit can be set in SBC Normal mode.

Note: It is recommended to perform flash programming only at nominal supply voltage VS = 13.5 V to ensure stable data communication.

9.3 Electrical characteristics of the LIN transceiver

Table 15 Electrical characteristics: LIN transceiver

T_j = -40°C to +150°C, V_{LIN} = 5.5 V to 18 V, R_L = 500 Ω, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Receiver output (RXDLIN pin)							
HIGH level output voltage	$V_{RXDLIN,H}$	0.8 × V_{CC}	–	–	V	I_{RXDLIN} = -2 mA V_{bus} = V_S	P_9.3.1
LOW level output voltage	$V_{RXDLIN,L}$	–	–	0.2 × V_{CC}	V	I_{RXDLIN} = 2 mA V_{bus} = 0 V	P_9.3.2
Transmission input (TXDLIN pin)							
HIGH level input voltage	$V_{TXDLIN,H}$	0.7 × V_{CC}	–	–	V	Recessive state	P_9.3.3
TXDLIN input hysteresis	$V_{TXDLIN,hys}$	–	0.2 × V_{CC}	–	V	1)	P_9.3.4
LOW level input voltage	$V_{TXDLIN,L}$	–	–	0.3 × V_{CC}	V	Dominant state	P_9.3.5
TXDLIN pull-up resistance	R_{TXDLIN}	20	40	80	kΩ	V_{TXDLIN} = 0 V	P_9.3.6
LIN bus receiver (LIN pin)							
Receiver threshold voltage, recessive to dominant edge	$V_{Bus,rd}$	0.4 × V_{LIN}	0.45 × V_{LIN}	–	V	–	P_9.3.7
Receiver dominant state	$V_{Bus,dom}$	–	–	0.4 × V_{LIN}	V	LIN2.2 Param. 17	P_9.3.8
Receiver threshold voltage, dominant to recessive edge	$V_{Bus,dr}$	–	0.55 × V_{LIN}	0.60 × V_{LIN}	V	–	P_9.3.9
Receiver recessive state	$V_{Bus,rec}$	0.6 × V_{LIN}	–	–	V	LIN2.2 Param 18	P_9.3.10
Receiver center voltage	$V_{Bus,c}$	0.475 × V_{LIN}	0.5 × V_{LIN}	0.525 × V_{LIN}	V	LIN2.2 Param 19	P_9.3.11
Receiver hysteresis	$V_{Bus,hys}$	0.07 × V_{LIN}	0.1 × V_{LIN}	0.175 × V_{LIN}	V	$V_{bus,hys}$ = $V_{bus,rec}$ - $V_{bus,dom}$ LIN2.2 Param 20	P_9.3.12
Wake-up threshold voltage	$V_{Bus,wk}$	0.40 × V_{LIN}	0.5 × V_{LIN}	0.6 × V_{LIN}	V	–	P_9.3.13
Dominant time for bus wake-up	$t_{WK,Bus}$	30	–	150	µs	2)	P_9.3.14

Table 15 Electrical characteristics: LIN transceiver (cont'd)

T_j = -40°C to +150°C, V_{LIN} = 5.5 V to 18 V, R_L = 500 Ω, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
LIN bus transmitter (LIN pin)							
Bus serial diode voltage drop	$V_{serdiode}$	0.4	0.7	1.0	V	1) $V_{TXDLIN} = V_{CC1}$; LIN2.2 Param 21	P_9.3.15
Bus recessive output voltage	$V_{BUS,ro}$	0.8 × V_{LIN}	–	V_{LIN}	V	V_{TXDLIN} = high Level	P_9.3.16
Bus short circuit current	$I_{BUS,sc}$	40	100	150	mA	V_{BUS} = 18 V; LIN2.2 Param 12	P_9.3.20
Leakage current loss of ground	$I_{BUS,lk1}$	-1000	-450	20	µA	V_{LIN} = 0 V; -12 V ≤ V_{BUS} ≤ 6 V; LIN2.2 Param 15	P_9.3.21
Leakage current loss of battery	$I_{BUS,lk2}$	–	–	20	µA	V_{LIN} = 0 V; 0 V ≤ V_{BUS} ≤ 18 V; LIN2.2 Param 16	P_9.3.22
Leakage current driver off	$I_{BUS,lk3}$	-1	–	–	mA	V_{LIN} = 18 V; V_{BUS} = 0 V; LIN2.2 Param 13	P_9.3.23
Leakage current driver off	$I_{BUS,lk4}$	–	–	20	µA	V_{LIN} = 8 V; V_{BUS} = 18 V; LIN2.2 Param 14	P_9.3.24
Bus pull-up resistance	R_{BUS}	20	30	47	kΩ	Normal mode LIN2.2 Param 26	P_9.3.25
LIN input capacitance	C_{BUS}		20	25	pF	1)	P_9.3.26
Receiver propagation delay bus dominant to RXDLIN LOW	$t_{d(L),R}$	–	1	6	µs	V_{CC} = 5 V; C_{RXDLIN} = 20 pF; LIN2.2 Param 31	P_9.3.27
Receiver propagation delay bus recessive to RXDLIN HIGH	$t_{d(H),R}$	–	1	6	µs	V_{CC} = 5 V; C_{RXDLIN} = 20 pF; LIN2.2 Param 31	P_9.3.28
Receiver delay symmetry	$t_{sym,R}$	-2	–	2	µs	$t_{sym,R} = t_{d(L),R} - t_{d(H),R}$; LIN2.2 Param 32	P_9.3.29
LIN transceiver enabling time	$t_{LIN,EN}$	8	13	18	µs	2) time from enabling LIN (CS HIGH) to first signal on RXDLIN	P_9.3.39
Bus dominant time out	$t_{BUS\_LIN\_TO}$	–	20	–	ms	1)2)	P_9.3.30
TXDLIN dominant time out	$t_{TXDLIN\_LIN\_TO}$	–	20	–	ms	1)2) V_{TXDLIN} = 0 V	P_9.3.31

Table 15 Electrical characteristics: LIN transceiver (cont'd)

T_j = -40°C to +150°C, V_{LIN} = 5.5 V to 18 V, R_L = 500 Ω, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
TXDLIN dominant time out recovery time	t_{torec}	–	10	–	µs	1)2)	P_9.3.32
Duty cycle D1 (For worst case at 20 kbit/s) LIN2.2 normal slope	D1	0.396	–	–		3) $TH_{Rec}(max) = 0.744 \times V_S$; $TH_{Dom}(max) = 0.581 \times V_S$; V_{LIN} = 7.0…18 V; t_{bit} = 50 µs; D1 = $t_{bus\_rec(min)}/2\ t_{bit}$; LIN2.2 Param 27	P_9.3.33
Duty cycle D2 (for worst case at 20 kbit/s) LIN2.2 normal slope	D2	–	–	0.581		3) $TH_{Rec}(min) = 0.422 \times V_S$; $TH_{Dom}(min) = 0.284 \times V_S$; V_{LIN} = 7.0…18 V; t_{bit} = 50 µs; D2 = $t_{bus\_rec(max)}/2\ t_{bit}$; LIN2.2 Param 28	P_9.3.34
Duty cycle D3 (for worst case at 10.4 kbit/s) SAE J2602 low slope	D3	0.417	–	–		3) $TH_{Rec}(max) = 0.778 \times V_S$; $TH_{Dom}(max) = 0.616 \times V_S$; V_{LIN} = 7.0…18 V; t_{bit} = 96 µs; D3 = $t_{bus\_rec(min)}/2\ t_{bit}$; LIN2.2 Param 29	P_9.3.35
Duty cycle D4 (for worst case at 10.4 kbit/s) SAE J2602 low slope	D4	–	–	0.590		3) $TH_{Rec}(min) = 0.389 \times V_S$; $TH_{Dom}(min) = 0.251 \times V_S$; V_{LIN} = 7.0…18 V; t_{bit} =96 µs; D4 = $t_{bus\_rec(max)}/2\ t_{bit}$; LIN2.2 Param 30	P_9.3.36

1) Not subject to production test, specified by design.

2) Not subject to production test, tolerance defined by internal oscillator tolerance.

3) Bus load conditions concerning LIN spec 2.2 C_{LIN}, R_{LIN} = 1 nF, 1 kΩ / 6.8 nF, 660 Ω / 10 nF, 500 Ω.

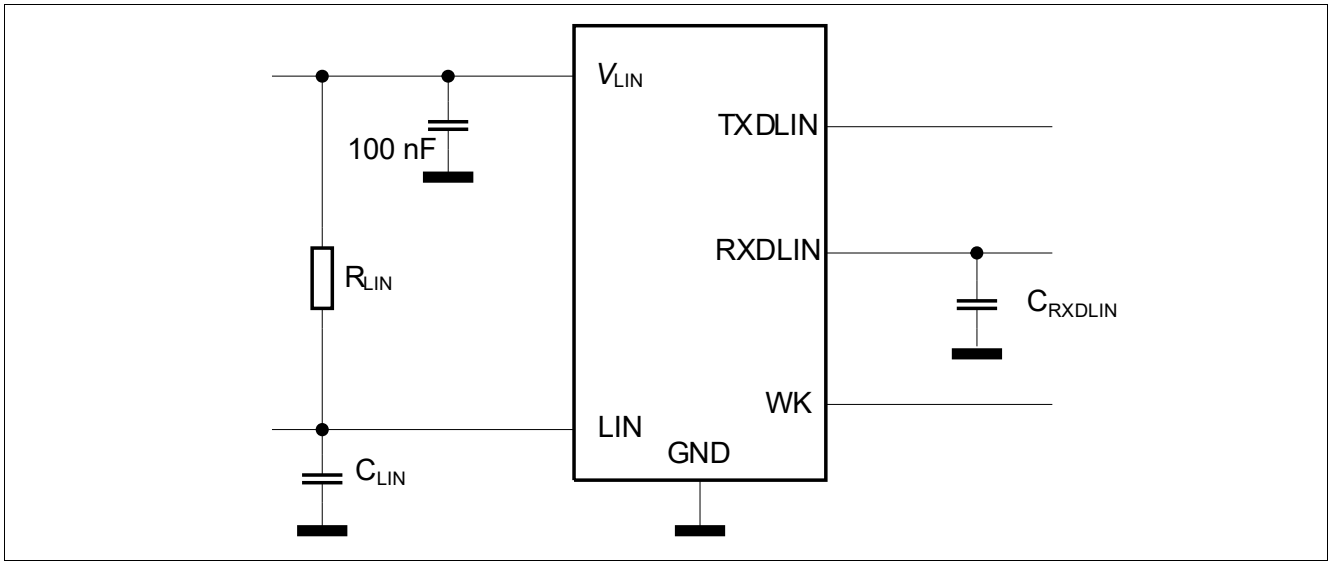

Figure 28 Simplified test circuit for dynamic characteristics

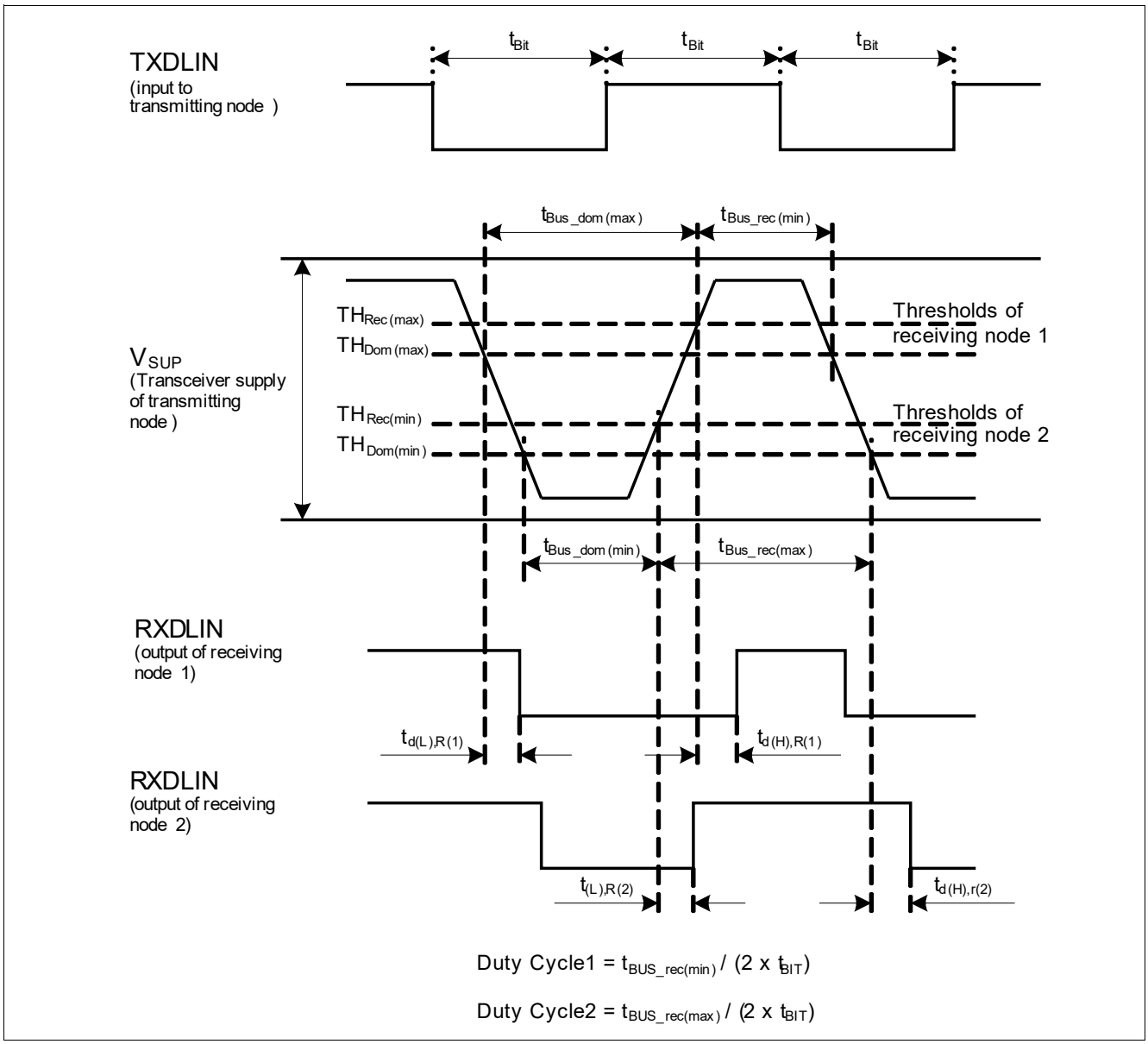

Figure 29 Timing diagram for dynamic characteristics

10 Wake input

10.1 Block description

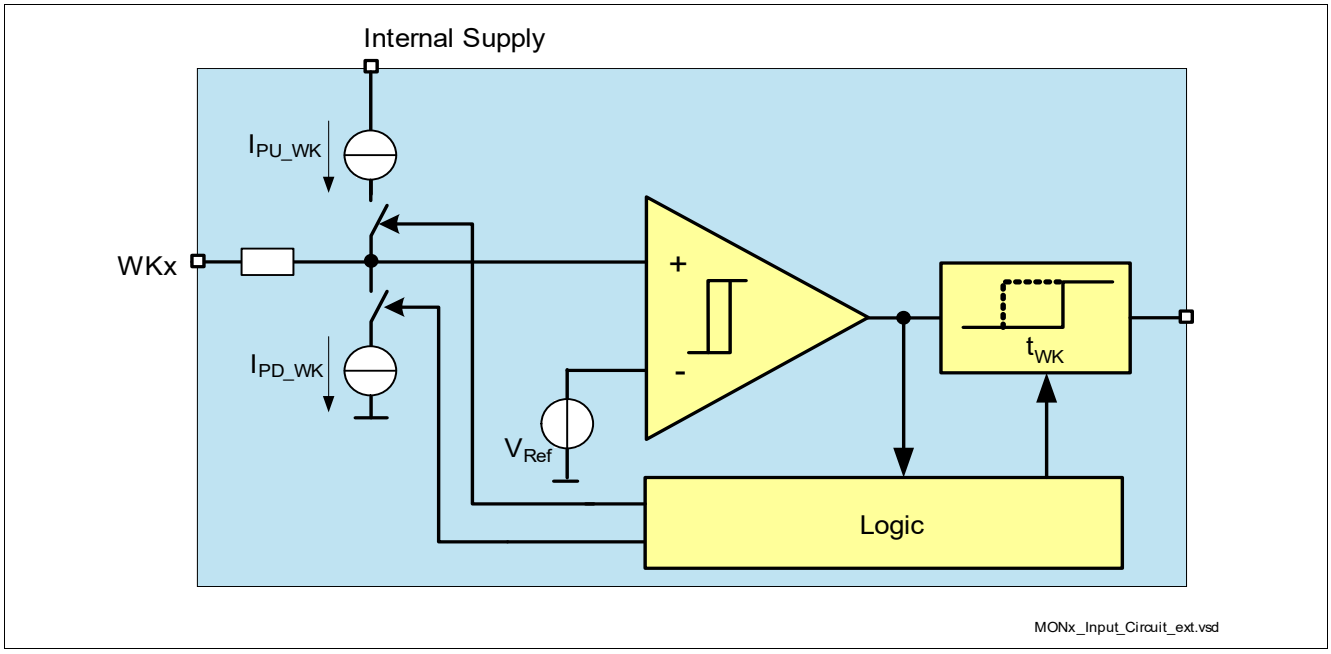

Figure 30 Wake input block diagram

Features

- One high-voltage inputs with 3 V (typ.) threshold voltage
- Wake-up capability for power saving modes
- Switch feature for DC/DC mode (PFM/PWM) in Stop mode
- Sensitive to level changes LOW to HIGH and HIGH to LOW
- Pull-up and pull-down current, configurable via SPI
- In SBC Normal and SBC Stop mode, the level of WK pin can be read via SPI

10.2 Functional description

The wake input pin is edge-sensitive input with a switching threshold of typically 3 V. This means that both transitions, HIGH to LOW and LOW to HIGH, result in SBC signalling. The signal is created in one of the following ways:

- By triggering the interrupt in SBC Normal and SBC Stop mode
- Waking up the device in SBC Sleep and SBC Fail-Safe mode

The WK pin can also be configured as a selection pin for PFM / PWM mode in Stop mode using the **PWM_BY_WK** bit of **HW_CTRL** register. In this case a LOW level at the WK pin will set the buck converter modulation to PFM mode, a HIGH level will set the buck converter modulation to PWM mode. In this configuration, the filter time is not taken into account because a defined signal from µC is expected.

The typical monitoring threshold voltage (**V_{WKth}**) is 3 V and therefore it is not recommend to use the pin directly connected to the microcontroller.

Two different wake detection modes can be selected via SPI:

- Static sense: WK inputs are always active
- Cyclic sense: WK inputs are only active for a certain time period (see **Chapter 5.2.1**)

The filtering time is **t_{FWK}**. The wake-up capability can be enabled or disabled via SPI command.

Figure 31 shows a typical wake-up timing and parasitic filter.

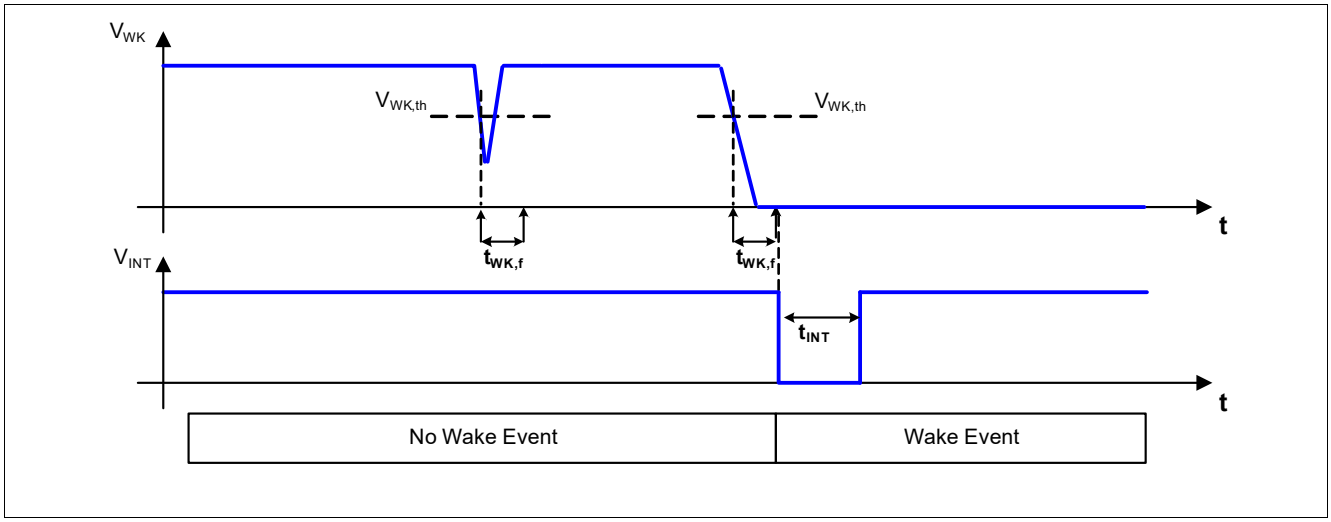

Figure 31 Wake-up filter timing for static sense

The state of the WK pin (LOW or HIGH) can always be read in SBC Normal and Stop mode at the bit **WK** on register **WK_LVL_STAT**.

When setting the bit **WK_EN**, to 1, the device wakes up from Sleep mode with a HIGH to LOW or LOW to HIGH transition on the selected WK input, in SBC Stop and SBC Normal mode an interrupt will be generated. From SBC Fail-Safe mode the device will always go to SBC Restart mode with a HIGH to LOW or LOW to HIGH transition. The wake source for a wake via wake pin can be read in the register **WK_STAT_1** at the bit **WK_WU**.

10.2.1 Wake input configuration

To ensure a defined and stable voltage levels at the internal comparator input it is possible to configure integrated current sources via the SPI register **WK_PUPD_CTRL**. The **Table 16** shows the possible pull-up and pull-down current.

Table 16 Pull-up/pull-down resistor

WK_PUPD_1	WK_PUPD_0	Output current	Note
0	0	No current source	WK is floating if left open (default setting)
0	1	Pull-down current	WK input internally pulled to GND
1	0	Pull-up current	WK input internally pulled to 5 V
1	1	Automatic switching	If a HIGH level is detected the pull-up current is activated, if LOW level is detected the pull down current is activated

Note: If there is no pull-up or pull-down configured on the WK input, then the respective input should be tied to GND or VS on board to avoid unintended floating and waking of the pin.

An example illustration of automatic switching configuration is shown in **Figure 32**.

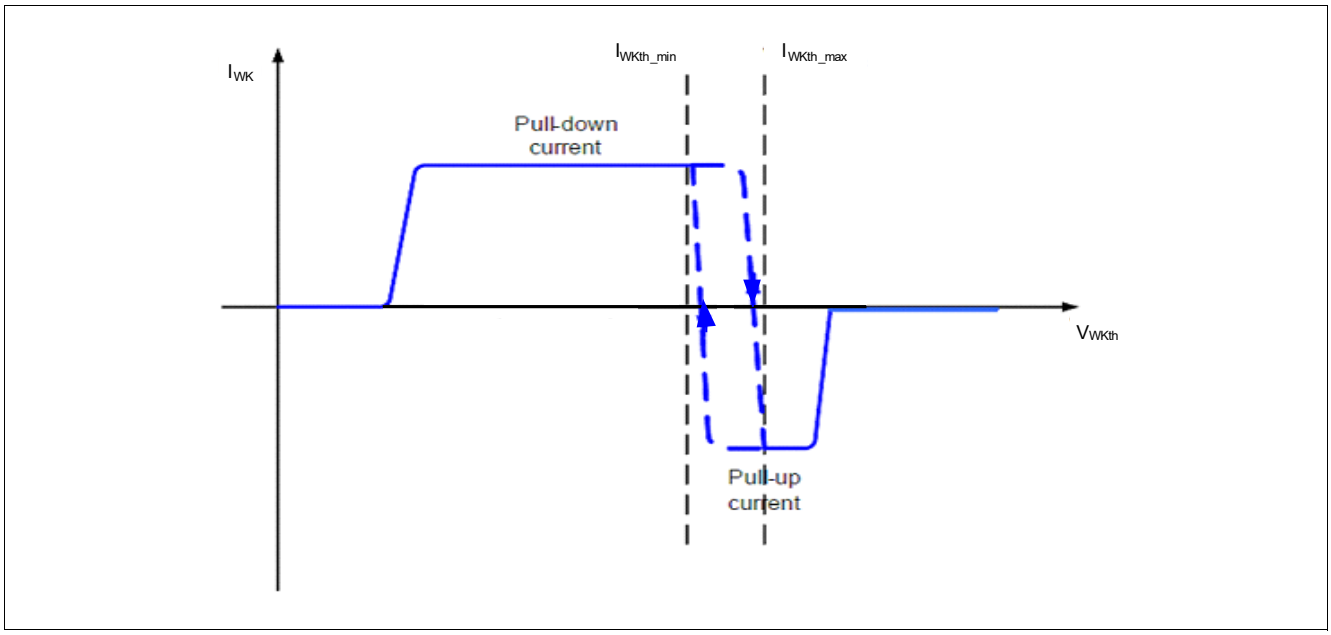

Figure 32 Illustration for pull-up/pull-down current sources with automatic switching configuration

10.3 Electrical characteristics

Table 17 Electrical characteristics

T_j = -40°C to +150°C; V_S = 5.5 V to 28 V; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
WK input pin characteristics							
Wake-up/monitoring threshold voltage	V_{WKth}	2	3	4	V	Hysteresis included	P_10.3.1
Threshold hysteresis	$V_{WKNth,hys}$	0.1	–	0.7	V	–	P_10.3.2
WK pin pull-up current	I_{PU_WK}	-20	-10	-3	µA	V_{WK_IN} = 4 V	P_10.3.3
WK pin pull-down current	I_{PD_WK}	3	10	20	µA	V_{WK_IN} = 2 V	P_10.3.4
Input leakage current	$I_{LK,l}$	-2	–	2	µA	0 V < V_{WK_IN} < 28 V SBC Stop or Sleep mode	P_10.3.5
Timing							
Wake-up filter time	t_{FWK}	–	16	–	µs	1)	P_10.3.6

1) Not subject to production test, tolerance defined by internal oscillator tolerance.

11 Interrupt function

11.1 Block and functional description

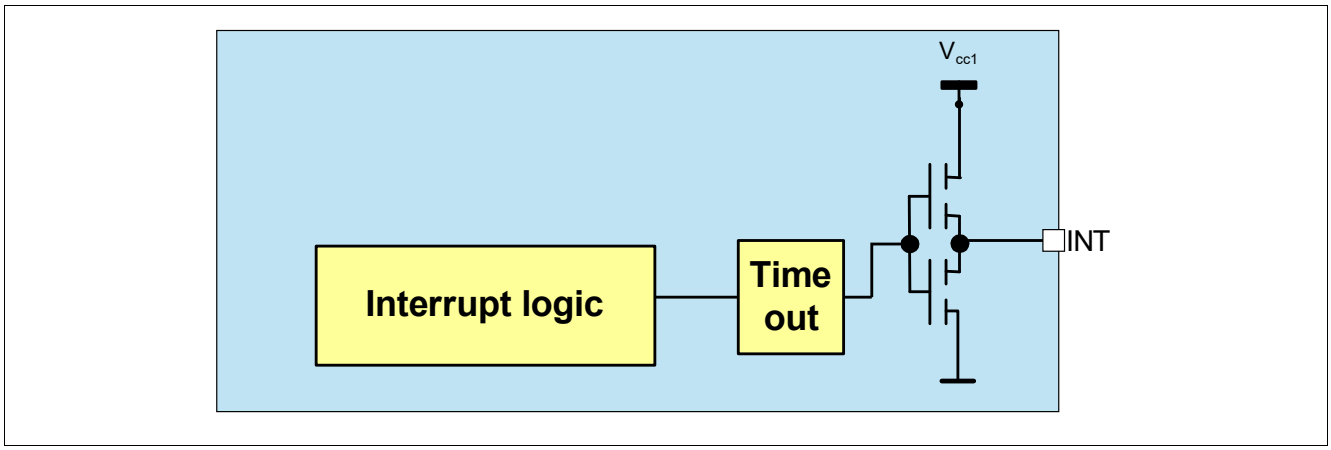

Figure 33 Interrupt block diagram

The interrupt is used to signal wake-up events in real time to the microcontroller. The interrupt block is designed as a push/pull output stage as shown in **Figure 33**. An interrupt is triggered and the INT pin is pulled LOW (active LOW) for t_{INT} in SBC Normal and Stop mode and it is released again once t_{INT} is expired. The minimum HIGH-time of INT between two consecutive interrupts is t_{INTD}. An interrupt does not automatically cause a SBC mode change.

The following wake-up events will be signaled via INT:

- All wake-up events stored in the wake status SPI register **WK_STAT_1** and **WK_STAT_2**
- An interrupt is only triggered if the respective function is also enabled as a wake source
- The register **WK_LVL_STAT** is not generating interrupts

In addition to this behavior, an INT will be triggered when:

- The SBC is sent to SBC Stop mode and not all bits were cleared in the **WK_STAT_1** and **WK_STAT_2** register
- An automatic transition PFM to PWM in the buck when the SBC is in SBC Stop mode (for more details please refer to **Chapter 6.4.2.1**)

The SPI status registers are updated at every falling edge of the INT pulse. All interrupt events are stored in the respective register (except the register **WK_LVL_STAT**) until the register is read and cleared via SPI command. A typical interrupt behavior is shown in **Figure 34**.

Interrupt function

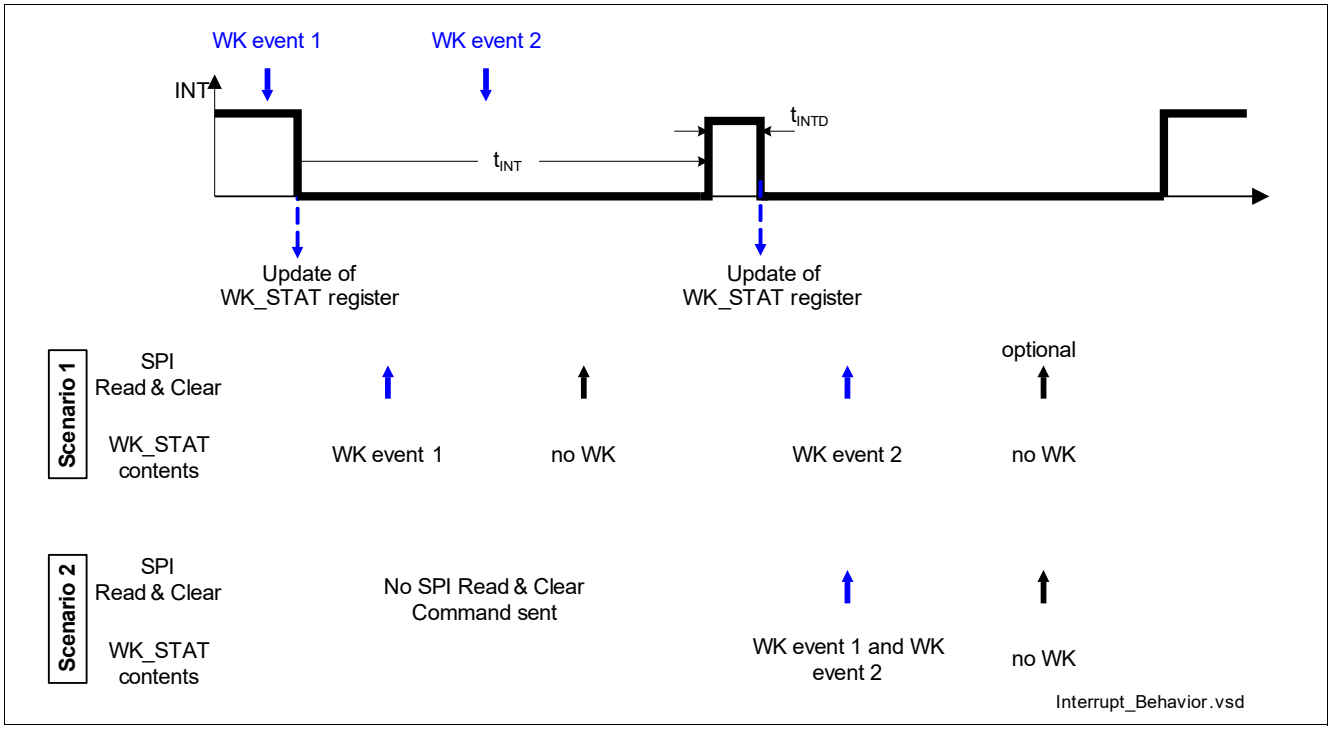

Figure 34 Interrupt signaling behavior

11.2 Electrical characteristics

Table 18 Interrupt output

T_j = -40°C to +150°C; V_S = 5.5 V to 28 V; SBC Normal mode; all voltages with respect to ground; positive current defined flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Interrupt output; pin INT							
INT HIGH output voltage	$V_{INT,H}$	0.8 × V_{CC1}	–	–	V	I_{INT} = -2 mA; INT = OFF	P_11.2.1
INT LOW output voltage	$V_{INT,L}$	–	–	0.2 × V_{CC1}	V	I_{INT} = 2 mA; INT = ON	P_11.2.2
INT pulse width	t_{INT}	–	100	–	µs	1)	P_11.2.3
INT pulse minimum delay time	t_{INTD}	–	100	–	µs	1) between consecutive pulses	P_11.2.4

1) Not subject to production test; tolerance defined by internal oscillator tolerance.

12 Fail-safe outputs and fail-safe input

12.1 Functional description

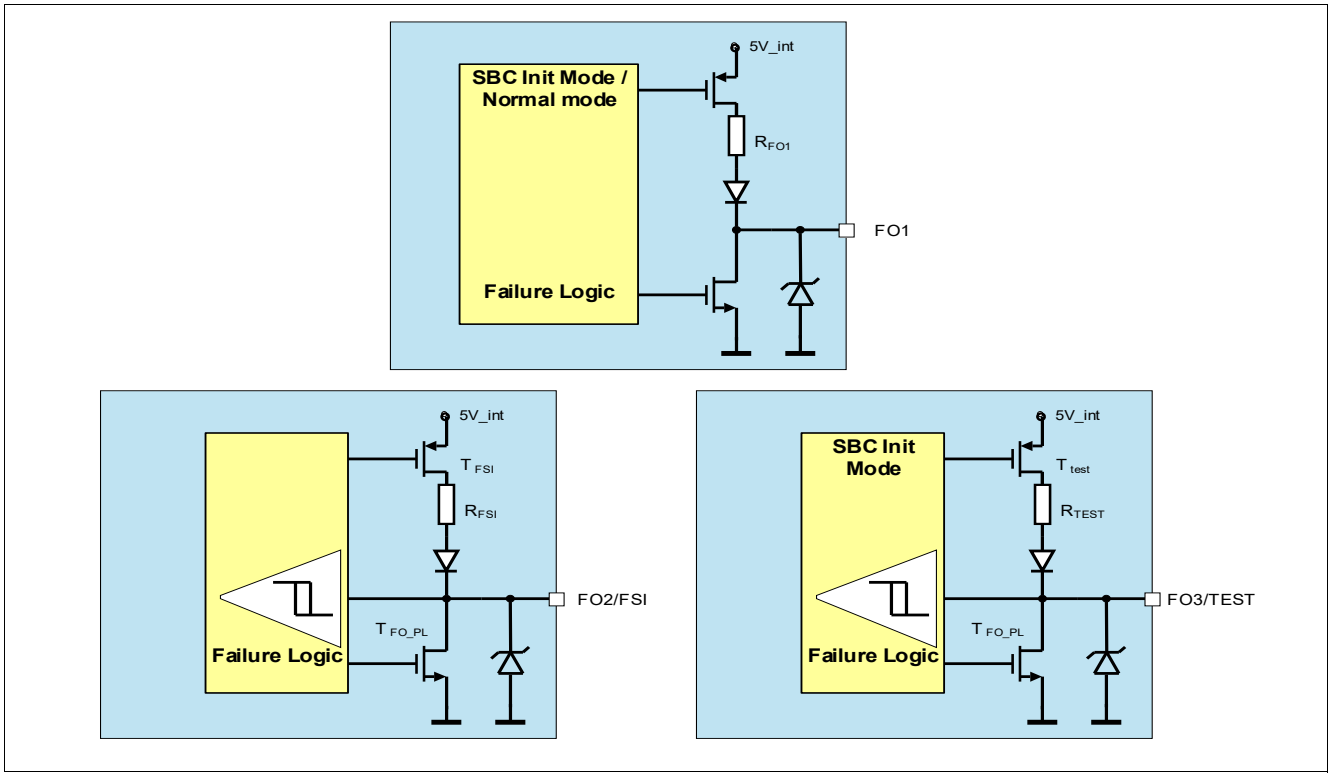

Figure 35 Fail-safe input and outputs block diagrams

The fail outputs consist of a failure logic block and three low-side switches. In case of a failure, the FO outputs are activated and the SPI bit **FO_ON_STATE** in the register **DEV_STAT** is set.

The fail outputs are activated under the following failure conditions:

Failure conditions

- After one or two watchdog trigger failures depending on configuration
- Thermal shutdown TSD2
- VCC1 short to GND
- RO clamped to HIGH

Configurations

It is possible to configure the FOx activation after a Watchdog trigger using the **CFG2** bit. Please refer to the **HW_CTRL** register.

In order to deactivate the fail output, the failure conditions (e.g. TSD2) must not be present anymore and the bit **FO_ON_STATE** needs to be cleared via SPI command. In case of watchdog fail, the fail output may only be disabled after the watchdog has been triggered successfully, i.e. the **WD_FAIL** bit must be cleared.

Note: The fail outputs are triggered for any of the above described failures and not only for failures leading to the Fail-Safe mode.

The three fail outputs are activated in parallel. The FO1 gives a static LOW signal in case of fail output activation. The FO2 provides a signal with a fixed frequency pulse and a duty cycle of 50% to generate an indicator signal. The FO3 provides a PWM signal with a fixed frequency and duty cycle of 20%, e.g. to generate a dimmed bulb signal.

Fail outputs

- FO1: Static fail output
- FO2: 1.25 Hz 50% duty cycle (typ.)
- FO3: 100 Hz 20% duty cycle (typ.)

Pull-up configuration

The integrated pull-up resistors are active if following conditions are fulfilled:

- FO1: SBC Init mode OR SBC Normal mode
- FO2: (SBC Init mode OR SBC Normal mode) AND **FSI_FO2** = 0
- FO3: SBC Init mode

12.2 Fail-safe input

The FO2 pin can be used as safety feature called fail-safe input.

A digital signal has to be generated by the microcontroller and the TLE9272QXV33 must detect the Low-to-High transition whitin $\mathbf{t_{FSI,W}}$ window time. The feature is enabled by default after power on. It can be disabled using the SPI command (**FSI_FO2**=1 on **HW_CTRL** register).

If there is no signal from the microcontroller, the TLE9272QXV33 sets the **FSI_FAIL** on **DEV_STAT** and both FO1 and FO3 are activated. The device remains in the same mode and neither reset nor interrupt will be triggered. The SPI status bit **FSI_FAIL** can only be cleared after a new rising edge on the FSI pin.

The **Figure 36** shows the timing diagram and level description of FSI input signal.

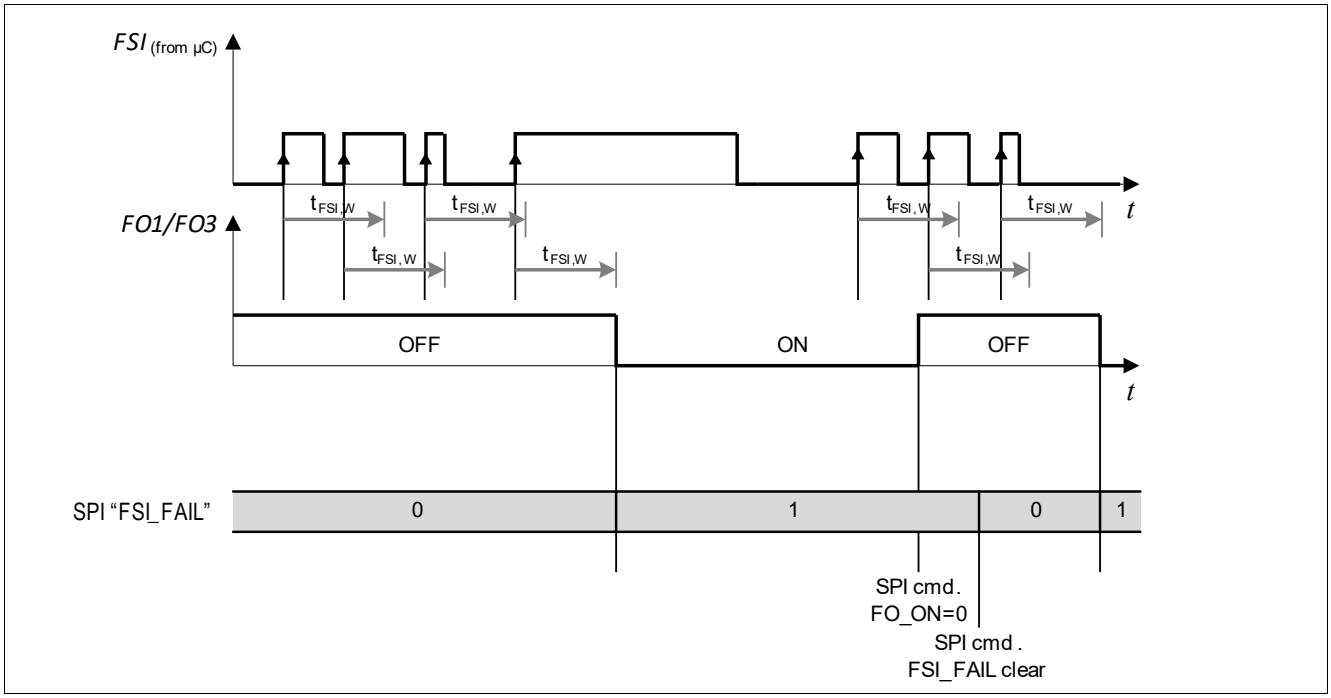

Figure 36 FSI timing diagram and level description

The fail-safe input feature is available only in SBC Normal mode.

12.3 Electrical characteristics

Table 19 Interrupt output

T_j = -40°C to +150°C; V_S = 5.5 V to 28 V; SBC Normal mode; all voltages with respect to ground; positive current defined flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Fail output; pin FO1, FO2, FO3							
FO LOW output voltage (active)	$V_{FO,L}$	–	0.6	1	V	I_{FO} = 5 mA	P_12.3.1
FO HIGH output current (inactive)	$I_{FO,H}$	0	–	2	µA	V_{FO} = 28 V	P_12.3.2
FO3 test mode select							
FO3/TEST HIGH-input voltage threshold	$V_{TEST,H}$	–	–	0.7 × V_{CC1}	V	–	P_12.3.28
FO3/TEST LOW-input voltage threshold	$V_{TEST,L}$	0.3 × V_{CC1}	–	–	V	–	P_12.3.29
FO3/Hysteresis of TEST input voltage	$V_{TEST,Hys}$	–	0.2 × V_{CC1}	–	V	1)	P_12.3.30
FO3/Pull-up resistance at pin TEST	R_{TEST}	–	5	–	kΩ	V_{TEST} = 0.2 × V_{CC1}	P_12.3.31
FO3/TEST input filter time	t_{TEST}	–	16	–	µs	1)	P_12.3.32
FO2/FSI input select							
FSI HIGH-input voltage threshold	$V_{FSI,H}$	–	–	0.7 × V_{CC1}	V	–	P_12.3.6
FSI LOW-input voltage threshold	$V_{FSI,L}$	0.3 × V_{CC1}	–	–	V	–	P_12.3.7
FSI hysteresis of input voltage	$V_{FSI,Hys}$	–	0.2 × V_{CC1}	–	V	1)	P_12.3.8
FSI pull-up resistance	R_{FSI}	–	40	–	kΩ	V_{FSI} = 0.2 × V_{CC1}	P_12.3.9
FSI input filter time	t_{FSI}	–	–	1.5	µs	1)	P_12.3.10
FSI window time	$t_{FSI,W}$	–	–	240	µs	1)	P_12.3.11
FO1							
FO1 pull-up resistance	R_{FO1}	–	40	–	kΩ	1) V_{FO1} = 0.2 × V_{CC1}	P_12.3.12

1) Not subject to production test; specified by design.

13 Supervision functions

13.1 Reset function

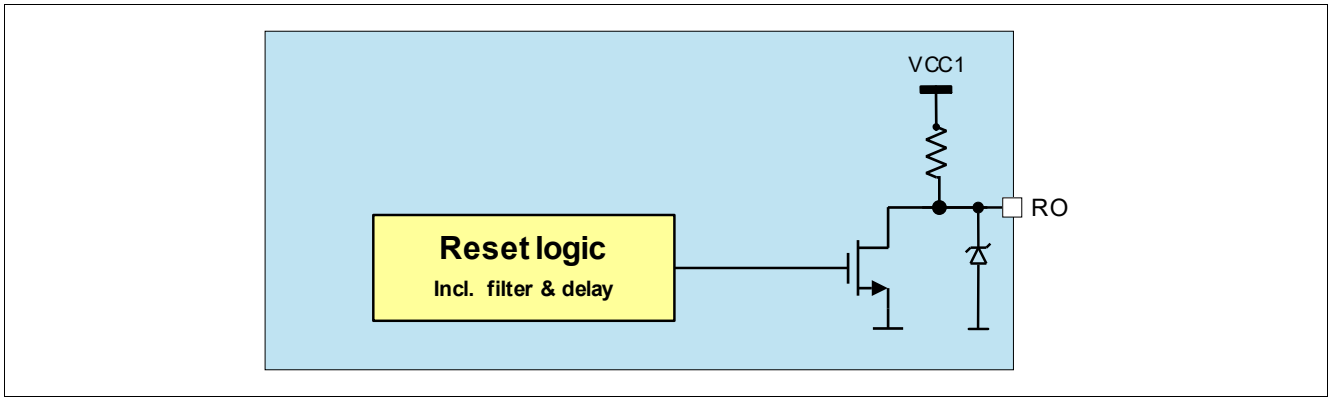

Figure 37 Reset block diagram

13.1.1 Reset output description

The reset output pin RO provides reset information to the microcontroller, for example, in the event that the output voltage has fallen below the undervoltage threshold $V_{RT1/2/3}$. In case of a reset event due to an undervoltage on buck regulator output voltage, the reset output RO is pulled to LOW after the filter time t_{RF} and stays LOW as long as the reset event is present plus a reset delay time t_{RD1}. When connecting the SBC to battery voltage, the reset signal remains LOW initially. When the buck regulator output voltage has reached the default reset threshold $V_{RT1,f}$, the reset output RO is released to HIGH after the reset delay time t_{RD1} (for a timing diagram, see also **Figure 4**). A reset can also occur due to a watchdog trigger failure. The reset threshold can be adjusted via SPI, the default reset threshold is $V_{RT1,f}$. The RO pin has an integrated pull-up resistor. If a reset is triggered, it will pull LOW for buck regulator output voltage (VCC1) ≥ 1 V and for VS ≥ $V_{POR,f}$. RO trigger timing regarding buck regulator undervoltage and watchdog trigger is shown in **Figure 38**.

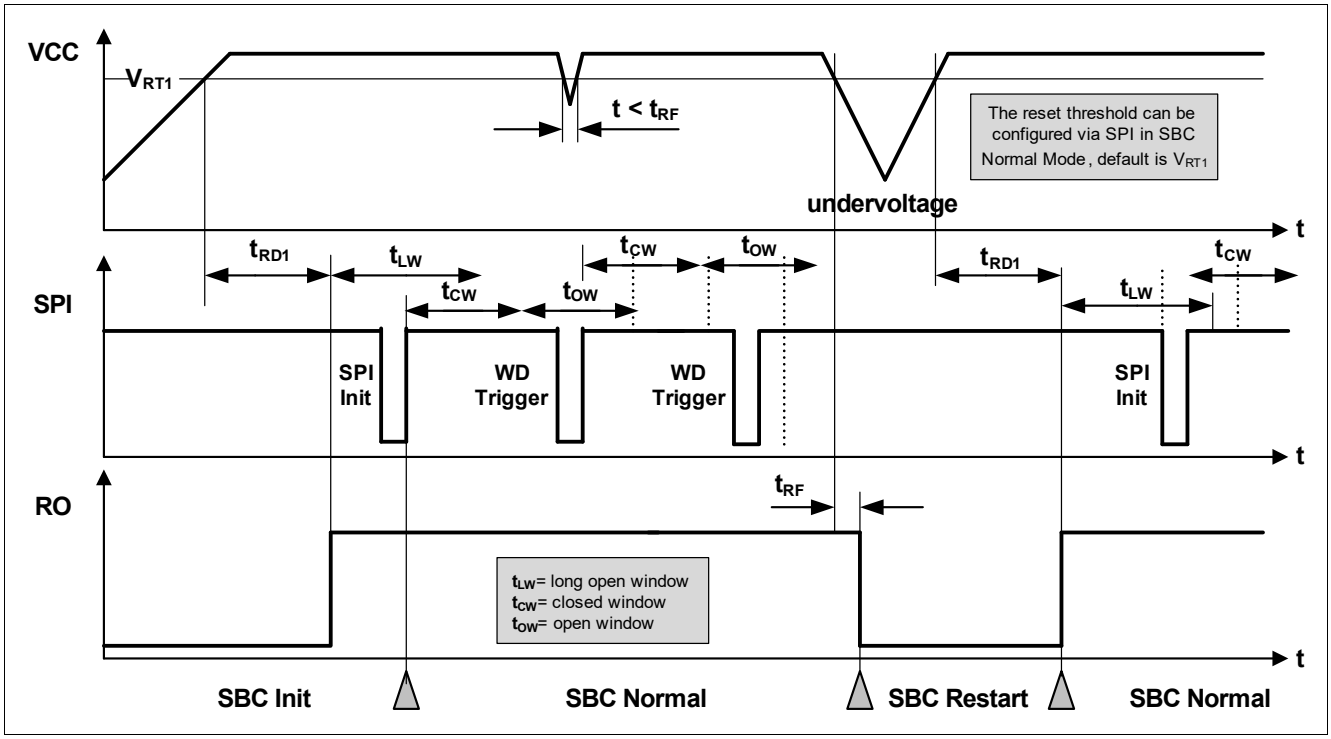

Figure 38 Reset timing diagram

13.1.2 Reset clamp to high

The RO pin is monitored internally. This feature detects if the RO pin is clamped to a high value from outside. The reset clamp to high is detected if the SBC generates a reset but the monitoring feedback senses a high level. The reset clamp is stored in **RO_CL_HIGH** bit on the **DEV_STAT** register.

The feature is available in SBC Normal, Stop and Restart mode. In SBC Sleep or Fail-Safe mode, the RO is not monitored because the buck regulator is disabled.

In case of watchdog failure, the reset clamp can be detected only if **VCC1_UV** on **SUP_STAT** register is 0 (no buck regulator undervoltage detected).

In case of a buck regulator undervoltage event, the reset clamp can be detected only after the buck regulator output voltage rises above the reset threshold.

13.1.3 Soft reset description

In SBC Normal and Stop mode, it is also possible to trigger a soft reset via an SPI command in order to bring the SBC into a defined state in case of failures. In this case, the microcontroller must send an SPI command and set the **MODE** bits to '11' in the **M_S_CTRL** register. As soon as this command becomes valid, the SBC is set back to SBC INIT mode and all SPI registers are set to their default values (see SPI **Chapter 14.5** and **Chapter 14.6**).
No Reset (RO) is triggered when the soft reset is executed.

Note: The device has to be in SBC Normal mode or SBC Stop mode when sending this command. Otherwise, it will be ignored.

13.2 Watchdog function

The watchdog is used to monitor the software execution of the microcontroller and to trigger a reset if the microcontroller stops serving the watchdog due to a lock up in the software.

Two different types of watchdog functions are implemented and can be selected via the bit **WD_WIN**:

- Time-out watchdog (default value)
- Window watchdog

The respective watchdog function can be selected and programmed in SBC Normal mode. The configuration remains unchanged in SBC Stop mode.

Refer to **Table 20** to match the SBC modes with the respective watchdog modes.

Table 20 Watchdog functionality by SBC modes

SBC mode	Watchdog mode	Remarks
INIT mode	Start with long open window	Watchdog starts with long open window after RO is released
Normal mode	WD programmable	Window watchdog, time-out watchdog
Stop mode	Watchdog is fixed or OFF	Watchdog OFF must be performed in SBC Normal mode
Sleep mode	OFF	SBC will start with long open window when entering SBC Normal mode
Restart mode	OFF	SBC will start with long open window when entering Normal mode
Fail-Safe mode	OFF	SBC will start with long open window when entering SBC Normal mode

The watchdog timing is programmed using an SPI command. As soon as the watchdog is programmed, the timer starts with the new setting and the watchdog must be served.The watchdog is triggered by sending a valid SPI-write command to the watchdog configuration register. The trigger SPI command is executed when the chip select input (CSN) becomes HIGH.

When coming from SBC Init or Restart mode the watchdog timer is always started with a long open window. The long open window (t_{LW}) allows the microcontroller to run its initialization sequences and then to trigger the watchdog via the SPI.

The watchdog timer period can be selected via the watchdog timing bit field (**WD_TIMER**) and is in the range of 10 ms to 1000 ms. This setting is valid for both watchdog types.

The following watchdog timer periods are available:

- WD setting 1: 10 ms
- WD setting 2: 20 ms
- WD setting 3: 50 ms
- WD setting 4: 100 ms
- WD setting 5: 200 ms (reset value)
- WD setting 6: 500 ms
- WD setting 7: 1000 ms

In case of a watchdog reset, SBC Restart mode is started and the SPI bits **WD_FAIL** are set. Once the RO goes HIGH again the watchdog immediately starts with a long open window and the SBC enters automatically SBC Normal mode.

In SBC Development mode, no reset is generated due to a watchdog failure, the watchdog is OFF.

After 3 consecutive resets due to watchdog failures, additional resets can be prevented by setting the **MAX_3_RST** bit on **WD_CTRL** register. The SBC will then remain in SBC Normal or Stop mode (the device will not reenter SBC Restart mode).

13.2.1 Time-out watchdog

The time-out watchdog is an easier and less secure watchdog than a window watchdog as the watchdog trigger can be done at any time within the configured watchdog timer period.

A correct watchdog service immediately results in starting a new watchdog timer period. Taking the tolerances of the internal oscillator into account leads to the safe trigger area as defined in **Figure 39**.

If the time-out watchdog period elapses, a watchdog reset is created by setting the reset output RO low and the SBC switches to SBC Restart mode.

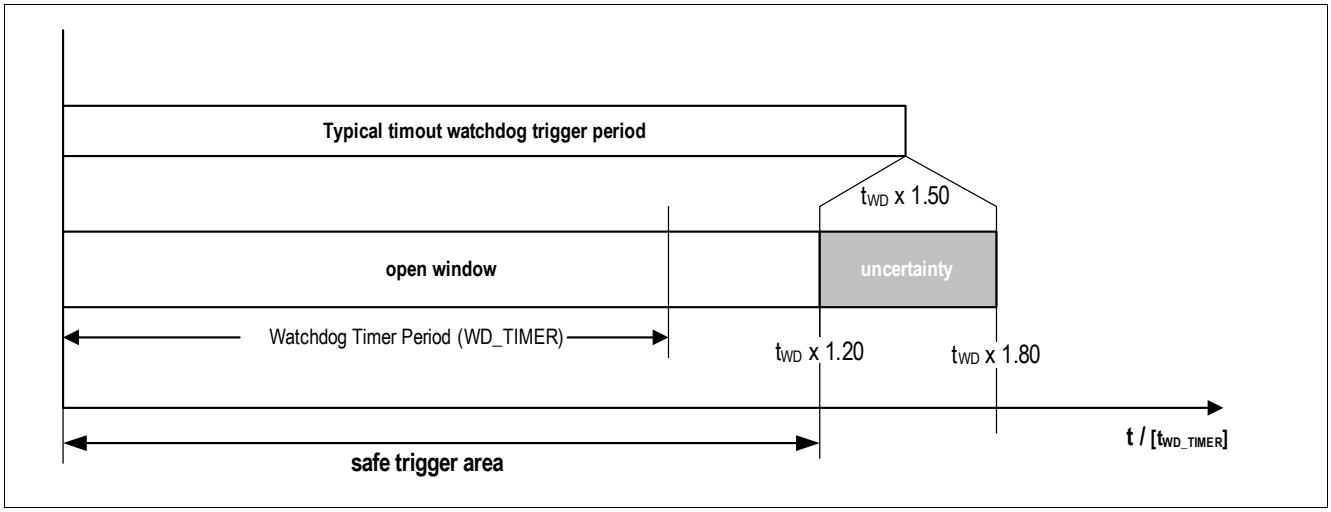

Figure 39 Time-out watchdog definitions

13.2.2 Window watchdog

Compared to the time-out watchdog, the characteristic of the window watchdog is that the watchdog timer period is divided between a closed and an open window. The watchdog must be triggered inside the open window.

A correct watchdog trigger results in starting the window watchdog period by a closed window followed by an open window.

The watchdog timer period is at the same time the typical trigger time and defines the middle of the open window.

Taking the oscillator tolerances into account leads to a safe trigger area of:

$t_{WD} \times 0.72 <$ safe trigger area $< t_{WD} \times 1.20$

The typical closed window is defined to a width of 60% of the selected window watchdog timer period. Taking the tolerances of the internal oscillator into account leads to the timings as defined in **Figure 40**.

A correct watchdog service immediately results in starting the next closed window.

Should the trigger signal meet the closed window or should the watchdog timer period elapse, then a watchdog reset is created by setting the reset output RO LOW. The SBC switches to SBC Restart mode.

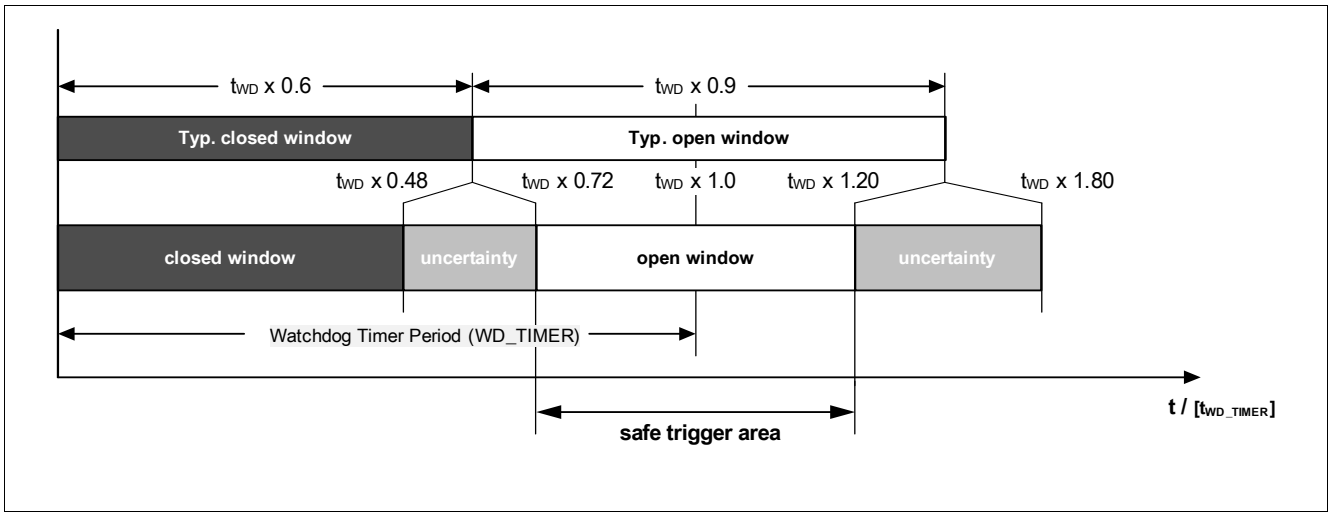

Figure 40 Window watchdog definitions

13.2.3 Watchdog setting check sum

A check sum bit is part of the SPI command to trigger the watchdog and to set the watchdog setting.

The sum of the 8 bits in the register **WD_CTRL** needs to be even. This is realized by either setting the bit **CHECKSUM** to “0” or “1”.

If the check sum is wrong the SPI command is ignored, i.e. the watchdog is not triggered or the settings are not changed and the bit **SPI_FAIL** is set.

The checksum is calculated by taking all 8 data bits into account.

$$\mathrm{CHKSUM} = \mathrm{Bit15} \oplus \ldots \oplus \mathrm{Bit8} \tag{13.1}$$

13.2.4 Watchdog during SBC Stop mode

The watchdog can be disabled for SBC Stop mode in SBC Normal mode. For safety reasons, there is a special sequence to be ensured in order to disable the watchdog. The sequence can be implemented only if the FSI feature is disabled (**FSI_FO2** = 1 on **HW_CTRL** register). The sequence is shown in **Figure 41**.

Two different bits (**WD_STM_ EN_0** and **WD_STM_ EN_1**) in the registers **WD_CTRL** and **WK_CTRL_1** need to be set.

If a sequence error occurs, then the bit **WD_STM_ EN_1** is cleared and the sequence has to be started again.

The watchdog can be enabled by triggering the watchdog in SBC Stop mode or by switching back to SBC Normal mode via SPI. In both cases, the watchdog will start with a long open window and the bits **WD_STM_ EN_1** and **WD_STM_ EN_0** are cleared. After the long open window, the watchdog has to be served as configured in **WD_CTRL** register.

*Note: The bit **WD_STM_ EN_0** will be cleared automatically when the sequence is started and it was “1” before.*

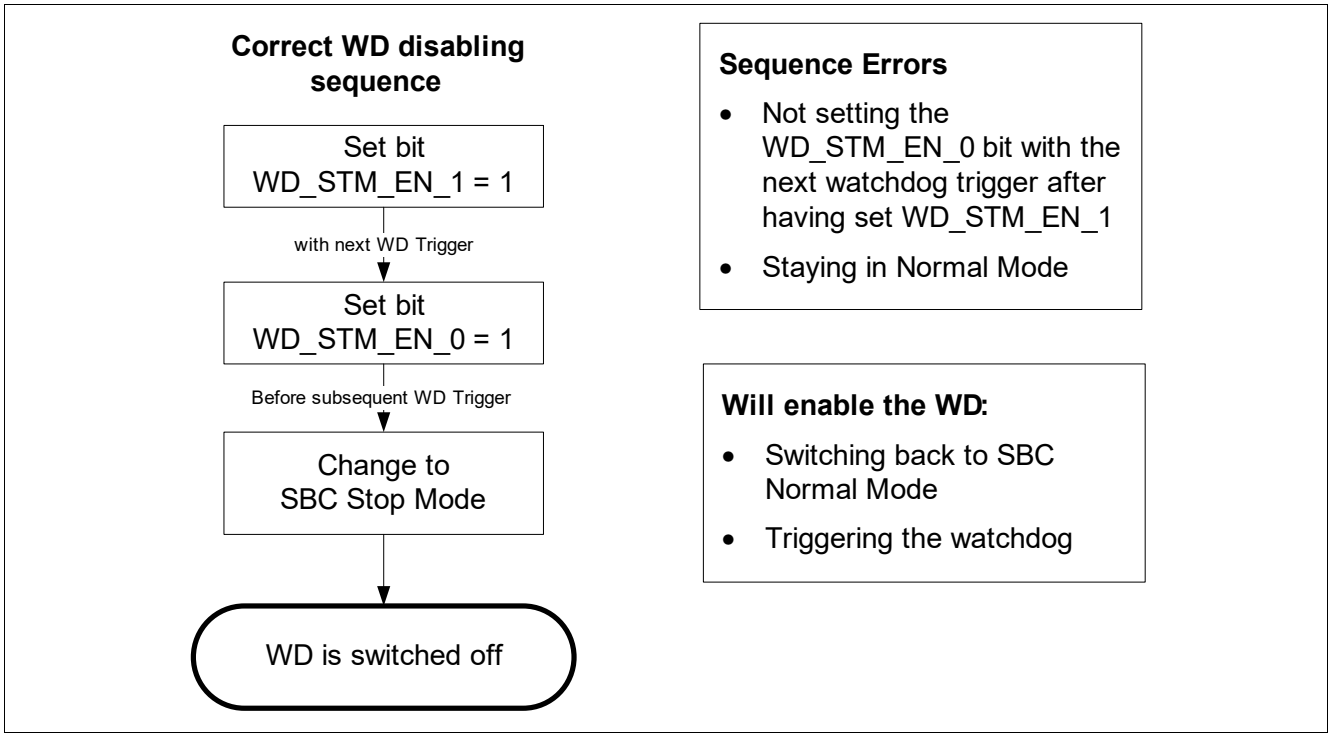

Figure 41 Watchdog disabling sequence in SBC Stop mode

13.2.4.1 WD start in SBC Stop mode due to bus wake

In SBC Stop mode, the WD can be disabled. In addition, a feature can be enabled to start the watchdog with any bus wake during SBC Stop mode. The feature is enabled by setting the bit **WD_EN_WK_BUS**. This bit can only be changed in SBC Normal mode and needs to be programmed before entering SBC Stop mode. It is not reset by the SBC. The sequence described in **Chapter 13.2.4** needs to be followed to disable the watchdog.

With this function enabled, the WD will be restarted by any wake event on CAN or LINx. The wake event on CAN or LINx will generate an interrupt and the RXDLINx or RXDCAN will be pulled to LOW. The watchdog starts with long open window. The watchdog can be triggered in SBC Stop mode or the SBC can be switched to SBC Normal mode. To disable the watchdog again, the SBC needs to be switched to SBC Normal mode and the sequence must be sent again. The sequence is shown in **Figure 42**.

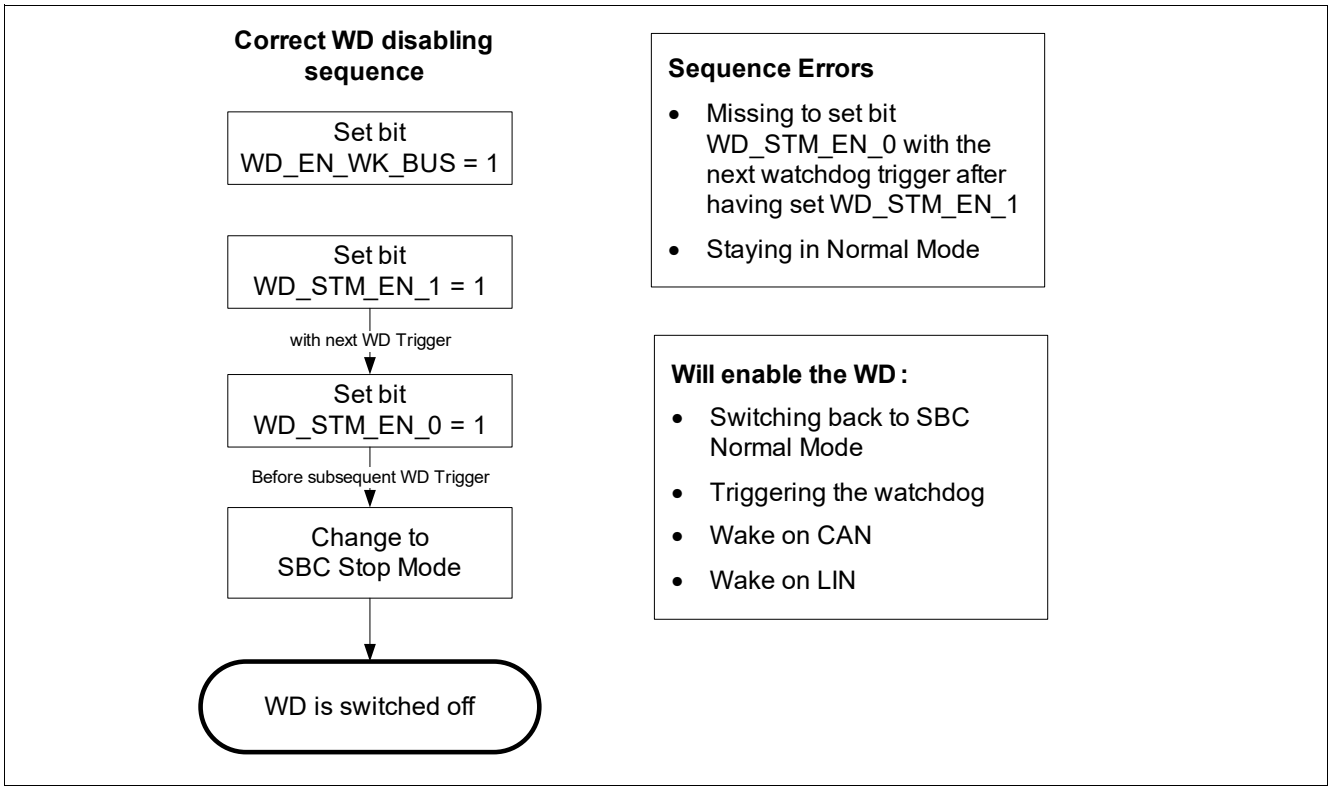

Figure 42 Watchdog disabling sequence (with wake via bus)

13.3 VS power on reset

When powering up, the device detects the VS power on reset when VS > $V_{POR,r}$, and the SPI bit **POR** is set to indicate that all SPI registers are set to POR default settings. The buck regulator starts up. The reset output is kept LOW and is only released when VCC1 has exceeded $V_{RT1,r}$ and after t_{RD1} has elapsed.

If VS < $V_{POR,f}$, an internal reset is generated and the SBC is switched OFF. The SBC will restart in INIT mode when VS > $V_{POR,r}$ rising. Timing behavior is shown in **Figure 43**.

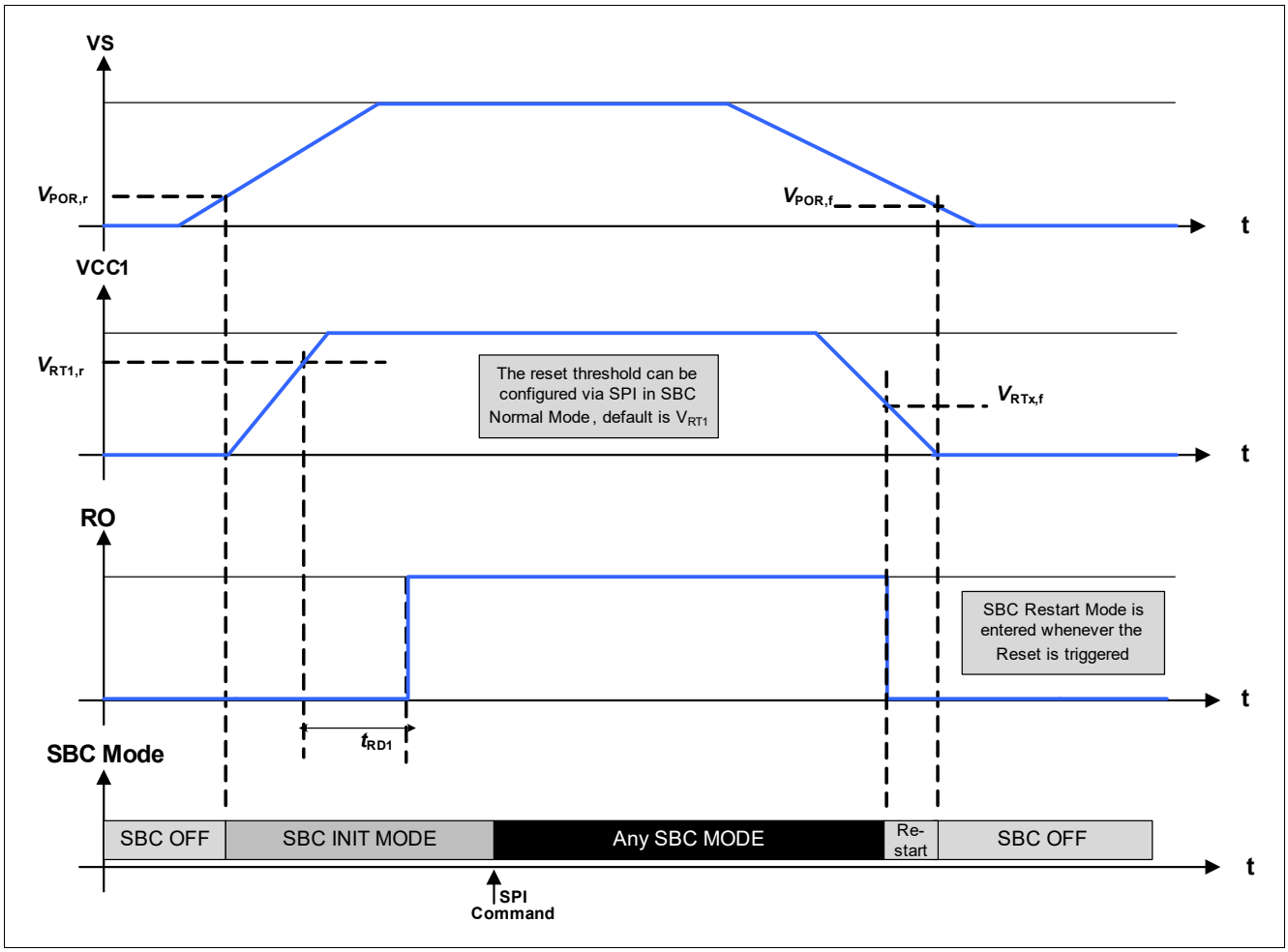

Figure 43 Ramp up/down example of supply voltage

13.4 Undervoltage VLIN

When the supply voltage VLIN reaches the undervoltage threshold ($V_{LIN,UVD}$) the SBC does the following actions:

- The SPI bit **VLIN_UV** is set. No other error bits are set. The bit can be cleared once the condition is no longer present
- LIN is set to LIN Receive-Only mode

For additional information, please refer to **Chapter 9.2.7**.

13.5 Buck regulator monitoring features

13.5.1 VCC1 undervoltage

As described in **Chapter 13.1**, and **Figure 44**, a reset will be triggered (RO pulled LOW) when the VCC1 output voltage reaches the undervoltage threshold (V_{RTx}) and the SBC enters SBC Restart mode. The bit **VCC1_UV** is set. The threshold can be configured using **VCC1_RT** bits.

The VCC1 undervoltage can be disabled by setting **VCC1_RT** to 11_B. With this configuration no reset is issued due to VCC1 undervoltage and no **VCC1_UV** bit is set. The under voltage detection has to be performed outside of the SBC when required.

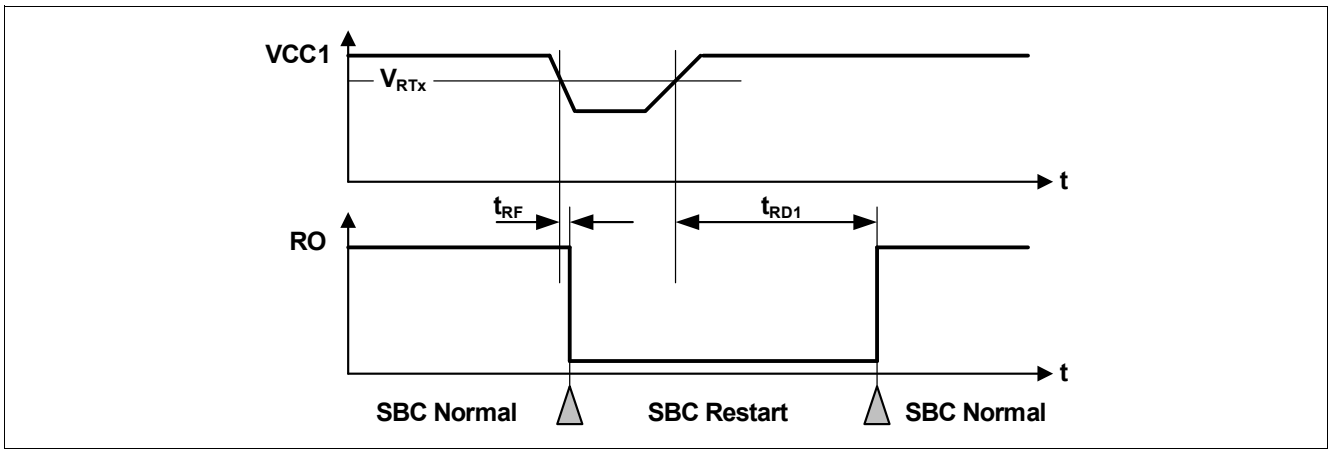

Figure 44 VCC1 undervoltage timing diagram

*Note: The **VCC1_UV** bit is not set in SBC Sleep and Fail-Safe mode as VCC1 is known to be 0 V in these cases.*

13.5.2 VCC1 overvoltage

For fail-safe reasons, a VCC1 overvoltage detection feature is implemented. It is active in SBC Init, Normal, and Stop mode.

If VCC1 voltage exceeds the $V_{CC1,OV,r}$ threshold, the SBC triggers following actions:

- The bit **VCC1_OV** is always set
- If the bit **VCC1_OV_ RST** is set, SBC Restart mode is entered. A reset event is generated. The SBC exits the SBC Restart mode and SBC Normal mode is resumed after the VCC1 over voltage is not present anymore (see also **Figure 45**)

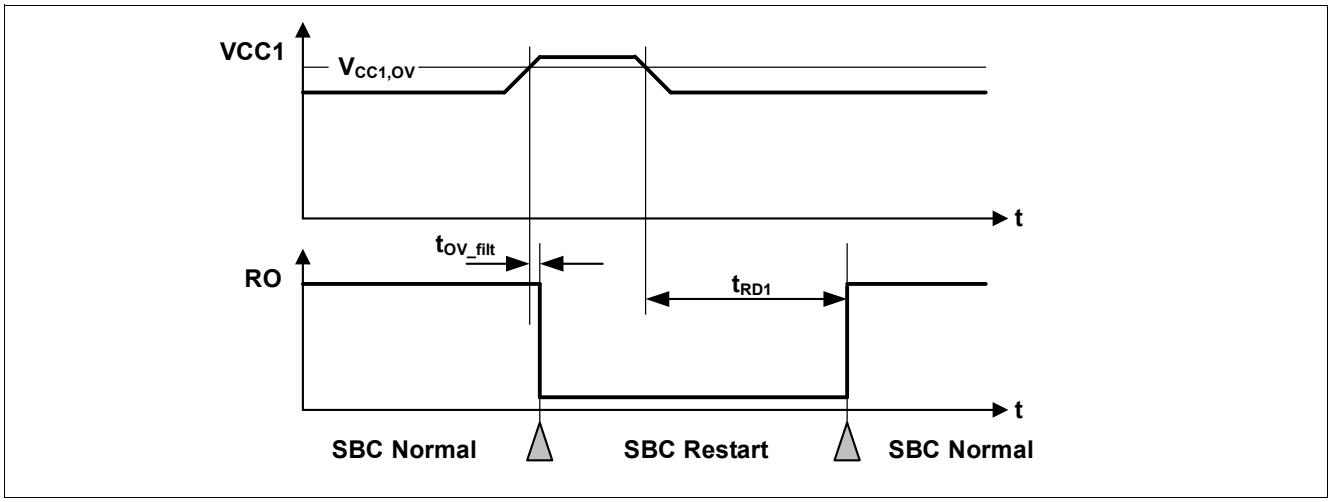

Figure 45 VCC1 overvoltage timing diagram

13.5.3 VCC1 short circuit

The short circuit protection feature for buck regulator is implemented as follows:

- When VCC1 stays below the undervoltage threshold VRTx for more than $t_{VCC1,SC}$ and at the same time VS is above the threshold V_{S,UV_TO}, the SBC enters SBC Fail-Safe mode and turns OFF the buck regulator. The FOx are activated and the SPI status bits **VCC1_SC**, **VCC1_UV** and **BCK_SH** are set. The SBC can be reactivated by a wake event on CAN, LINx or WK

13.5.4 SMPS status register

The TLE9272QXV33 has a dedicated SMPS status register which provides information about the buck and boost regulators. No SBC mode changes and no transceivers configurations changes are triggered when an **SMPS_STAT** register bit is set.

13.6 VCC2 undervoltage

An undervoltage warning is implemented for VCC2 as follows:

- In case VCC2 drops below the $V_{CC2,UV,f}$ threshold for t > $t_{VCC2,UV}$, the SPI bit **VCC2_UV** is set and can be only cleared via SPI

*Note: The **VCC2_UV** flag is not set during turn-on or turn-off of V_{CC}.*

13.7 VCAN undervoltage

The CAN module has a dedicated feature to detect undervoltage condition on the VCAN supply pin. Refer to **Chapter 8.2.7** for additional information.

13.8 Thermal protection

Three independent and different thermal protection features are implemented in the SBC according to the system impact:

- Individual thermal shutdown of specific blocks
- Temperature prewarning of buck regulator
- SBC thermal shutdown due to buck regulator overtemperature

13.8.1 Individual thermal shutdown

As a first-level protection measure, the output stages VCC2, CAN and LINx are independently switched OFF when the respective block reaches the temperature threshold **T_{jTSD1}**. Then the **TSD1** bit is set. This bit can only be cleared via SPI once the overtemperature is not present anymore. Regardless of the SBC mode, the thermal shutdown protection is only active when the respective block is ON.

The different modules behave as follows:

- VCC2: It is switched OFF and the control bits **VCC2_ON** are cleared. The status bit **VCC2_OT** is set. Once the over temperature condition is not present anymore, the VCC2 must be reconfigured by SPI. The thermal protection in VCC2 is available only in SBC Normal mode or SBC Stop mode with watchdog activated
- CAN: The transmitter is disabled and stays in CAN Normal mode acting like CAN Receive-Only mode. The status bits **CAN_FAIL** = 01_B are set. Once the overtemperature condition is not present anymore, the CAN transmitter is automatically switched on
- LIN1, LIN2, LIN3: The transmitter is disabled and stays in LIN Normal mode acting like LIN Receive-Only mode. The respective status bits LINx_FAIL are set to 01_B. Once the overtemperature condition is not present anymore, the LIN transmitter is automatically switched on

Note: The diagnosis bits are not cleared automatically and have to be cleared via SPI once the overtemperature condition is not present anymore.

13.8.2 Temperature prewarning

As a next level of thermal protection, a temperature prewarning is implemented if the buck regulator reaches the temperature prewarning threshold **T_{jPW}**. The status bit **TPW** is set. This bit can only be cleared via SPI once the overtemperature is not present anymore. Regardless of the SBC mode the temperature prewarning is active only if the buck converter is ON.

13.8.3 SBC thermal shutdown

As a highest level of thermal protection, a temperature shutdown of the SBC occurs if the buck regulator reaches the thermal shutdown temperature threshold **T_{jTSD2}**. The temperature protection is available only in case that the buck regulator works in PWM modulation. The thermal protection is not available if the buck regulator works in PFM mode.

Once a TSD2 event is detected, SBC Fail-Safe mode is entered for at least **t_{TSD2}**. The default wake sources (CAN, LINx, WK pin) are enabled together with the fail-safe outputs.

When a TSD2 event is detected, the status bit **TSD2** is set. This bit can only be cleared via SPI in SBC Normal mode once the overtemperature is not present anymore. Regardless of the SBC mode the thermal shutdown is only active if the buck converter is ON.

13.9 Electrical characteristics

Table 21 Electrical specification

T_j = -40°C to +150°C; V_S = 5.5 V to 28 V; SBC Normal mode; all voltages with respect to ground; positive current defined flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
VCC1 monitoring, reset generator; pin RO TLE9272QXV33							
Reset threshold voltage RT1,f	$V_{RT1,f}$	2.97	3.04	3.14	V	Default setting; V_{CC1} falling	P_13.9.20
Reset threshold voltage RT1,r	$V_{RT1,r}$	3.04	3.1	3.2	V	Default setting; V_{CC1} rising	P_13.9.23
Reset threshold voltage RT2,f	$V_{RT2,f}$	2.44	2.57	2.64	V	SPI option; V_{CC1} falling	P_13.9.28
Reset threshold voltage RT2,r	$V_{RT2,r}$	2.51	2.64	2.71	V	SPI option; V_{CC1} rising	P_13.9.29
Reset threshold voltage RT3,f	$V_{RT3,f}$	1.98	2.08	2.18	V	SPI option; $V_S \geq 4V$; V_{CC1} falling	P_13.9.30
Reset threshold voltage RT3,r	$V_{RT3,r}$	2.05	2.15	2.24	V	SPI option; $V_S \geq 4V$; V_{CC1} rising	P_13.9.31
Reset threshold hysteresis	$V_{RT,hys}$	15	66	130	mV	–	P_13.9.32
V_{CC1} overvoltage detection threshold	$V_{CC1,OV,r}$	3.4	3.55	3.6	V	Rising V_{CC1}	P_13.9.70
V_{CC1} overvoltage detection hysteresis	$V_{CC1,OV,hys}$	15	66	130	mV	–	P_13.9.8
V_{CC1} short to GND filter time	$t_{VCC1,SC}$	–	4	–	ms	2)	P_13.9.11
V_{CC1} overvoltage filter time	$t_{OV,filt}$	–	7	–	µs	2)	P_13.9.58
VS threshold for V_{CC1} undervoltage time out detection	V_{S,UV_TO}	3.7	4	4.4	V	VS needs to be above to activate VCC1_SC time-out	P_13.9.9
Reset LOW output voltage	$V_{RO,HIGH}$	–	0.2	0.4	V	I_{RO} = 1 mA for $V_{CC1} \geq 1$ V	P_13.9.14
Reset HIGH output voltage	$V_{RO,LOW}$	0.7 × $V_{CC1µC}$	–	$V_{CC1µC}$ + 0.3 V	V	I_{RO} = -20 µA	P_13.9.15
Reset pull-up resistor	R_{RO}	10	20	40	kΩ	V_{RO} = 0 V	P_13.9.16

Table 21 Electrical specification (cont'd)

T_j = -40°C to +150°C; V_S = 5.5 V to 28 V; SBC Normal mode; all voltages with respect to ground; positive current defined flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Reset filter time	t_{RF}	4	10	26	µs	2) $V_{CC1} < V_{RT1x}$ to RO = LOW	P_13.9.17
Reset delay time	t_{RD1}	1.5	2	2.5	ms	1)2)	P_13.9.18
VCC2 monitoring							
VCC2 undervoltage threshold (falling)	$V_{CC2,UV,f}$	4.5	–	4.75	V	VCC2 falling	P_13.9.21
VCC2 undervoltage threshold (rising)	$V_{CC2,UV,r}$	4.6	–	4.9	V	VCC2 rising	P_13.9.55
VCC2 undervoltage detection hysteresis	$V_{CC2,UV,hys}$	20	100	250	mV	–	P_13.9.56
VCC2 undervoltage Filter time	$t_{VCC2,UV}$	–	7	–	µs	2)	P_13.9.22
Watchdog generator							
Long open window	t_{LW}	240	300	360	ms	4)	P_13.9.34
Internal oscillator	f_{CLKSBC}	0.8	1.0	1.2	MHz	–	P_13.9.24
Minimum waiting time during SBC Fail-Safe mode							
Min. waiting time in fail-safe	$t_{FS,min}$	–	100	–	ms	2)3)	P_13.9.41
Power on reset, over-/undervoltage protection							
VS power ON reset rising	$V_{POR,r}$	4.5	–	5	V	V_S increasing	P_13.9.25
VS power ON reset falling	$V_{POR,f}$	–	–	3	V	V_S decreasing BOOST=OFF	P_13.9.26
VLIN undervoltage detection threshold	$V_{LIN,UVD}$	4.8	–	5.5	V	Hysteresis included	P_13.9.27
VLIN undervoltage detection hysteresis	$V_{LIN,UVD,hys}$	–	200	–	mV	4)	P_13.9.57
Overtemperature shutdown[4)]							
Thermal prewarning ON temperature	T_{jPW}	125	145	165	°C	4)	P_13.9.37
Thermal shutdown TSD1	T_{jTSD1}	165	185	200	°C	4)	P_13.9.38
Thermal shutdown TSD2	T_{jTSD2}	165	185	200	°C	4)	P_13.9.39
Deactivation time after thermal shutdown TSD2	t_{TSD2}	–	1	–	s	2)	P_13.9.40

1) The reset delay time will start when V_{CC1} crosses above the selected V_{rtx} threshold.
2) Not subject to production tests. Tolerance defined by internal oscillator tolerance.
3) This time applies for all failure entries except a device thermal shutdown (TSD2 has a 1 s waiting time t_{TSD2}).
4) Not subject to production test, specified by design.

14 Serial Peripheral Interface

14.1 SPI description

The 16-bit wide Control Input Word is read via the data input SDI, which is synchronized with the clock input CLK provided by the microcontroller. The output word appears synchronously at the data output SDO (see **Figure 46**).

The transmission cycle begins when the chip is selected by the input CSN (Chip Select Not), LOW active. After the CSN input returns from LOW to HIGH, the word that has been read is interpreted according to the content. The SDO output switches to tristate status (HIGH impedance) at this point, thereby releasing the SDO bus for other use.

The state of SDI is shifted into the input register with every falling edge on CLK. The state of SDO is shifted out of the output register after every rising edge on CLK. The SPI of the SBC is not daisy chain capable.

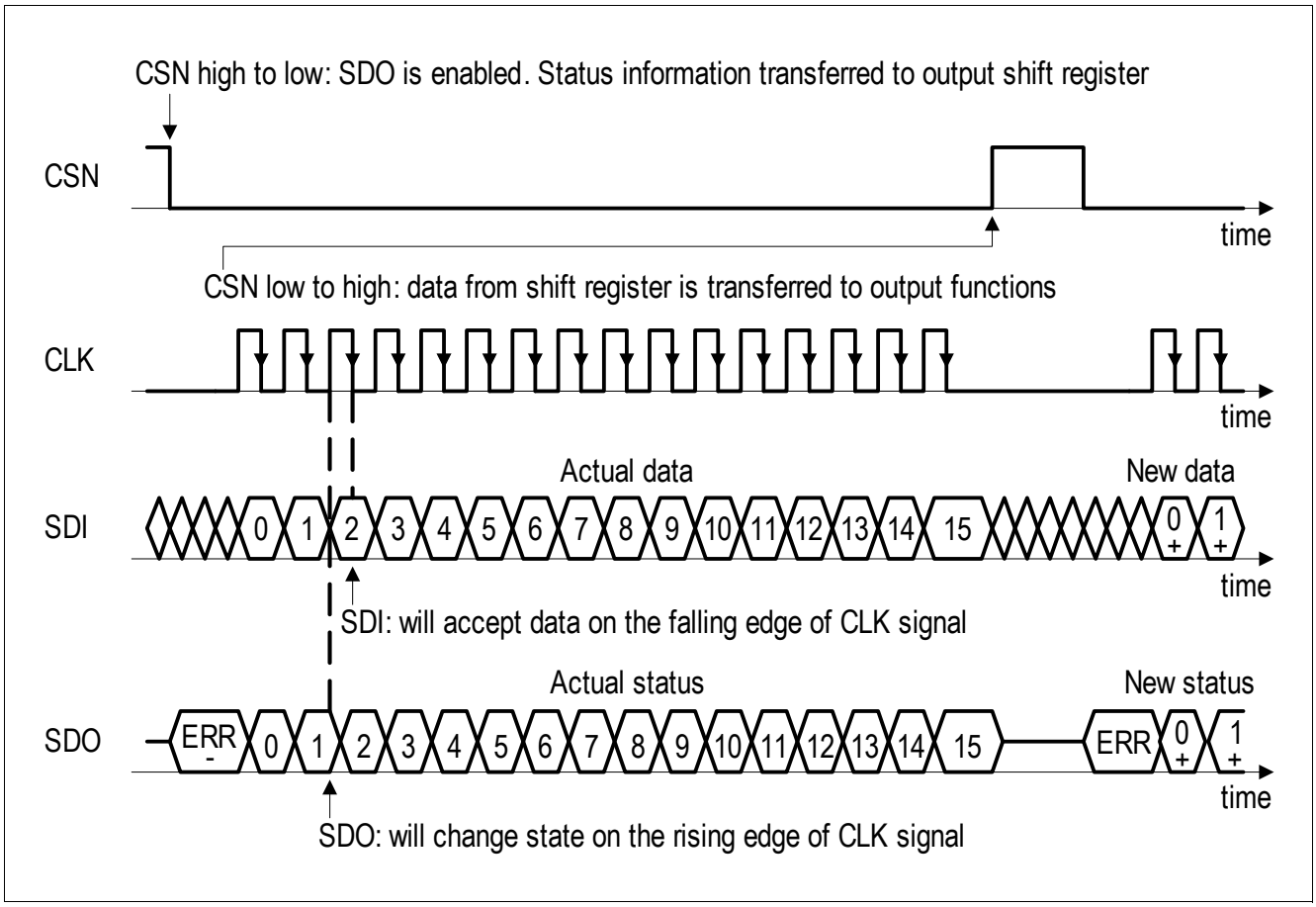

Figure 46 SPI data transfer timing (note the reversed order of LSB and MSB shown in this figure compared to the register description)

14.2 Failure signalization in the SPI data output

When the microcontroller sends a wrong SPI command to the SBC, the SBC ignores the information. Wrong SPI commands can be either an invalid control command requesting to go to an SBC mode which is not allowed by the state machine, for example from SBC Stop mode to SBC Sleep mode. In this case the diagnosis bit '**SPI_FAIL**' is set. This bit can be only reset by actively clearing it using an SPI command.

Invalid SPI commands are listed below:

- Illegal state transitions:
  Going from SBC Stop to SBC Sleep mode. In this case, the SBC enters in addition the SBC Restart mode.
  Trying to go to SBC Stop or SBC Sleep mode from SBC Init mode. In this case, the SBC enters SBC Normal mode
- Attempting to change the watchdog settings during Stop mode ;.
  Only WD trigger, returning to SBC Normal mode, select Software Reset, set to SBC Stop mode to return from PWM to PFM when automatic buck mode transition has happened and read and clear commands are valid SPI commands in SBC Stop mode
- Attempt to go to Sleep mode when all bits in the **BUS_CTRL_1** and **WK_CTRL_2** registers are cleared. In this case, the **SPI_FAIL** bit is set and the SBC enters Restart mode.
  Note that at least one wake source must be activated in order to avoid a deadlock situation in Sleep mode, i.e. the SBC would not be able to wake up anymore. There is no signalling or failure handling for the attempt to go to SBC Stop mode when all bits in the registers **BUS_CTRL_1** and **WK_CTRL_2** are cleared because the microcontroller can leave this mode via SPI

Signalization of the ERR flag in the SPI data output (see Figure 46):

In addition, the number of received input clocks is supervised to be 0- or 16 clock cycles and the input word is discarded in case of a mismatch (0 clock cycle to enable ERR signalization). Both errors - 0 bit and 16 bit CLK mismatch or CLK high during CSN edges - are flagged in the following SPI output by a HIGH at the data output (SDO pin, bit ERR) before the first rising edge of the clock is received. The error logic also recognizes if CLK was HIGH during CSN edges. The complete SPI command is ignored in these cases.

Note: It is also possible (no ERR flag is set) to quickly check for the ERR flag without sending any data bits. i.e. no SPI clocks are sent in this case.

14.3 SPI programming

For the TLE9272QXV33, 7 bits are used for the address selection (6...0). Bit 7 is used to decide between Read_Only and Read_Clear for the status bits, and between Write and Read Only for configuration bits. For the actual configuration and status information, 8 data bits (BIT15...8) are used.

Writing, clearing and reading is done byte wise. SPI configuration and status bits are not cleared automatically and must be cleared by the microcontroller, e.g. if the TSD2 was set due to overtemperature. The configuration bits will be partially automatically cleared by the SBC - please refer to the individual registers description for detailed information. During SBC Restart mode or Sleep mode or Fail-Safe mode, the SPI communication is ignored by the SBC, i.e. it is not interpreted.

There are two types of SPI registers:

- Control registers: The registers used to configure the SBC, e.g. SBC mode, watchdog trigger, etc.
- Status registers: The registers used to signal the status of the SBC, e.g. wake-up events, warnings, failures, etc.

For the status registers, the requested information is given in the same SPI command in DO.
For the control registers, the status of the respective bit is also shown in the same SPI command, but if the setting is changed this is only shown with the next SPI command (it is only valid after CSN HIGH) of the same register.

The SBC status information from the SPI status registers is transmitted in a compressed format with each SPI response on SDO in the so-called Status Information Field register (see also **Figure 47**). The purpose of this register is to quickly signal the information to the microcontroller if there was a change in one of the SPI status registers. In this way, the microcontroller does not need to constantly read all the SPI status registers but only those registers that have changed. Each bit in the Status Information Field represents an SPI status register (see **Table 22**). As soon as one bit is set in one of the status registers, the respective bit in the Status Information Field register is set. The register **WK_LVL_STAT** is not included in the status Information field. This is shown in **Table 22**.

For example, if bit 0 in the Status Information Field is set to 1, one or more bits of the register 100 0001 (**SUP_STAT**) are set to 1. Then this register needs to be read in a second SPI command. The bit in the Status Information Field will be set to 0 when all bits in the register 100 0001 are set back to 0.

Table 22 Status information field

Status information bit	Symbol address bit	Status register
0	100 0001	**SUP_STAT**: Supply status - V_S fail, V_{CCx} fail, POR
1	100 0010	**THERM_STAT**: Thermal protection status
2	100 0011	**DEV_STAT**: Device status - mode before wake, WD fail, SPI fail, failure
3	100 0100	**BUS_STAT_1**: Bus failure status: CAN, LIN
4	100 0101	**BUS_STAT_2**: Bus failure status: CAN, LIN
5	100 0110	**WK_STAT_1**: Wake source status
6	100 0111	**WK_STAT_2**: Wake source status
7	100 1100	**SMPS_STAT**: SMPS status

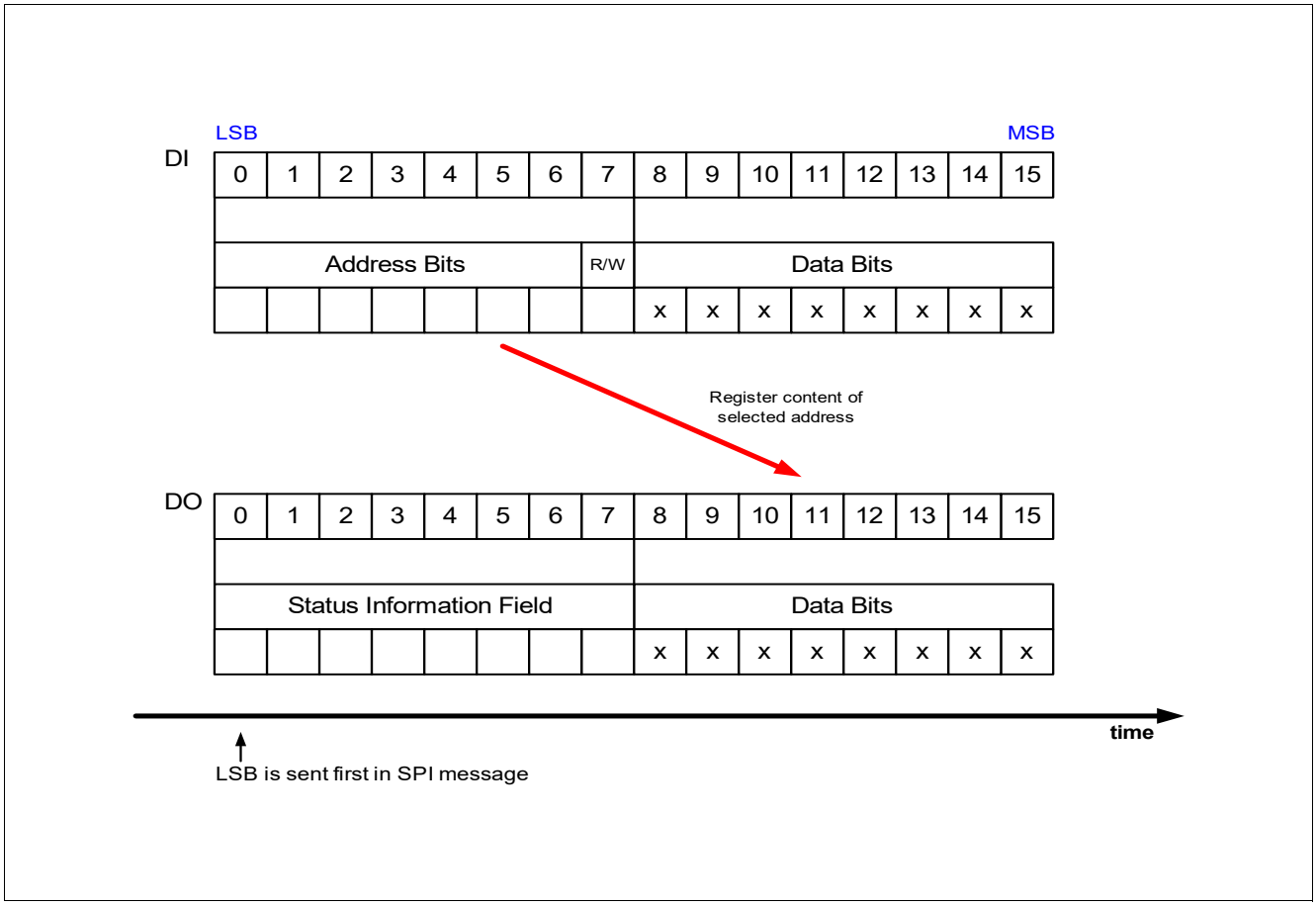

Figure 47 SPI operation mode

14.4 SPI bit mapping

Figure 48 and show the mapping of the SPI bits and the respective registers.

The control registers ‘000 0001’ to ‘001 1110’ are READ/WRITE register. Depending on bit 7 the bits are only read or also written. The new setting of the bit after write can be seen with a new read / write command.

The registers ‘100 0001’ to ‘111 1110’ are Status Registers and can be read or read with clearing the bit (if possible) depending on bit 7. To clear a data byte of one of the Status Registers, bit 7 must be set to 1. The register **WK_LVL_STAT** is an exception as it shows the actual voltage level at the respective WK pin (LOW/HIGH) and can thus not be cleared.

When changing to a different SBC mode, certain configurations and status bits will be cleared:

- The SBC mode bits are updated to the actual status, e.g. when returning to Normal mode
- In Sleep mode, the CAN and LIN control bits will be changed to CAN/LIN wake capable if they were ON before. FOx will stay activated if it was triggered before
- VCC2 can be active in Low power mode (Stop/Sleep). The configuration can only be done in Normal mode. Diagnosis is active (UV, OT)
- Depending on the respective configuration, CAN/LIN transceivers will be either OFF, woken or still wake capable

	Register Short Name	7	6...0
		Read-Only (1)	Address A6...A0
Control Registers	**CONTROL REGISTERS**		
	M_S_CTRL	read/write	0000001
	HW_CTRL	read/write	0000010
	WD_CTRL	read/write	0000011
	BUS_CTRL_1	read/write	0000100
	BUS_CTRL_2	read/write	0000101
	WK_CTRL_1	read/write	0000110
	WK_CTRL_2	read/write	0000111
	WK_PUPD_CTRL	read/write	0001000
	TIMER1_CTRL	read/write	0001100
	SYS_STATUS_CTRL	read/write	0011110
Status Registers	**STATUS REGISTERS**		
	SUP_STAT	read/clear	1000001
	THERM_STAT	read/clear	1000010
	DEV_STAT	read/clear	1000011
	BUS_STAT_1	read/clear	1000100
	BUS_STAT_2	read/clear	1000101
	WK_STAT_1	read/clear	1000110
	WK_STAT_2	read/clear	1000111
	WK_LVL_STAT	read	1001000
	SMPS_STAT	read/clear	1001100
	FAM_PROD_STAT	read	1111110

Figure 48 SPI bit mapping

	Register Short Name	15	14	13	12	11	10	9	8	7	6...0
		Data Bit 15...8								Read-Only (1)	Address A6...A0
		D7	D6	D5	D4	D3	D2	D1	D0		
Control Registers	**CONTROL REGISTERS**										
	M_S_CTRL	MODE_1	MODE_0	reserved	VCC2_ON_1	VCC2_ON_0	VCC1_OV_RST	VCC1_RT_1	VCC1_RT_0	read/write	0000001
	HW_CTRL	FSI_FO2	PWM_TLAG	FO_ON	PWM_BY_WK	PWM_AUTO	BOOST_V	BOOST_EN	CFG2	read/write	0000010
	WD_CTRL	CHECKSUM	WD_STM_EN_0	WD_WIN	WD_EN_WK_BUS	MAX_3_RST	WD_TIMER_2	WD_TIMER_1	WD_TIMER_0	read/write	0000011
	BUS_CTRL_1	LIN_FLASH	LIN_LSM	LIN_TXD_TO	LIN1_1	LIN1_0	reserved	CAN_1	CAN_0	read/write	0000100
	BUS_CTRL_2	reserved	reserved	reserved	LIN3_1	LIN3_0	reserved	LIN2_1	LIN2_0	read/write	0000101
	WK_CTRL_1	reserved	TIMER1_WK_EN	reserved	reserved	reserved	WD_STM_EN_1	reserved	reserved	read/write	0000110
	WK_CTRL_2	reserved	reserved	reserved	reserved	reserved	reserved	reserved	WK_EN	read/write	0000111
	WK_PUPD_CTRL	reserved	reserved	reserved	reserved	reserved	reserved	WK_PUPD_1	WK_PUPD_0	read/write	0001000
	TIMER1_CTRL	reserved	reserved	reserved	reserved	reserved	TIMER1_PER_2	TIMER1_PER_1	TIMER1_PER_0	read/write	0001100
	SYS_STATUS_CTRL	SYS_STAT_7	SYS_STAT_6	SYS_STAT_5	SYS_STAT_4	SYS_STAT_3	SYS_STAT_2	SYS_STAT_1	SYS_STAT_0	read/write	0011110
Status Registers	**STATUS REGISTERS**										
	SUP_STAT	POR	VLIN_UV	VCC1_OV	VCC2_OT	VCC2_UV	VCC1_SC	reserved	VCC1_UV	read/clear	1000001
	THERM_STAT	reserved	reserved	reserved	reserved	reserved	TSD2	TSD1	TPW	read/clear	1000010
	DEV_STAT	DEV_STAT_1	DEV_STAT_0	RO_CL_HIGH	FSI_FAIL	WD_FAIL_1	WD_FAIL_0	SPI_FAIL	FO_ON_STATE	read/clear	1000011
	BUS_STAT_1	reserved	LIN1_FAIL_1	LIN1_FAIL_0	reserved	reserved	CAN_FAIL_1	CAN_FAIL_0	VCAN_UV	read/clear	1000100
	BUS_STAT_2	reserved	reserved	reserved	LIN3_FAIL_1	LIN3_FAIL_0	LIN2_FAIL_1	LIN2_FAIL_0	reserved	read/clear	1000101
	WK_STAT_1	PFM_PWM	reserved	CAN_WU	TIMER_WU	reserved	reserved	reserved	WK_WU	read/clear	1000110
	WK_STAT_2	reserved	reserved	reserved	reserved	reserved	LIN3_WU	LIN2_WU	LIN1_WU	read/clear	1000111
	WK_LVL_STAT	TEST	reserved	CFG2_STATE	reserved	reserved	reserved	reserved	WK	read	1001000
	SMPS_STAT	BST_ACT	BST_SH	BST_OP	BST_GSH	reserved	BCK_SH	BCK_OP	BCK_OOR	read/clear	1001100
	FAM_PROD_STAT	FAM_3	FAM_2	FAM_1	FAM_0	PROD_3	PROD_2	PROD_1	PROD_0	read	1111110

Figure 49 Detailed SPI bit mapping

14.5 SPI control registers

Read-/write operation (see **Chapter 14.3**):

- The 'POR / Soft Reset Value' defines the register content after POR or SBC Reset
- The 'Restart Value' defines the register content after SBC Restart, where 'x' means the bit is unchanged
- One 16-bit SPI command consist of two bytes:
  - The 7-bit address and one additional bit for the register access mode and
  - Following the data byte
    The numbering of following bit definitions refers to the data byte and correspond to the bits D0...D7 and to the SPI bits 8...15 (see also **Figure 49**)
- There are three different bit types:
  - '**r**' = READ; read-only bits (or reserved bits)
  - '**rw**' = READ/WRITE; readable and writable bits
  - '**rwh**' = READ/WRITE/HARDWARE; as **rw** with the possibility that the hardware can change the bits
- Reading a register is done byte wise by setting the SPI bit 7 to "0" (= read-only)
- Writing to a register is done byte wise by setting the SPI bit 7 to "1"
- SPI control bits are in general not cleared or changed automatically. This must be done by the microcontroller via SPI programming

M_S_CTRL
Mode- and supply control (Address 000 0001$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: 0000 0xxx$_B$

7	6	5	4	3	2	1	0
MODE_1	**MODE_0**	**Reserved**	**VCC2_ON_1**	**VCC2_ON_0**	**VCC1_OV_RST**	**VCC1_RT_1**	**VCC1_RT_0**
rw	rw	r	rw	rw	rw	rw	rw

Field	Bits	Type	Description
MODE	7:6	rw	**SBC mode control** 00_B , SBC Normal mode 01_B , SBC Sleep mode 10_B , SBC Stop mode 11_B , SBC Reset: Soft reset is executed (RO is not triggered)
Reserved	5	r	**Reserved, always reads as 0**
VCC2_ON	4:3	rw	**VCC2 mode control** 00_B , VCC2 OFF 01_B , VCC2 ON in Normal mode 10_B , VCC2 ON in Normal and Stop mode 11_B , VCC2 ON in Normal, Stop and Sleep mode
VCC1_OV_RST	2	rw	**VCC1 overvoltage reset enable** 0_B , Overvoltage on V_{CC1} will not trigger a reset 1_B , Overvoltage on V_{CC1} will trigger a reset, SBC goes to SBC Restart mode

Field	Bits	Type	Description
VCC1_RT	1:0	rw	**VCC1 reset threshold control** 00_B , Vrt1 selected (highest threshold) 01_B , Vrt2 selected 10_B , Vrt3 selected 11_B , Undervoltage Reset disabled

Note: Trying to enter SBC Sleep mode without any of the wake sources enabled will result in entering SBC Restart mode and triggering a Reset.

HW_CTRL
Hardware control (Address 000 0010_B)
POR / Soft Reset Value: $0000\ 0000_B$; Restart Value: $xx0x\ xxxx_B$

7	6	5	4	3	2	1	0
FSI_FO2	**PWM_TLAG**	**FO_ON**	**PWM_BY_WK**	**PWM_AUTO**	**BOOST_V**	**BOOST_EN**	**CFG2**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
FSI_FO2	7	rw	**Failure safe input activation** This bit is used to activate the fail-safe input by software. 0_B , FSI active 1_B , FSI disable. The pin is set as output (FO2)
PWM_TLAG	6	rw	**PWM lag time** This bit permits to set the time between the PWM to PFM transition. 0_B , 100 µs 1_B , 1 ms
FO_ON	5	rw	**Failure outputs activation** This bit is used to activate the fail outputs by software. 0_B , FOx not activated by software, FOx can be activated by defined failure 1_B , FOx activated by software
PWM_BY_WK	4	rw	**PWM of buck converter enabled by WK pin in SBC Stop mode** 0_B , Buck converter uses PFM in Stop mode 1_B , Buck converter can be switched between PFM and PWM by the level of the WK pin in SBC Stop mode
PWM_AUTO	3	rw	**Automatic transition PFM-PWM in SBC Stop mode** This bit is used to activate the automatic transition PFM to PWM in SBC Stop mode. 0_B , Buck converter always uses PFM in SBC Stop mode 1_B , Buck converter uses automatic transition PFM to PWM in case large current needed in SBC Stop mode. To come back in PFM, write a SBC Stop mode command to **M_S_CTRL**

Field	Bits	Type	Description
BOOST_V	2	rw	**Boost voltage selection** 0_B , Boost voltage 8 V typical 1_B , Boost voltage 6.65 V typical
BOOST_EN	1	rw	**Boost converter enable** 0_B , Boost off 1_B , Boost enabled, automatic switch ON for VS voltage lower than VBST,THx
CFG2	0	rw	**Configuration select 2** 0_B , Fail outputs (FOx) are active after 2nd watchdog trigger fail Config 3 1_B , Fail outputs (FOx) are active after 1st watchdog trigger fail Config 1

Note: The selection between Config 1 respectively Config 3 is done by the pin CFG. The CFG pin defines if the SBC goes to Fail-Safe mode with V_{CC1} OFF in case of a watchdog failure.

WD_CTRL
Watchdog control (Address 000 0011$_B$)
POR / Soft Reset Value: 0001 0100$_B$; Restart Value: x00x x100$_B$

7	6	5	4	3	2	1	0
CHECKSUM	**WD_STM_EN_0**	**WD_WIN**	**WD_EN_WK_BUS**	**MAX_3_RST**	**WD_TIMER_2**	**WD_TIMER_1**	**WD_TIMER_0**
w	rwh	rw	rwh	rw	rwh	rwh	rwh

Field	Bits	Type	Description
CHECKSUM	7	w	**Checksum bit** The sum of bit 7...0 needs to be even. Otherwise the bit SPI_FAIL is set and the command ignored. This bit will always read as '0'. 0_B , Counts as 0 for checksum calculation 1_B , Counts as 1 for checksum calculation
WD_STM_EN_0	6	rwh	**Watchdog activation during SBC Stop mode** 0_B , Watchdog is active in SBC Stop mode 1_B , Watchdog is deactivated in SBC Stop mode
WD_WIN	5	rw	**Watchdog window time-out feature enabled** 0_B , Watchdog works as time-out Watchdog 1_B , Watchdog works as Window Watchdog
WD_EN_WK_BUS	4	rwh	**Enable the watchdog after transceiver (CAN/LIN) wake-up in SBC Stop mode** 0_B , Watchdog will not start after a CAN/LIN1/LIN2/LIN3/ wake 1_B , Watchdog starts with a long open window after CAN/LIN1/LIN2/LIN3 wake

Field	Bits	Type	Description
MAX_3_RST	3	rw	**Limit number of resets due to a watchdog failure** 0_B , Always generate a reset in case of WD fail 1_B , After 3 consecutive resets due to WD fail, no further reset is generated
WD_TIMER	2:0	rwh	**Watchdog timer period** 000_B , 10 ms 001_B , 20 ms 010_B , 50 ms 011_B , 100 ms 100_B , 200 ms 101_B , 500 ms 110_B , 1s 111_B , reserved

*Note: See also **Chapter 13.2.4** for more information on disabling the watchdog SBC Stop mode.*

BUS_CTRL_1
Bus control (Address 000 0100_B)
POR / Soft Reset Value: $0010\ 0000_B$; **Restart Value: xxxx $x0xx_B$**

7	6	5	4	3	2	1	0
LIN_FLASH	**LIN_LSM**	**LIN_TXD_TO**	**LIN1_1**	**LIN1_0**	**reserved**	**CAN_1**	**CAN_0**
rw	rw	rw	rwh	rwh	r	rwh	rwh

Field	Bits	Type	Description
LIN_FLASH	7	rw	**LIN flash programming mode** 0_B , Slope control mechanism active 1_B , Deactivation of slope control for baud rates up to 115 kBaud
LIN_LSM	6	rw	**LIN LOW-slope mode selection** 0_B , LIN Normal-slope mode is activated 1_B , LIN Low-slope mode is activated
LIN_TXD_TO	5	rw	**LIN TXD time-out control** 0_B , TXDLIN time-out feature disabled 1_B , TXDLIN time-out feature enabled
LIN1	4:3	rwh	**LIN module mode** 00_B , LIN1 OFF 01_B , LIN1 is wake capable 10_B , LIN1 Receive-Only mode 11_B , LIN1 Normal mode
Reserved	2	r	**Reserved, always reads as 0**

Field	Bits	Type	Description
CAN	1:0	rwh	**HS-CAN module mode** 00_B , CAN OFF 01_B , CAN is wake capable 10_B , CAN Receive-Only mode 11_B , CAN Normal mode

*Note: In case CAN transceiver is configured to '11' while going to SBC Stop or Sleep mode, it will be automatically set to wake capable ('01'). However, the SPI bits will stay unchanged, i.e. once the SBC returns to Normal mode, the previous state is recovered again ('11'). The Receive-Only mode ('10') has to be selected by purpose before entering SBC Stop mode. For more details, refer to **Figure 18**.*
In case of entering SBC Sleep mode, the CAN transceiver has to be set to CAN wake capable or CAN OFF mode before.
*In case LIN transceiver is configured to '11' while going to SBC Stop or Sleep mode, it will be automatically set to wake capable ('01'). However, the SPI bits will stay unchanged, i.e. once the SBC returns to Normal mode, the previous state is recovered again ('11').The Receive-Only mode ('10') has to be selected by purpose before entering SBC Stop mode. For more details, refer to **Figure 25**.*

BUS_CTRL_2
Bus control (Address 000 0101_B)
POR / Soft Reset Value: $0000\ 0000_B$; Restart Value: $000x\ x0xx_B$

7	6	5	4	3	2	1	0
reserved	**reserved**	**reserved**	**LIN3_1**	**LIN3_0**	**reserved**	**LIN2_1**	**LIN2_0**
r	r	r	rwh	rwh	r	rwh	rwh

Field	Bits	Type	Description
Reserved	7:5	r	**Reserved, always reads as 0**
LIN3	4:3	rwh	**LIN module mode** 00_B , LIN3 OFF 01_B , LIN3 is wake capable 10_B , LIN3 Receive-Only mode 11_B , LIN3 Normal mode
Reserved	2	r	**Reserved, always reads as 0**
LIN2	1:0	rwh	**LIN module mode** 00_B , LIN2 OFF 01_B , LIN2 is wake capable 10_B , LIN2 Receive-Only mode 11_B , LIN2 Normal mode

*Note: In case either CAN or LIN transceivers are configured to '11' while going to SBC Stop or Sleep mode, they will be automatically set to wake capable ('01'). However, the SPI bits will stay unchanged, i.e. once the SBC returns to Normal mode, the previous state is recovered again ('11').The Receive-Only mode ('10') has to be selected by purpose before entering SBC Stop mode. For more details, refer to **Figure 25**.*

WK_CTRL_1
Wake input control (Address 000 0110$_B$)
POR / Soft Reset Value: 0000 0000$_B$; **Restart Value: 0x00 0000$_B$**

7	6	5	4	3	2	1	0
reserved	**TIMER1_WK_EN**	**reserved**	**reserved**	**reserved**	**WD_STM_EN_1**	**reserved**	**reserved**
r	rw	r	r	r	rwh	r	r

Field	Bits	Type	Description
Reserved	7	r	**Reserved, always reads as 0**
TIMER1_WK_EN	6	rw	**Timer1 wake source control** 0_B , Timer1 wake disabled 1_B , Timer1 is enabled as a wake source
Reserved	5:3	r	**Reserved, always reads as 0**
WD_STM_EN_1	2	rwh	**Watchdog activation during SBC Stop mode** 0_B , Watchdog is active in Stop mode 1_B , Watchdog is deactivated in Stop mode
Reserved	1:0	r	**Reserved, always reads as 0**

WK_CTRL_2
Wake source control (Address 000 0111$_B$)
POR / Soft Reset Value: 0000 0001$_B$; **Restart Value: 0000 000x$_B$**

7	6	5	4	3	2	1	0
reserved	**reserved**	**reserved**	**reserved**	**reserved**	**reserved**	**reserved**	**WK_EN**
r	r	r	r	r	r	r	rw

Field	Bits	Type	Description
Reserved	7:1	r	**Reserved, always reads as 0**
WK_EN	0	rw	**WK wake source control** 0_B , WK wake disabled 1_B , WK is enabled as a wake source

WK_PUPD_CTRL
Wake input level control (Address 000 1000$_B$)
POR / Soft Reset Value: 0000 0000$_B$; **Restart Value: 0000 00xx$_B$**

7	6	5	4	3	2	1	0
reserved	**reserved**	**reserved**	**reserved**	**reserved**	**reserved**	**WK_PUPD_1**	**WK_PUPD_0**
r	r	r	r	r	r	rw	rw

Field	Bits	Type	Description
Reserved	7:2	r	**Reserved, always reads as 0**
WK_PUPD	1:0	rw	**WK pull-up/pull-down configuration** 00_B , No pull-up/pull-down selected 01_B , Pull-down resistor selected 10_B , Pull-up resistor selected 11_B , Automatic switching to pull-up or pull-down

TIMER1_CTRL
Timer1 control and selection (Address 000 1100_B)
POR / Soft Reset Value: 0000 0000_B; **Restart Value: 0000 $0xxx_B$**

7	6	5	4	3	2	1	0
reserved	**reserved**	**reserved**	**reserved**	**reserved**	**TIMER1_PER_2**	**TIMER1_PER_1**	**TIMER1_PER_0**
r	r	r	r	r	rw	rw	rw

Field	Bits	Type	Description
Reserved	7:3	r	**Reserved, always reads as 0**
TIMER1_PER	2:0	rw	**Timer1 period configuration** 000_B , 10 ms 001_B , 20 ms 010_B , 50 ms 011_B , 100 ms 100_B , 200 ms 101_B , 1 s 110_B , 2 s 111_B , reserved

SYS_STATUS_CTRL
System status control (Address 001 1110_B)
POR Value: 0000 0000_B; **Restart Value/Soft Reset Value: xxxx $xxxx_B$**

7	6	5	4	3	2	1	0
SYS_STAT_7	**SYS_STAT_6**	**SYS_STAT_5**	**SYS_STAT_4**	**SYS_STAT_3**	**SYS_STAT_2**	**SYS_STAT_1**	**SYS_STAT_0**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
SYS_STAT	7:0	rw	**System status control byte (bit0=LSB; bit7=MSB)** Dedicated byte for system configuration, access only by microcontroller. No SBC functions

Notes

1. *The **SYS_STATUS_CTRL** register is an exception for the default values, i.e. it will keep its configured value even after a Soft Reset.*
2. *This byte is intended for storing system configurations of the ECU by the microcontroller and it is writable in SBC Normal and Stop mode. The byte is not accessible by the SBC and is also not cleared after Fail-Safe or SBC Restart mode. It allows the microcontroller to quickly store system configuration without losing the data.*

14.6 SPI status information registers

Read-/write operation (see **Chapter 14.3**):

- One 16-bit SPI command consists of two bytes:
  - The 7-bit address and one additional bit for the register access mode and
  - Following the data byte will be ignored when accessing a status register
    The numbering of following bit definitions refers to the data byte and correspond to the bits D0...D7 and to the SPI bits 8...15 (see also)
- There are two different bit types:
  - **'r'** = READ: read-only bits (or reserved bits)
  - **'rc'** = READ/CLEAR: readable and clearable bits
- Reading a register is done byte wise by setting the SPI bit 7 to "0" (= read-only)
- Clearing a register is done byte wise by setting the SPI bit 7 to "1"
- SPI status registers are in general not cleared or changed automatically (an exception are the **WD_FAIL** bits). This must be done by the microcontroller via SPI command

SUP_STAT
Supply voltage fail status (Address 100 0001_B)
POR / Soft Reset Value: x000 0000_B; **Restart Value: xxxx xx0x$_B$**

7	6	5	4	3	2	1	0
POR	**VLIN_UV**	**VCC1_OV**	**VCC2_OT**	**VCC2_UV**	**VCC1_SC**	**reserved**	**VCC1_UV**
rc	rc	rc	rc	rc	rc	r	rc

Field	Bits	Type	Description
POR	7	rc	**Power-on-reset detection** 0_B , No POR 1_B , POR occurred
VLIN_UV	6	rc	**VLIN undervoltage detection** 0_B , No VLIN undervoltage 1_B , VLIN undervoltage detected
VCC1_OV	5	rc	**VCC1 overvoltage detection** 0_B , No VCC1 overvoltage 1_B , VCC1 overvoltage detected
VCC2_OT	4	rc	**VCC2 overtemperature detection** 0_B , No overtemperature 1_B , VCC2 overtemperature detected
VCC2_UV	3	rc	**VCC2 undervoltage detection** 0_B , No VCC2 undervoltage 1_B , VCC2 undervoltage detected

Field	Bits	Type	Description
VCC1_SC	2	rc	**VCC1 short to GND detection** 0_B , No short 1_B , VCC1 short to GND detected
Reserved	1	r	**Reserved, always reads 0**
VCC1_UV	0	rc	**VCC1 undervoltage detection** 0_B , No VCC1 undervoltage 1_B , VCC1 undervoltage detected

Notes

1. *When VCC1 is OFF (for example in SBC Sleep mode), the bits VCC1_SC and VCC1_UV will not be set.*
2. *When VCC2 is OFF, the bit VCC2_UV and VCC2_OT will not be set.*
3. *When all LIN's are wake capable or OFF, VLIN_UV will not be set.*

THERM_STAT
Thermal protection status (Address 100 0010$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: 0000 0xxx$_B$

7	6	5	4	3	2	1	0
reserved	**reserved**	**reserved**	**reserved**	**reserved**	**TSD2**	**TSD1**	**TPW**
r	r	r	r	r	rc	rc	rc

Field	Bits	Type	Description
Reserved	7:3	r	**Reserved, always reads as 0**
TSD2	2	rc	**TSD2 thermal shutdown detection** 0_B , No TSD2 fail 1_B , TSD2 thermal shutdown detected (leading to SBC Fail-Safe mode)
TSD1	1	rc	**TSD1 thermal shutdown detection** 0_B , No TSD1 fail 1_B , TSD1 thermal shutdown detected
TPW	0	rc	**Thermal prewarning** 0_B , No thermal prewarning 1_B , Thermal prewarning detected

DEV_STAT
Device information status (Address 100 0011$_B$)
POR / Soft Reset Value: 0000 0000$_B$; Restart Value: xxxx xxxx$_B$

7	6	5	4	3	2	1	0
DEV_STAT_1	**DEV_STAT_0**	**RO_CL_HIGH**	**FSI_FAIL**	**WD_FAIL_1**	**WD_FAIL_0**	**SPI_FAIL**	**FO_ON_STATE**
rc	rc	rc	rc	rh	rh	rc	rc

Field	Bits	Type	Description
DEV_STAT	7:6	rc	**Device status before Restart mode** 00_B , Cleared (register must be actively cleared) 01_B , Restart after failures (WD fail, TSD2, VCC1_UV and VCC1_OV); also wake from SBC Fail-Safe mode 10_B , Wake from Sleep mode 11_B , Not used
RO_CL_HIGH	5	rc	**Reset PIN clamped to HIGH level detected** 0_B , No Reset Clamped to HIGH detected 1_B , Reset Clamped to HIGH detected
FSI_FAIL	4	rc	**FSI fail information** 0_B , No FSI fail 1_B , Failure on FSI pattern recognized
WD_FAIL	3:2	rh	**Number of WD-fail event** 00_B , No WD-fail 01_B , 1x WD-fail, causing SBC activates FOx in Config1 10_B , 2x WD-fails, causing SBC activates FOx in Config3 11_B , Reserved (never achieved)
SPI_FAIL	1	rc	**SPI fail information** 0_B , No SPI fail 1_B , Invalid SPI command detected, SPI command is not executed
FO_ON_STATE	0	rc	**Fail outputs on status** 0_B , FO outputs are not activated 1_B , FO outputs are activated

Notes

1. *The bits **DEV_STAT** show the status of the device before it went through Restart. Either the device came from regular Sleep mode (‘10’) or a failure (‘01’ - SBC Restart or SBC Fail-Safe mode: WD fail, TSD2 fail, VCC1_UV fail or VCC1_OV if bit **VCC1_OV_ RST** is set) occurred.*
2. *The **WD_FAIL** bits are configured as a counter and are the only status bits which are cleared automatically by the SBC. They are cleared after a successful watchdog trigger. See also **Chapter 12.1**.*
3. *The SPI_FAIL bit is cleared only by SPI command.*

BUS_STAT_1
Bus communication status (Address 100 0100_B)
POR / Soft Reset Value: 0000 0000_B; Restart Value: 0xx0 $0xxx_B$

7	6	5	4	3	2	1	0
reserved	**LIN1_FAIL_1**	**LIN1_FAIL_0**	**reserved**	**reserved**	**CAN_FAIL_1**	**CAN_FAIL_0**	**VCAN_UV**
r	rc	rc	r	r	rc	rc	rc

Field	Bits	Type	Description
Reserved	7	r	**Reserved, always reads as 0**
LIN1_FAIL	6:5	rc	**LIN failure status** 00_B , No error 01_B , LIN TSD shutdown, also TSD1 is signaled 10_B , LIN_TXD_DOM: TXDLIN dominant time out 11_B , LIN_BUS_DOM: BUS dominant time out
Reserved	4:3	r	**Reserved, always reads as 0**
CAN_FAIL	2:1	rc	**CAN failure status** 00_B , No error 01_B , CAN TSD shutdown, also TSD1 signaled 10_B , CAN_TXD_DOM: TXDCAN dominant time out 11_B , CAN_BUS_DOM: BUS dominant time out
VCAN_UV	0	rc	**Undervoltage VCAN supply** 0_B , Normal operation 1_B , VCAN supply undervoltage detected. Transmitter disabled

Notes

1. *CAN and LIN recovery conditions:*
   1.) TXD Time Out: TXD goes HIGH or transmitter is set to wake capable or switched off.
   2.) Bus dominant time out: Bus will become recessive or transceiver is set to wake capable or switched off.
   3.) Supply undervoltage: as soon as the threshold is crossed again, i.e. VLIN > VS_UV for LIN and VCAN > VCAN_UV for CAN.
   4.) In all cases (also for TSD shutdown): to enable the bus transmission again, TXD needs to be HIGH for a certain time (transmitter enable time).
2. *The VCAN_UV comparator is enabled if the CAN is CAN Normal mode or CAN Receive-Only mode or CAN Wake Capable after one valid WUP is detected.*

BUS_STAT_2
Bus communication status (Address 100 0101_B)
POR / Soft Reset Value: 0000 0000_B; Restart Value: 000x $xxx0_B$

7	6	5	4	3	2	1	0
reserved	**reserved**	**reserved**	**LIN3_FAIL_1**	**LIN3_FAIL_0**	**LIN2_FAIL_1**	**LIN2_FAIL_0**	**reserved**
r	r	r	rc	rc	rc	rc	r

Field	Bits	Type	Description
Reserved	7:5	r	**Reserved, always reads as 0**

Field	Bits	Type	Description
LIN3_FAIL	4:3	rc	**LIN failure status** 00_B , No error 01_B , LIN TSD shutdown, also TSD1 signaled 10_B , LIN_TXD_DOM: TXDLIN dominant time out 11_B , LIN_BUS_DOM: BUS dominant time out
LIN2_FAIL	2:1	rc	**LIN failure status** 00_B , No error 01_B , LIN TSD shutdown, also TSD1 signaled 10_B , LIN_TXD_DOM: TXDLIN dominant time out 11_B , LIN_BUS_DOM: BUS dominant time out
Reserved	0	r	**Reserved, always reads as 0**

Notes

1. *LIN recovery conditions:*
   1.) TXD Time Out: TXD goes HIGH or transmitter is set to wake capable or switched off.
   2.) Bus dominant time out: Bus will become recessive or transceiver is set to wake capable or switched off.
   3.) Supply undervoltage: as soon as the threshold is crossed again, i.e. VLIN > VS_UV
   4.) In all cases (also for TSD shutdown): to enable the bus transmission again, TXD needs to be HIGH for a certain time (transmitter enable time).

WK_STAT_1
Wake-up source and information status (Address 100 0110_B)
POR / Soft Reset Value: 0000 0000_B; **Restart Value: x0xx $000x_B$**

7	6	5	4	3	2	1	0
PFM_PWM	**reserved**	**CAN_WU**	**TIMER_WU**	**reserved**	**reserved**	**reserved**	**WK_WU**
rc	r	rc	rc	r	r	r	rc

Field	Bits	Type	Description
PFM_PWM	7	rc	**PFM_PWM automatic transition detected** 0_B , No automatic PFM_PWM transition detected 1_B , Automatic PFM_PWM transition detected
Reserved	6	r	**Reserved, always reads as 0**
CAN_WU	5	rc	**Wake up via CAN bus** 0_B , No Wake up 1_B , Wake up
TIMER_WU	4	rc	**Wake up via timer** 0_B , No Wake up 1_B , Wake up
Reserved	3:1	r	**Reserved, always reads as 0**

Field	Bits	Type	Description
WK_WU	0	rc	**Wake up via WK** 0_B , No Wake up 1_B , Wake up

WK_STAT_2
Wake-up source and information status (Address 100 0111$_B$)
POR / Soft Reset Value: 0000 0000$_B$; **Restart Value: 0000 xxxx$_B$**

7	6	5	4	3	2	1	0
reserved	**reserved**	**reserved**	**reserved**	**reserved**	**LIN3_WU**	**LIN2_WU**	**LIN1_WU**
r	r	r	r	r	rc	rc	rc

Field	Bits	Type	Description
Reserved	7:3	r	**Reserved, always reads as 0**
LIN3_WU	2	rc	**Wake up via LIN3 bus** 0_B , No Wake up 1_B , Wake up
LIN2_WU	1	rc	**Wake up via LIN2 bus** 0_B , No Wake up 1_B , Wake up
LIN1_WU	0	rc	**Wake up via LIN1 bus** 0_B , No Wake up 1_B , Wake up

WK_LVL_STAT
WK input level (Address 100 1000$_B$)
POR / Soft Reset Value: x100 000x$_B$; **Restart Value: x1x0 000x$_B$**

7	6	5	4	3	2	1	0
TEST	**reserved**	**CFG2_STATE**	**reserved**	**reserved**	**reserved**	**reserved**	**WK**
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
TEST	7	r	**Status of TEST pin** 0_B , LOW Level (= 0) 1_B , HIGH Level (= 1), SBC Development mode is enabled, No reset triggered due to wrong watchdog trigger
reserved	6	r	**Reserved, always reads as 1**

Field	Bits	Type	Description
CFG2_ STATE	5	r	**Status of CFG2 bit on HW_CTRL register** This bit shows the setting in bit **CFG2**. 0_B , LOW Level; Fail outputs (FOx) are active after 2nd watchdog trigger fail Config 3 1_B , HIGH Level; Fail outputs (FOx) are active after 1st watchdog trigger fail Config 1
Reserved	4:1	r	**Reserved, always reads as 0**
WK	0	r	**Status of WK** 0_B , LOW Level (= 0) 1_B , HIGH Level (= 1)

SMPS_STAT
SMPS state (Address 100 1100_B)
POR / Soft Reset Value: 0000 $0xxx_B$; Restart Value: xxxx $0xxx_B$

7	6	5	4	3	2	1	0
BST_ACT	**BST_SH**	**BST_OP**	**BST_GSH**	**reserved**	**BCK_SH**	**BCK_OP**	**BCK_OOR**
rc	rc	rc	rc	r	rc	rc	rc

Field	Bits	Type	Description
BST_ACT	7	rc	**Boost regulator active** 0_B , Boost not active 1_B , Boost active
BST_SH	6	rc	**BSTD and SNSP short detection** 0_B , No short detected on BSTD and SNSP pins 1_B , BSTD or SNSP pins short to GND
BST_OP	5	rc	**BSTD, SNSP SNSN open detection** 0_B , No open detection in BSTD, SNSP and SNSN pins 1_B , Or operation between: BSTD loss of diode detected, SNSP loss of resistor detected, SNSN loss of GND detected
BST_GSH	4	rc	**BSTG pin short detection** 0_B , BSTG no short detected 1_B , BSTG short detected to GND or internal supply
Reserved	3	r	**Reserved, always reads as 0**
BCK_SH	2	rc	**BCKSW pin short detection** 0_B , No short detected 1_B , Short to GND or short to VS detected on BCKSW pin
BCK_OP	1	rc	**BCKSW pin open detection** 0_B , No BCKSW open detected 1_B , BCKSW open detected

Field	Bits	Type	Description
BCK_OOR	0	rc	**VCC1 out-of-range** 0_B , VCC1 inside $V_{CC1,out1}$ ±12% 1_B , VCC1 outside $V_{CC1,out1}$ ±12%

FAM_PROD_STAT
SWK Data0 register (Address 111 1110_B)
POR / Soft Reset Value: 0010 $xxxx_B$; Restart Value: 0010 $xxxx_B$

7	6	5	4	3	2	1	0
FAM_3	**FAM_2**	**FAM_1**	**FAM_0**	**PROD_3**	**PROD_2**	**PROD_1**	**PROD_0**
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
FAM	7:4	r	**Family of products** 0010_B , TLE927x Family, High End SBC
PROD	3:0	r	**Product variant** 0100_B , LIN1/2 available, V_{CC1} = 5 V 0101_B , LIN1/2 available, V_{CC1} = 3.3 V 1000_B , LIN1-3 available, V_{CC1} = 5 V 1001_B , LIN1-3 available, V_{CC1} = 3.3 V 1100_B , LIN1-4 available, V_{CC1} = 5 V 1101_B , LIN1-4 available, V_{CC1} = 3.3 V

14.7 Electrical characteristics

Table 23 Electrical characteristics: power stage

T_j = -40°C to +150°C, V_S = 5.5 V to 28 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
SPI frequency							
Maximum SPI frequency	$f_{SPI,max}$	–	–	4.0	MHz	1)	P_14.8.1
SPI interface; logic inputs SDI, CLK and CSN							
H-input voltage threshold	V_{IH}	–	–	0.7 × V_{CC1}	V	–	P_14.8.2
L-input voltage threshold	V_{IL}	0.3 × V_{CC1}	–	–	V	–	P_14.8.3
Hysteresis of input voltage	V_{IHY}	–	0.2 × V_{CC1}	–	V	1)	P_14.8.4
Pull-up resistance at pin CSN	R_{ICSN}	20	40	80	kΩ	V_{CSN} = 0.7 × V_{CC1}	P_14.8.5
Pull-down resistance at pin SDI and CLK	$R_{ICLK/SDI}$	20	40	80	kΩ	$V_{SDI/CLK}$ = 0.2 × V_{CC1}	P_14.8.6
Input capacitance at pin CSN, SDI or CLK	C_I	–	10	–	pF	1)	P_14.8.7
Logic output SDO							
H-output voltage level	V_{SDOH}	V_{CC1} - 0.4	V_{CC1} - 0.2	–	V	I_{DOH} = -1.6 mA	P_14.8.8
L-output voltage level	V_{SDOL}	–	0.2	0.4	V	I_{DOL} = 1.6 mA	P_14.8.9
Tri-state leakage current	I_{SDOLK}	-10	–	10	µA	V_{CSN} = V_{CC1}; 0 V < V_{DO} < V_{CC1}	P_14.8.10
Tri-state input capacitance	C_{SDO}	–	10	15	pF	1)	P_14.8.11
Data input timing[1)]							
Clock period	t_{pCLK}	250	–	–	ns	–	P_14.8.12
Clock HIGH time	t_{CLKH}	125	–	–	ns	–	P_14.8.13
Clock LOW time	t_{CLKL}	125	–	–	ns	–	P_14.8.14
Clock LOW before CSN LOW	t_{bef}	125	–	–	ns	–	P_14.8.15
CSN setup time	t_{lead}	250	–	–	ns	–	P_14.8.16
CLK setup time	t_{lag}	250	–	–	ns	–	P_14.8.17
Clock LOW after CSN HIGH	t_{beh}	125	–	–	ns	–	P_14.8.18
SDI setup time	t_{DISU}	100	–	–	ns	–	P_14.8.19
SDI hold time	t_{DIHO}	50	–	–	ns	–	P_14.8.20

Table 23 Electrical characteristics: power stage (cont'd)

T_j = -40°C to +150°C, V_S = 5.5 V to 28 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input signal rise time at pin SDI, CLK and CSN	t_{rIN}	–	–	50	ns	–	P_14.8.21
Input signal fall time at pin SDI, CLK and CSN	t_{fIN}	–	–	50	ns	–	P_14.8.22
Delay time for mode changes[2)]	$t_{Del,Mode}$	–	–	10	µs	–	P_14.8.23
CSN HIGH time	$t_{CSN(high)}$	3	–	–	µs	–	P_14.8.24
Data output timing[1)]							
SDO rise time	t_{rSDO}	–	30	80	ns	C_L = 100 pF	P_14.8.25
SDO fall time	t_{fSDO}	–	30	80	ns	C_L = 100 pF	P_14.8.26
SDO enable time	t_{ENSDO}	–	–	50	ns	LOW impedance	P_14.8.27
SDO disable time	t_{DISSDO}	–	–	50	ns	HIGH impedance	P_14.8.28
SDO valid time	t_{VASDO}	–	–	50	ns	C_L = 100 pF	P_14.8.29

1) Not subject to production test; specified by design.

2) Applies to all mode changes triggered via SPI commands.

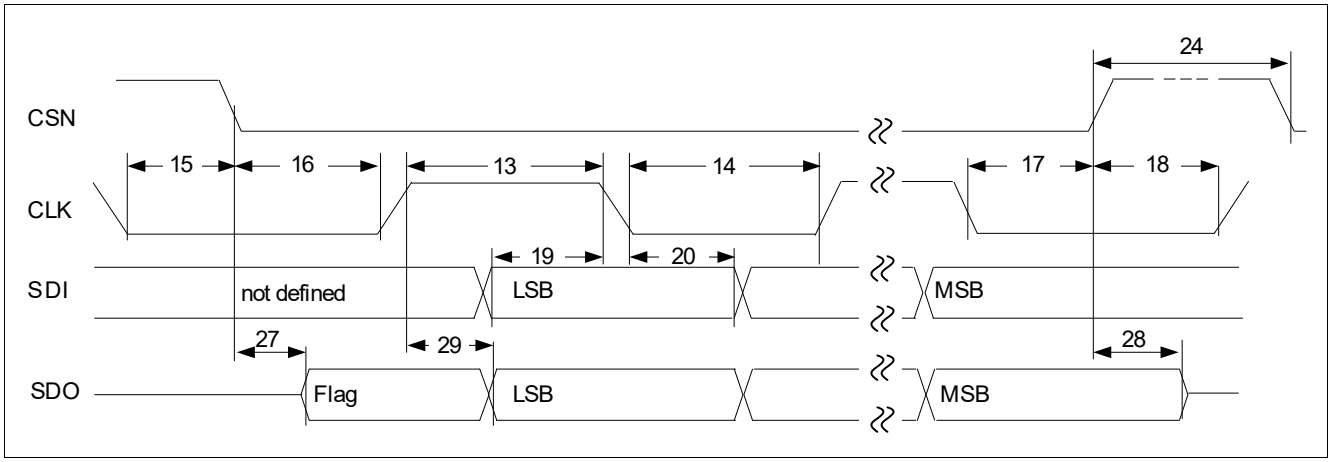

Figure 50 SPI timing diagram

Note: Numbers in drawing correlate to the last 2 digits of the number field in the electrical characteristics table.

15 Application information

15.1 Application diagram with boost module

Note: The following information is given as a hint for the implementation of the device only and should not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

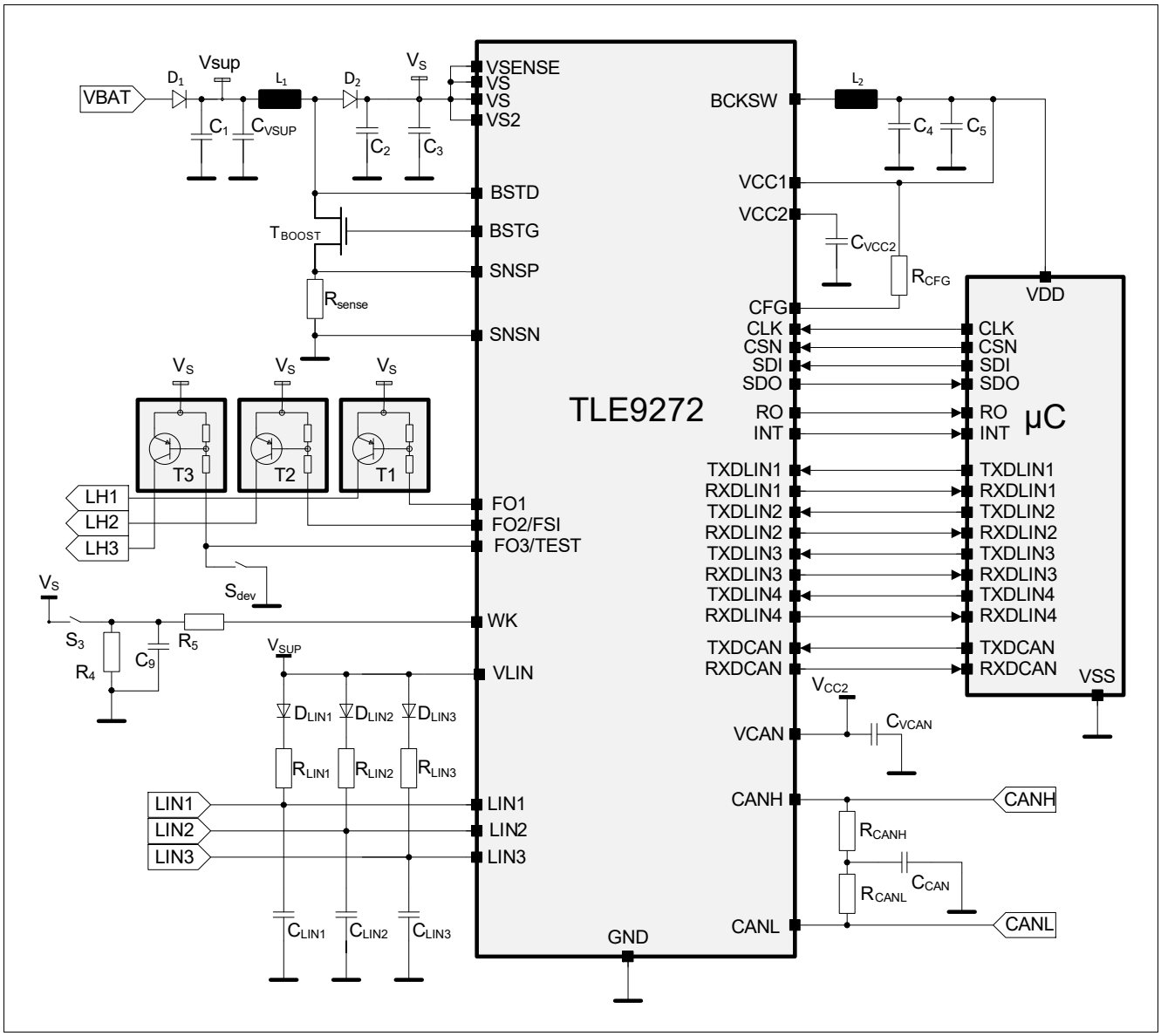

Figure 51 Application diagram

Note: This is a very simplified example of an application circuit. The function must be verified in the real application.

Table 24 Bill of material for Figure 15.1

Ref.	Typical value	Purpose/comment
Capacitances		
C_1	47 µF ±20% electrolytic	Buffering capacitor to cut off battery spikes, depending on the application
C_{VSUP}	100 nF ±20% ceramic	Input filter battery capacitor for optimum EMC behavior
C_2	100 µF…560 µF ±20%, 50 V electrolytic	Output boost capacitor. ESR ≤ 1 Ω over the temperature range
C_3	1 µF…10 µF ±20%, 50 V ceramic	Input buck capacitor. Low ESR
C_4	10 µF ±20%, 16 V ceramic	[1] Output buck capacitor, for cost optimization. Low ESR
C_5	47 µF ±20%, 16 V electrolytic	[1] Output buck capacitor, for cost optimization. ESR ≤ 4 Ω over the temperature range
C_{VCC2}	2.2 µF ±20%, 16 V ceramic	Blocking capacitor, min. 470 nF for stability. Low ESR
C_9	10 nF ±20% ceramic	Spikes filtering, as required by application. Mandatory protection for off-board connection
C_{VCAN}	100 nF ±20%, 16 V ceramic	Input filter CAN supply. The capacitor must be placed close to the VCAN pin. One additional buffer capacitor ≥1 µF shall be placed for optimum EMC and CAN FD performances
C_{CAN}	47 nF / OEM dependent	Split termination stability
C_{LIN1}	1 nF / OEM dependent	LIN master termination
C_{LIN2}	1 nF / OEM dependent	LIN master termination
C_{LIN3}	1 nF / OEM dependent	LIN master termination
C_{LIN4}	1 nF / OEM dependent	LIN master termination
Resistances		
R_{SENSE}	100 mΩ ±1%	Boost regulator current sense. Depending on required current limitation
R_{CFG}	10 kΩ…22 kΩ ±5%	Required for hardware initialization
R_4	10 kΩ ±20%	Wetting current of the switch, as required by application
R_5	10 kΩ ±20%	Limit the WK pin current, e.g. for ISO pulses
R_{CANH}	60 Ω / OEM dependent	CAN bus termination
R_{CANL}	60 Ω / OEM dependent	CAN bus termination
R_{LIN1}	1 kΩ / OEM dependent	LIN master termination (if configured as a LIN master)
R_{LIN2}	1 kΩ / OEM dependent	LIN master termination (if configured as a LIN master)
R_{LIN3}	1 kΩ / OEM dependent	LIN master termination (if configured as a LIN master)
Inductors		
L_1	22 µH ±20%[2]	Boost regulator coil
L_2	47 µH ±20%[2]	Buck regulator coil

Table 24 Bill of material for Figure 15.1 (cont'd)

Ref.	Typical value	Purpose/comment
Active components		
D_1	e.g. SS34HE3/9AT (Vishay)	Reverse polarity protection. Depending for the application
D_2	e.g. SL04-GS08 or SS34HE3/9AT (Vishay)	Boost regulator power diode. Forward current depends on the application
D_{LIN1}	e.g. BAS70	Requested by LIN standard; reverse polarity protection of network
D_{LIN2}	e.g. BAS70	Requested by LIN standard; reverse polarity protection of network
D_{LIN3}	e.g. BAS70	Requested by LIN standard; reverse polarity protection of network
D_{LIN4}	e.g. BAS70	Requested by LIN standard; reverse polarity protection of network
T_{BOOST}	e.g. BSS606N	Boost regulator external MOSFET. Maximum Rds_on ≤ 100 mΩ, Drain current max ≤ 3 A, Drain-Source max voltage ≤ 60 V
T_1	e.g. BCR191W	High active FO1 control
T_2	e.g. BCR191W	High active FO2 control
T_3	e.g. BCR191W	High active FO3 control
µC	e.g. XC2xxx	Microcontroller

1) For for optimum dynamic behavior, C4 and C5 = 22 µF ±20%, 16 V ceramic low ESR.

2) The saturation current has to be define in according with the maximum current required by the application.

15.2 Application diagram without boost module

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

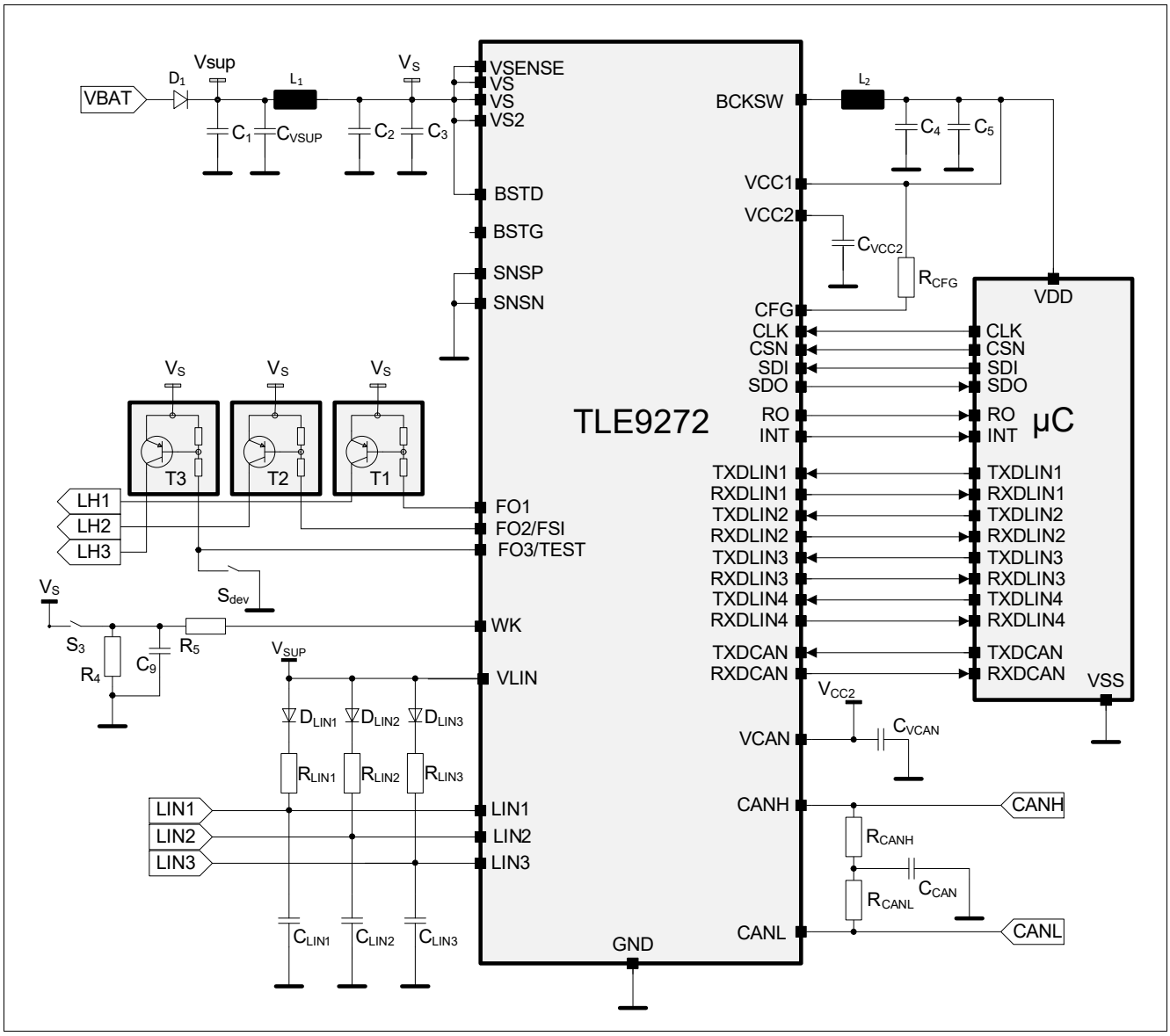

Figure 52 Application diagram

Note: This is a very simplified example of an application circuit. The function must be verified in the real application.

Table 25 Bill of material for Figure 15.2

Ref.	Typical value	Purpose/comment
EMI filter components[1)]		
C_1	47 µF ±20%, 50 V electrolytic	Input EMI filter capacitor, depending on the application
L_1	2.2 µH ±20%[2)]	Input EMI filter inductor, depending on the application
C_2	4.7 µF ±20%, 50 V ceramic low ESR	Input EMI filter capacitor, depending on the application
Capacitances		
C_{VSUP}	100 nF ±20% ceramic	Input filter battery capacitor for optimum EMC behavior
C_3	1 µF…10 µF ±20% ceramic	Input buck capacitor. Low ESR
C_4	10 µF ±20%, 16 V ceramic	[3)] Output buck capacitor, for cost optimization. Low ESR
C_5	47 µF ±20%, 16 V electrolytic	[3)] Output buck capacitor, for cost optimization. ESR ≤ 4 Ω over the temperature range
C_{VCC2}	2.2 µF ±20% ceramic	Blocking capacitor, min. 470 nF for stability. Low ESR
C_9	10 nF ceramic	Spikes filtering, as required by application. Mandatory protection for off-board connection
C_{VCAN}	100 nF ± 20%, 16 V ceramic	Input filter CAN supply. The capacitor must be placed close to the VCAN pin. One additional buffer capacitor ≥ 1 µF shall be placed for optimum EMC and CAN FD performances
C_{CAN}	47 nF / OEM dependent	Split termination stability
C_{LIN1}	1 nF / OEM dependent	LIN master termination
C_{LIN2}	1 nF / OEM dependent	LIN master termination
C_{LIN3}	1 nF / OEM dependent	LIN master termination
C_{LIN4}	1 nF / OEM dependent	LIN master termination
Resistances		
R_{CFG}	10 kΩ…22 kΩ ±5%	Required for hardware initialization
R_4	10 kΩ ±5%	Wetting current of the switch, as required by application
R_5	10 kΩ ±5%	Limit the WK pin current, e.g. for ISO pulses
R_{CANH}	60 Ω / OEM dependent	CAN bus termination
R_{CANL}	60 Ω / OEM dependent	CAN bus termination
R_{LIN1}	1 kΩ / OEM dependent	LIN master termination (if configured as a LIN master)
R_{LIN2}	1 kΩ / OEM dependent	LIN master termination (if configured as a LIN master)
R_{LIN3}	1 kΩ / OEM dependent	LIN master termination (if configured as a LIN master)
R_{LIN4}	1 kΩ / OEM dependent	LIN master termination (if configured as a LIN master)
Inductors		
L_2	47 µH ±20%[2)]	Buck regulator coil

Table 25 Bill of material for Figure 15.2 (cont'd)

Ref.	Typical value	Purpose/comment
Active Components		
D_1	e.g. SS34HE3/9AT (Vishay)	Reverse polarity protection. Depending for the application
D_{LIN1}	e.g. BAS70	Requested by LIN standard; reverse polarity protection of network
D_{LIN2}	e.g. BAS70	Requested by LIN standard; reverse polarity protection of network
D_{LIN3}	e.g. BAS70	Requested by LIN standard; reverse polarity protection of network
D_{LIN4}	e.g. BAS70	Requested by LIN standard; reverse polarity protection of network
T_1	e.g. BCR191W	High active FO1 control
T_2	e.g. BCR191W	High active FO2 control
T_3	e.g. BCR191W	High active FO3 control
µC	e.g. XC2xxx	Microcontroller

1) The input EMI filter has to be evaluated in according with the final application. The values are only given as hint.
2) The saturation current has to be define in according with the maximum current required by the application.
3) For optimum dynamic behavior, C4 and C5 = 22 µF ±20%, 16 V ceramic low ESR.

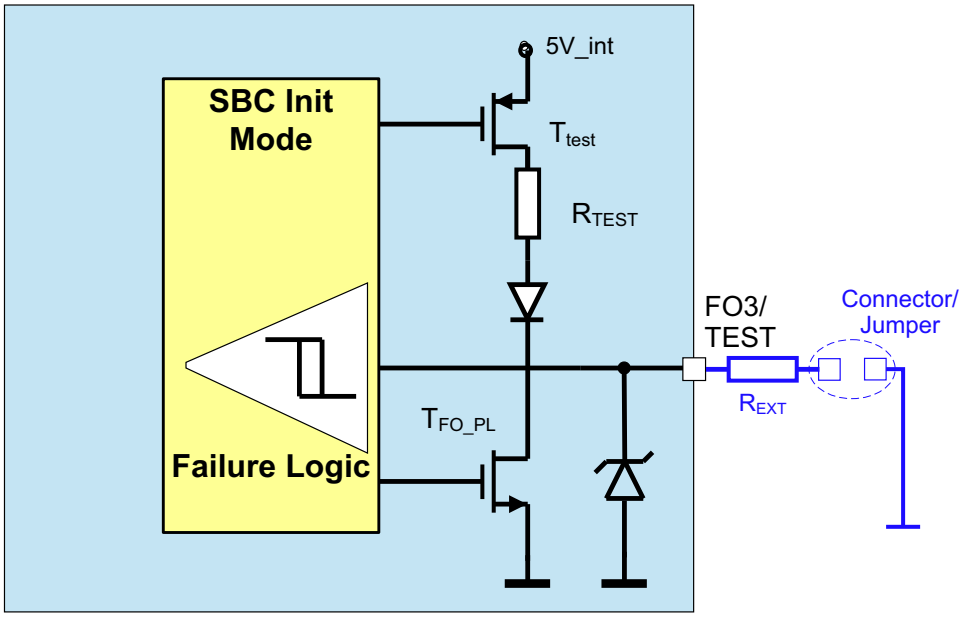

Figure 53 Hint for increasing the robustness of pin FO3/TEST during debugging or programming

15.3 ESD tests

*Note: Tests for ESD robustness according to IEC61000-4-2 “gun test” (150pF, 330Ω) have been performed. The results and test condition are available in a test report. The minimum values for the test are listed in **Table 26** below.*

Table 26 ESD “Gun Test”

Performed test	Result	Unit	Remarks
ESD at pin CANH, CANL, LIN, versus GND	>6	kV	1)2) positive pulse
ESD at pin CANH, CANL, LIN, versus GND	< -6	kV	1)2) negative pulse

1) ESD susceptibility “ESD GUN” according to LIN EMC 1.3 Test Specification, Section 4.3 (IEC 61000-4-2). Tested by external test house (IBEE, EMC Test report Nr. 01-03-17).

2) ESD Test “Gun Test” is specified with external components for pins VS, WK, BKSW, VCC2. Refer to application diagram in **Chapter 15.2** for more information.

EMC and ESD susceptibility tests according to SAE J2962-2 (2010) have been performed. Tested by external test house (UL LLC, Test report Nr. 2017-327).

15.4 Thermal behavior of package

The figure below shows the thermal resistance (R_{th_JA}) of the device versus the cooling area on the bottom of the PCB for T_A = 85°C. Every line reflects a different PCB and thermal via design.

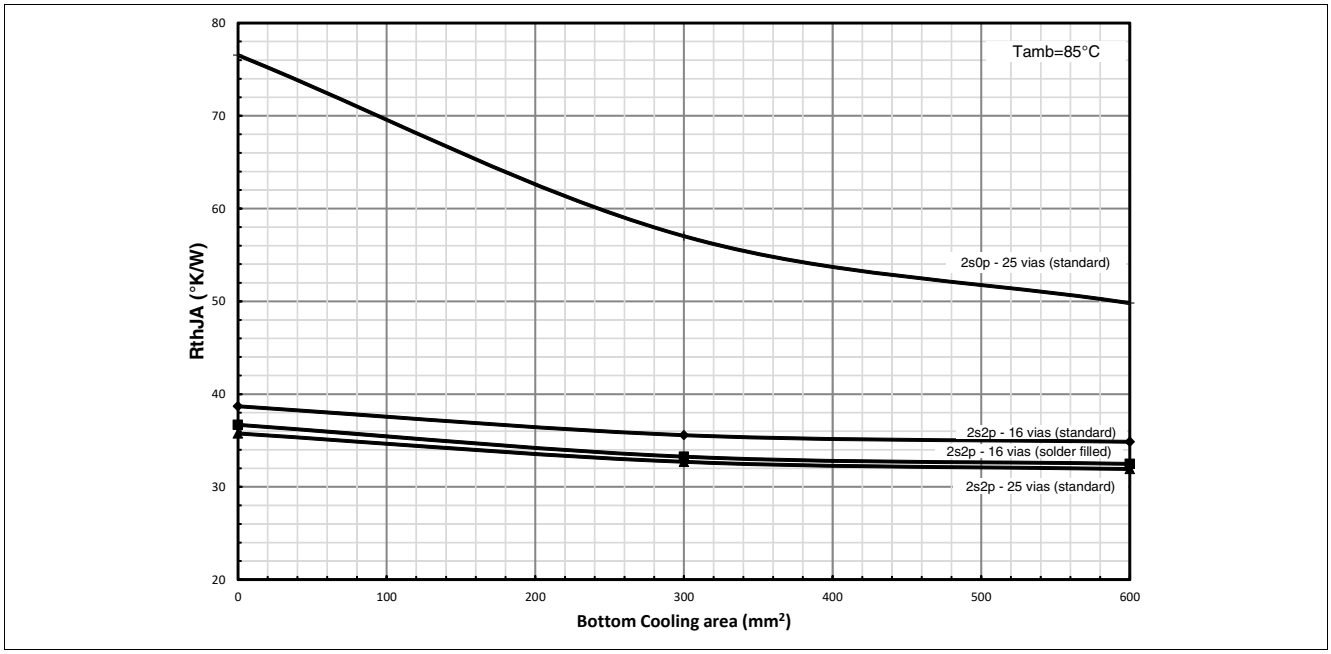

Figure 54 Thermal resistance (R_{th_JA}) versus cooling area

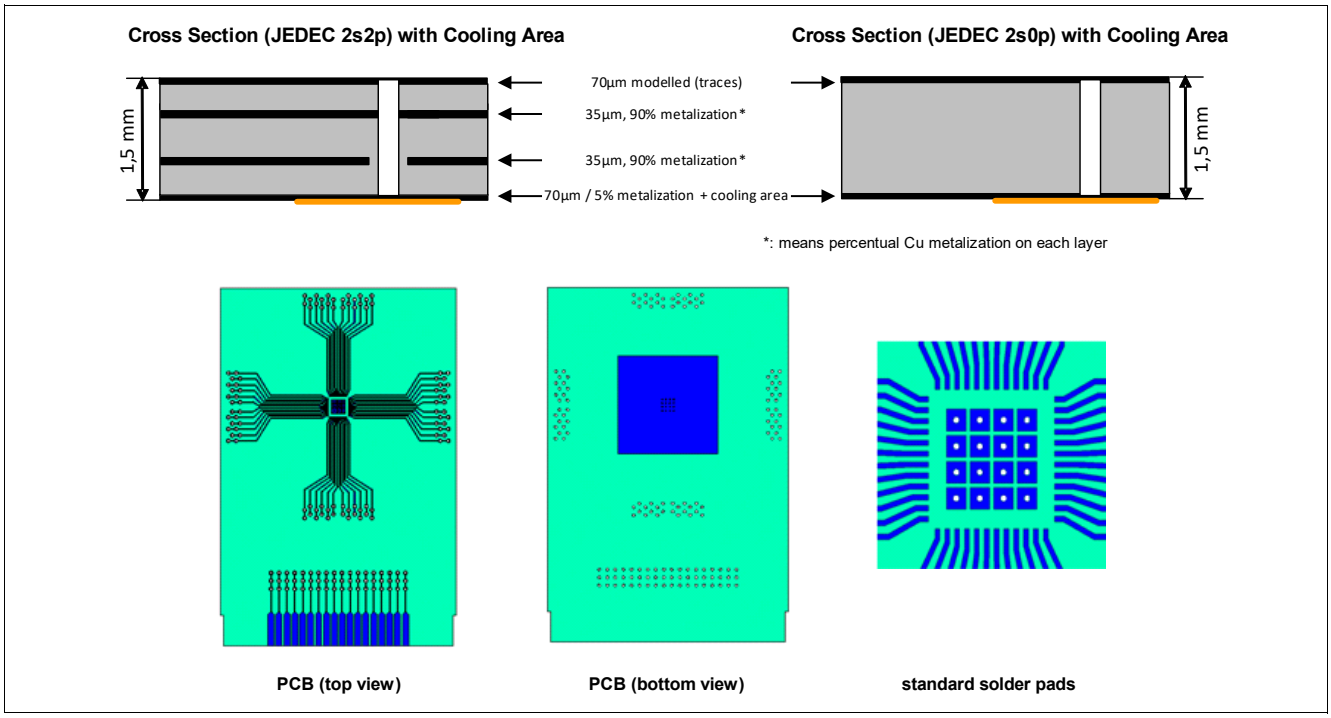

Figure 55 Board setup

Board setup is defined according to JESD 51-2,-5,-7.

Board: 76.2 × 114.3 × 1.5 mm^3 with 2 inner copper layers (35 µm thick), with thermal via array under the exposed pad contacting the first inner copper layer and 300 mm^2 cooling area on the bottom layer (70 µm).

16 Package outlines

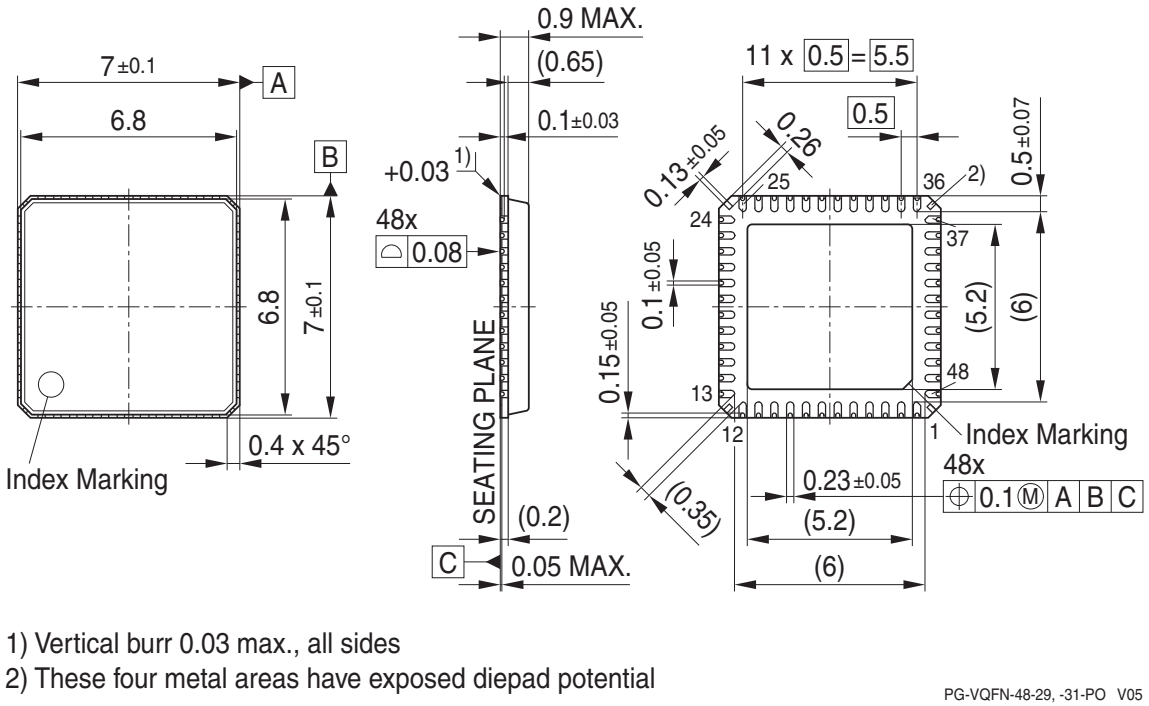

Figure 56 PG-VQFN-48 [1)]

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Further information on packages

https://www.infineon.com/packages

1) Dimensions in mm

17 Revision history

Revision	Date	Changes
2.0	2022-05-06	• Editorial changes • Added OrderabelPartNumber to the second page • Deleted 47 µH as an option for boost inductor in **Chapter 6.2.3** and **Chapter 15.1** • Added **Chapter 6.3.3** and **Chapter 6.3.4** with detailed description of the boost switch gate driver and the BSTG short circuit detection feature. Therefore replaced parameter P_6.5.27 and P_6.5.9 by new parameter in **Table 10** section “Boost switch gate driver” • Added parameter P_6.5.4 specifying current limit for buck regulator. No product change. • Correction within WD_CTRL register: Watchdog checksum bit is write only. Always read as 0. No product change. • Extended the capacitance range of output boost capacitor C2 within the application information (**Chapter 15.1**) • Pin configuration: Clearer wording for exposed pad connection to GND • Updated specification of charge device model to JEDEC JS-002 • Added clarification to P_10.3.1 (V_{WKth}): “Hysteresis included” • Corrected the output circuitry of FO1 in **Figure 35** and added explanation when the pull up transistors are switched. Added parameter R_{FO1} (P_12.3.12). No product change. • Hints for unused pins: Changed recommendation for N.C.-Pins to “leave open” to gain pin compatibility within the variants.
1.5	2019-09-27	Datasheet updated: • Editorial changes • General – changed “SBC Software development mode” to “SBC development mode” • Updated **Table 13** – added P_8.3.54 and P_8.3.55 (no product change) – tightened P_8.3.15 – tightened P_8.3.8 and P_8.3.42 by additional footnote • Added **Figure 53**
1.4	2018-11-20	Datasheet updated: Updated CAN description (**Figure 3**, **Figure 5.1.4**, **Figure 18**, **Chapter 8.2.4**).
1.3	2017-11-17	First revision of datasheet: Updated description **Chapter 13.8.1**.

Revision history

Revision	Date	Changes
1.2	2017-10-22	Preliminary Datasheet: Updated the **Figure 3** on SBC Normal Mode. Update the description of **Figure 21**. Removed the “optional” on **Figure 21**. Added P_8.3.58 (according to ISO11898-2:2016). Added P_4.1.28 (according to ISO11898-2:2016). Correct description **Chapter 13.5.1**. Correct description **Chapter 13.5.2** and updated **Figure 45**. Corrected the bit type of **SMPS_STAT** register. Corrected description on **Chapter 13.8.3** and **Figure 3**. Updated P_8.3.7 test conditions. Updated P_8.3.6 test conditions. Updated P_8.3.5 test conditions. Updated P_8.3.16 test conditions. Updated the description about LIN rearming in **Chapter 9.2.4**. Updated the description about CAN rearming in **Chapter 8.2.4**. Updated SYS_STAT_CTRL register note description. Updated **Chapter 9.2.6** description. Update **Chapter 8.2.7** description. Added chapter outcome pre and system tests verification. Added P_8.3.50, P_8.3.51, P_8.3.52 and P_8.3.53. Change description on **WK_LVL_STAT** and **Table 6** regarding the Fail-Safe Output behavior in case of watchdog trigger issue. Added the VCC2,UV Blanking time as internal parameter. Modified description **Chapter 8.2.6**. Add additional Note in SUP_STAT, BUS_STAT_1 and BUS_STAT_2 regarding the register content after one software reset. Update LIN wake-up description. Updated description **Chapter 13.8.3**. Updated parameter P_13.9.34. Updated FSI in Stop Mode and Restart Mode description. Updated max limit of P_12.3.11. Updated description DEV_STAT register Notes. Update test condition P_8.3.26.
1.1	2016-10-17	Target Datasheet updated: Added CAN FD timing parameters up to 5Mbps. Corrected the naming of **Figure 22** ($t_{LOOP,f}$ and $t_{LOOP,r}$). Updated the title of **Figure 41** and **Figure 42**. Improve the description of LIN wake-up pattern detection (**Chapter 9.2.4**). Updated footnote [5] on **Chapter 8.3** according to ISO11898-2. Added description 11_B on **WD_FAIL**: reserved (never achieved). Updated description **Chapter 13.2.3**.
1.0	2015-10-08	First Revision of Datasheet.

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