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APPLICATION NOTE 5570

Integrating Power Passives and Tactical Trade-Offs for Power Efficiency: Part 2, Balance - Work Through All the Choices

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Abstract: Power efficiency is a critical element of any design. Power management has become more complex, with every microamp counting in the search to extend battery life or minimize heat. This application note explores paradoxical engineering trade-offs, such as reducing ripple in switching power supplies and managing power in standby and sleep modes, to achieve increased power efficiency.

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Introduction

Power efficiency—we have all had to deal with it in our designs. Always a critical element of any design, today power management is a particularly complex and difficult topic because we must count every microamp to extend battery life or minimize heat. Sometimes being a design engineer feels like walking a tightrope. We solve by iteration, revisit the various operating modes, redefine the conditions, and balance trade-offs with application needs.

This application note is the second in a series on power efficiency. The first, application note 5569, "Integrating Power Passives and Tactical Trade-Offs



for Power Efficiency: Part 1, Harmony - Design like a Symphony Conductor," discusses how a design engineer must identify even small deficiencies in the power structure that could negatively impact power efficiency. Like a musical conductor, engineers control the power parameters that result in a harmonious, efficient system...or conversely, something less than ideal. In this application note, we continue to explore many of the contradictory, incongruous, and paradoxical engineering trade-offs available to us. If we look closely, in fact, we perform a balancing act with every design decision.

Lasting Impact of Seemingly Minor Changes

The universal challenge (or sometimes a curse) of circuit design is to reduce noise and ripple on power supplies with minimal components. This is at the heart of power-supply efficiency. It can be an elusive target and even appear nonsensical to the inexperienced. Yet, every seemingly tiny change has an impact.¹

A smart power designer moves an inductor an eighth of an inch and rotates it 90 degrees on a board. As a result, power efficiency increases 20%. Here is where power decoupling capacitors and the input source impedance or resistance are critical.² An inexperienced designer tries to save pennies and loses energy as heat when inferior capacitors with a higher equivalent series resistance (ESR) are used. Conversely, the effectiveness of a power-supply decoupling capacitor can be increased by adding series inductors, resistors, and ferrite beads to make them into lowpass filters. This technique helps when the application has a known sensitive bandwidth requirement. We can optimize the noise rejection and reduce decoupling capacitance size by understanding the bandwidth needs of the application.³ Let's take a closer look at some of the design challenges and trade-offs available to us, and how we can negotiate through the trade-off of each.⁴

Reducing Ripple

Switching power supplies have output ripple. One approach is to use filtering to reduce this ripple. Another approach is to create less ripple by using multiple switchers that are time-interleaved. The most common approach employs two- or three-phase devices. The fact that two or three synchronous ripple trains are combined reduces the ripple. Good, yes, but there is a trade-off with component count: typically two or three smaller inductors are necessary (one for each phase).⁵

Another major consideration is the ripple allowed on the voltage. In the case of a GSM[®] cell phone, the power pulses occur at 217Hz and its harmonics. The battery's internal impedance changes with the current drawn, thus making a decoupling capacitor across the battery important. How much capacitance is needed? There is no simple answer. It becomes an iterative process to optimize power decoupling. Board layout, capacitor size, and dielectrics have large effects on system complexity. Moreover, making the power as clean as possible without over cleaning could easily require additional power decoupling capacitors or capacitance.

Maximizing Current Use for Multiple Circuits

Let's talk about stacked circuits. Suppose that we have two sets of digital circuits that draw similar amounts of current. The circuits have few inputs and outputs and can run on approximately 2.5V, but the power supply is 5V. We can use a buck switching supply and make 2.5V with a little heat loss. How about stacking the circuits one on top of the other? For example, circuit 1 operates from ground to 2.5V and circuit 2 operates between 2.5V and 5V. In effect, we are using the current twice. The power dissipated in circuits 1 and 2 remains the same and no extra heat is produced by a buck converter. There is, however, a downside because the voltages going in and out of the circuits need to be translated up and down. Compared to the buck converter, translating a few signals is less complex, uses less power, and produces less heat.

Switching Supplies

Gyrators transform capacitance into inductance. While gyrators cannot store energy like a real inductor in a switching power supply, they are handy to use as lowpass power filters. Switching supplies can utilize tapped inductors, autotransformers, and actual transformers with multiple windings for isolation. The most efficient supplies are those that are matched to their loads. Knowing the system application allows one to regulate the master supply and allow subsupplies to operate open loop.⁶

Dissipating Power and Reducing Voltage

Logic circuits for complementary metal-oxide semiconductors (CMOS) (**Figure 1**) dissipate power in two ways: through leakage and through charging and discharging capacitance when switching. Leakage tends to be IC-process dependent. As the transistor size shrinks, the power voltage is reduced and the insulation layers become thinner. Leakage current, whether reverse-biased junction or subthreshold current, is generally lost power as it does not contribute to the job at hand. Operating or dynamic power is typically orders of magnitude larger than the leakage current. See **Figure 2**.



Figure 1. A typical CMOS input circuit.



Figure 2. Voltage on a CMOS input pin vs. power-supply current. Data are for the MAX5391 digital potentiometer.

There is more to say about switching: the higher the switching frequency, the higher the power loss. The biggest power savings with switching comes from reducing the operating voltage. Dividing the voltage by two, while maintaining the capacitance and frequency, reduces power consumption by a factor of four. This is explained by the formula $P = CV^2f$, where the terms are power, capacitance, voltage, and frequency. All the terms are linear except voltage, which is quadratic. This explains why voltage has such a big effect.

Voltage reduction brings other trade-offs. A lower voltage swing makes noise immunity problematic. If one chooses half-voltage clocks, one must translate the voltage up and down. The metal-oxide semiconductor (MOS) transistors become slower because the threshold voltages cannot scale with the voltage. This can be a major issue if you need to avoid disproportionate leakage current.

Reducing Capacitance

Reducing capacitance in a design has always been a good way to improve performance and lower power. There are two categories of capacitance: parasitic and unavoidable.^{7, 8} Since it is the product of capacitance and frequency that counts, we can trade off one for the other. We always reduce parasitic capacitance as much as possible; for unavoidable capacitance, we try to reduce the frequency.⁹ One effective method of reducing switching frequency is to stop the clock with clock gating. This eliminates any switching and removes power from circuits that are not necessary for current function. Some processors sleep with greatly reduced clock frequencies. Instead of megahertz clock rates, they may use a 32kHz clock. A 32kHz crystal is a common watch frequency. In this way, the processor can keep accurate track of time and wake up at precise intervals.

Managing Power in Standby and Sleep Modes

Understanding the application's ratio of operation to standby or sleep modes is essential in optimizing power consumption. The IC fabrication process greatly impacts power consumption in some subtle ways as we discuss below. Engineers started thinking about this some years ago when battery-operated devices had to last 10 years between battery changes. These devices include residential natural gas and water meters, and smoke and carbon monoxide (CO) alarms. Another striking example is a microwave oven with a clock. The clock is powered 24/7 and the microwave is used a few minutes a day, so the cost of power over a year may be equal for the oven and the clock. "Vampire power" is what we call the unseen power used during sleep or when operation is seemingly shut down.

We can use another hypothetical example to illustrate the issue. We have two IC processes. Scenario A draws 15mA during operation and 50nA in sleep mode. We drop the operating current for scenario B to 6mA, but the leakage goes up to 250nA. This leakage in scenario B severely impacts a battery-powered application where the device must sleep more than 99.99% of the time so that the battery lasts for years. A device that is awake one second a day is one part in 86,400. With scenario A, the total current used is 0.01932 amp seconds per day (i.e., 0.015 amp seconds during operation, 0.00432 amp seconds in sleep mode). With scenario B, the total is 0.02760 amp seconds (i.e., 0.006 amp seconds during operation and 0.0216 amp seconds in sleep mode). Surprise. Scenario B with the "improved", new lower operating current actually performs worse! At the risk of preaching too much, this example highlights the need to understand the application and interaction of the IC fabrication process very well.

How can we reduce standby power in a consumer appliance that needs remote control? There are

numerous possible answers. If a power indicator is necessary for customer confidence, then we can make the LED blink for a few microseconds, which is shorter than a human blink and thus is easily visible to people.

Another option to reduce standby power is to make the infrared radiation (IR) receiver sleep most of the time. To do this, the remote must be on for two seconds when the "ON" button is pressed; the "ON" IR code is modulated with repeated "ON" codes that are unique for that kind of appliance. The appliance, including the microprocessor for recognizing the IR code, is off as much as possible. When the IR receiver is awake, it has a bandpass filter that allows the IR modulation to pass and rectify its output. This makes the receiver ignore sunlight and IR remotes at other frequencies. When IR modulation is detected, the microprocessor turns on to see if the IR code matches the code for this appliance. It can use the remainder of the two-second "ON" command to do this. If the code matches, the appliance wakes up. If the code does not match, the appliance goes back to sleep. This approach reduces the circuit's operating power in standby mode and uses the bandpassed, rectified "ON" signal to minimize the chance of false wake-up calls.

There is another important situation to consider here. What happens if the input AC power is lost? Will the appliance stay off until the people use the remote to turn it on? Here we need to consider the safety of the appliance and perhaps the operating environment too. For example, we would not want an oven, hair dryer, or heating appliance to turn on without notice and start a fire.

Managing Modes to Extend Battery Life

Knowing the exact behavior of the power-supply load allows us to customize mode changes to match battery conditions. Circuits can be classified according to their ability to accept swings in voltage or regulation tolerance.¹⁰

- Analog circuits with strict regulation tolerance requirements: ADCs, DACs, RF power amplifiers
- Analog circuits with wider regulation tolerance: op amps and circuits with good power-supply rejection ratios (PSRRs)
- Digital circuits with tight voltage tolerances: inputs and outputs (I/Os) and external interfaces
- Digital circuits with medium-strict voltage tolerances: CPUs and memory
- Digital circuits with loose voltage tolerances: random logic and state machines

A cell phone is an example of how mode changes can extend battery life. When the battery is almost fully charged, a switch can supply the battery voltage directly to some circuits and use a buck converter for other circuits. As the battery voltage drops, the power from the buck converter can be switched to directly receive battery power. Further, as the battery voltage continues to drop, the voltage may need a boost converter to maximize battery life. From this example, we can appreciate how understanding the power load and its sensitivities can be an advantage for extending battery life.

A modern smartphone can operate in different modes, each of which has its own power issues. Here the key to successful power efficiency is understanding the application well. Under high power it can operate as a phone in full-duplex mode, simultaneously transmitting and receiving. The transmission probably appears continuous to the user. An engineer, however, might see either pulsating power as the system transmits in a time slot (time-division multiple access, or TDMA, an early Global System for Mobile (GSM) communication) or more continuous power consumption in a direct sequence spread-spectrum system (code-division multiple access, or CDMA).¹¹

Operating modes also change to accommodate specific operating configurations. Using the smartphone again as our example, it may have a dozen or more operational modes, such as airplane mode (no radio transmission); Wi-Fi[®]-only transmission; MP3 player; turn-by-turn directions with display on, off, or dim; gaming mode; text-only; camera; Skype[®]; eBook reader; and thousands of apps. In these modes lie opportunities to extend battery life by turning off unneeded circuitry.

Conclusion

Knowledge is power. Detailed knowledge of the application is the most powerful tool at the designer's disposal. It dictates the boundaries of the issue but still allows the clever engineer to think creatively, decrease the size and cost, increase battery life, and ultimately provide a pleasant operating experience for the user.

This may all seem obvious to most engineers and readers. Yet, the task and effort to optimize power efficiency are not as straightforward as they seem. With each challenge, and most certainly with each decision, the power designer must balance trade-offs as though walking on a tight rope. The interaction of even small changes on other seemingly unrelated circuits requires constant vigilance. So our design process must be iterative, changing small things to optimize the system's overall power consumption. This is also why a good experienced power designer can work magic in extending battery life.

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