

2.5V, 2GHz (3.2 Gbps) Ultra-Precision, Differential 1:2 LVDS Fanout Buffer with Internal Termination and Fail Safe Input

General Description

The SY89835U is a 2.5V, high-speed 2GHz differential Low Voltage Differential Swing (LVDS) 1:2 fanout buffer optimized for ultra-low skew applications. Within device skew is guaranteed to be less than 20ps over supply voltage and temperature. A unique Fail-Safe Input (FSI) protection prevents metastable conditions when no signal is present or when the selected input clock fails to a DC voltage (voltage between the pins of the differential input drops sufficiently below 100 mV).

MICREL

The SY89835U is part of Micrel's high-speed clock synchronization family. For applications that require a different I/O combination, consult Micrel's web site, and choose from a comprehensive product line of high-speed, low-skew fanout buffers, translators and clock generators.

Data sheets and support documentation can be found on Micrel's web site at: <u>www.micrel.com</u>.

Functional Block Diagram



Features

- Guaranteed AC performance over temperature and voltage:
 - DC-to > 3.2Gbps throughput
 - 210ps typical propagation delay (IN-to-Q)
 - <20ps within-device skew
 - <150ps rise/fall times
- Fail Safe Input
 - Prevents outputs from oscillating
- Ultra-low jitter design
 - <1ps_{RMS} cycle-to-cycle jitter
 - <10ps_{PP} total jitter
 - <1ps_{RMS} random jitter
 - <10ps_{PP} deterministic jitter
- High-speed LVDS outputs
- 2.5V ±5% power supply operation
- Industrial temperature range: -40°C to +85°C
- Available in 8-pin (2mm x 2mm) MLF™ package

Applications

- Clock or data distribution
- SONET clock or data distribution
- Fibre Channel clock or data distribution
- Gigabit Ethernet clock or data distribution

Markets

- DataCom
- Telecom
- Storage
- ATE
- Precision test and measurement

Precision Edge is a registered trademark of Micrel, Inc.

MLF and MicroLeadFrame are trademarks of Amkor Technology, Inc.

Micrel Inc. • 2180 Fortune Drive • San Jose, CA 95131 • USA • tel +1 (408) 944-0800 • fax + 1 (408) 474-1000 • http://www.micrel.com



Ordering Information⁽¹⁾

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89835UMG	MLF-8	Industrial	835 with Pb-Free bar-line indicator	NiPdAu Pb-Free
SY89835UMGTR ⁽²⁾	MLF-8	Industrial	835 with Pb-Free bar-line indicator	NiPdAu Pb-Free

Notes:

1. Contact factory for die availability. Dice are guaranteed at TA = 25°C, DC Electricals only.

2. Tape and Reel.

Pin Configuration



8-Pin MLF™ (MLF-8)

Pin Description

Pin Number	Pin Name	Pin Function
1	VCC	Positive Power Supply: Bypass with $0.1\mu F/(0.01\mu F)$ low ESR capacitor and place as close to VCC pin as possible. Power supply tolerance is ±5%.
2, 3	IN, /IN	Differential Inputs: This input pair is the differential signal input to the device. Input accepts DC-Coupled differential signals as small as 100mV ($200mV_{PP}$). The input is internally terminated with 100 Ω between IN and /IN. If the input swing falls below a certain threshold (typically 30mV), the Fail Safe Input (FSI) feature will guarantee a stable output by latching the output to its last valid state. Please refer to the "Input Interface Applications" section for more details.
4	GND	Ground. GND pins and exposed pad must be connected to the most negative potential of the device ground.
5, 6 7, 8	/Q1, Q1 /Q0, Q0	Differential Outputs (LVDS): Normally terminated with 100Ω across the pair (Q, /Q). See "LVDS Outputs" section, Figure 2a.

Truth Table

IN	/IN	Q	/Q
0	1	0	1
1	0	1	0

Absolute Maximum Ratings⁽¹⁾

Supply Voltage (V_{CC})	
LVDS Output Current (I _{OUT})	±10mA
Input Current	
Source or Sink Current on (IN, /IN)	±50mA
Lead Temperature (soldering, 20sec.)	.260°C
Storage Temperature (T _s)–65°C to -	+150°C

DC Electrical Characteristics⁽⁴⁾

 $T_A = -40^{\circ}C$ to +85°C, unless otherwise stated.

Operating Ratings⁽²⁾

Supply Voltage (V _{IN})	. +2.375V to +2.635V
Ambient Temperature (T _A)	–40°C to +85°C
Package Thermal Resistance ⁽³⁾	
MLF™	
Still-air (θ _{JA})	93°C/W
Junction-to-board (ψ_{JB})	

Symbol	Parameter	Condition	Min	Тур	Max	Units
V _{CC}	Power Supply Voltage Range		2.375	2.5	2.625	V
Icc	Power Supply Current	No load, max. V _{CC}		50	70	mA
$R_{\text{DIFF}_\text{IN}}$	Differential Input Resistance (IN-to-/IN)		90	100	110	Ω
V _{IH}	Input HIGH Voltage (IN, /IN)		1.2		V _{cc}	V
VIL	Input LOW Voltage (IN, /IN)		0		V _{IH} -0.1	V
V _{IN}	Input Voltage Swing (IN, /IN)	see Figure 2c	0.1		V _{cc}	V
V_{DIFF_IN}	Differential Input Voltage Swing (IN - /IN)	see Figure 2d	0.2			V
V_{IN_FSI}	Input Voltage Threshold that Triggers FSI			30	100	mV

LVDS Outputs DC Electrical Characteristics⁽⁴⁾

 V_{CC} = +2.5V ±5%, R_L = 100 Ω across the outputs; T_A = -40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Тур	Max	Units
V _{OUT}	Output Voltage Swing	See Figure 2c	250	325		mV
V _{DIFF_OUT}	Differential Output Voltage Swing	See Figure 2d	500	650		mV
V _{OCM}	Output Common Mode Voltage		1.125	1.20	1.275	V
ΔV_{OCM}	Change in Common Mode Voltage		-50		50	mV

Notes:

 Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

- 2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
- 3. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB. ψ_{JB} and θ_{JA} values are determined for a 4-layer board in still-air number, unless otherwise stated.
- 4. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

AC Electrical Characteristics⁽⁵⁾

 V_{CC} = +2.5V ±5%, R_L = 100 Ω across the outputs; T_A = -40°C to +85°C, unless otherwise stated.

Symbol	Paramet	ter	Condition		Min	Тур	Max	Units
f _{MAX}	Maximur	n Frequency	V _{OUT} > 200mV	NRZ Data	3.2			Gbps
				Clock	2.0	3.0		GHz
t _{PD}	Propaga	tion Delay IN-to-Q	V _{IN} : 100mV-200mV		150	300	500	ps
			> 200mV		100	210	400	
t _{Skew}	Within D	evice Skew	Note 6			5	20	ps
	Part-to-F	Part Skew	Note 7				200	ps
t _{Jitter}	Data	Random Jitter	Note 8				1	ps _{RMS}
		Deterministic Jitter	Note 9				10	ps _{PP}
	Clock	Cycle-to-Cycle Jitter	Note 10				1	ps _{RMS}
		Total Jitter	Note 11				10	ps _{PP}
t _{r,} t _f	Output F (20% to	Rise/Fall Times 80%)	At full output swing.		40	75	150	ps
	Duty Cyc	cle	Differential I/O		47		53	%

Notes:

5. High-frequency AC parameters are guaranteed by design and characterization.

6. Within device skew is measured between two different outputs under identical input transitions.

7. Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and no skew at the edges at the respective inputs.

8. Random jitter is measured with a K28.7 pattern, measured at $\leq f_{MAX}$.

9. Deterministic jitter is measured at 2.5Gbps with both K28.5 and 2²³–1 PRBS pattern.

10. Cycle-to-cycle jitter definition: the variation period between adjacent cycles over a random sample of adjacent cycle pairs. $t_{JITTER_CC} = T_n - T_{n+1}$, where T is the time between rising edges of the output signal.

 Total jitter definition: with an ideal clock input frequency of ≤ f_{MAX} (device), no more than one output edge in 10¹² output edges will deviate by more than the specified peak-to-peak jitter value.

Functional Description

Fail-Safe Input (FSI)

The input includes a special failsafe circuit to sense the amplitude of the input signal and to latch the outputs when there is no input signal present, or when the amplitude of the input signal drops sufficiently below $100mV_{PK}$ ($200mV_{PP}$).

Input Clock Failure Case

If the input clock fails to a floating, static, or extremely low signal swing, the FSI function will eliminate a metastable condition and guarantee a stable output signal. No ringing and no undetermined state will occur at the output under these conditions.

Please note that the FSI function will not prevent duty cycle distortion in case of a slowly deteriorating (but still toggling) input signal. Due to the FSI function, the propagation delay will depend upon the rise and fall time of the input signal and on its amplitude. Refer to "Typical Operating Characteristics" for detailed information.



Timing Diagrams

Typical Characteristics

 V_{CC} = 2.5V, GND = 0V, V_{IN} = 100mV, R_L = 100 Ω across the outputs, T_A = 25°C, unless otherwise stated.



100 8

400

600 800

INPUT RISE/FALL TIME (ps)

200

1200

Functional Characteristics

 V_{CC} = 2.5V, GND = 0V, V_{IN} = 100mV, R_L = 100 Ω across the outputs, T_A = 25°C, unless otherwise stated.





Input Stage



Figure 1. Simplified Differential Input Buffer

LVDS Outputs

LVDS specifies a small swing of 325mV typical, on a nominal 1.20V common mode above ground. The common mode voltage has tight limits to permit large variations in ground noise between an LVDS driver and receiver. These outputs can drive AC- or DC-coupled differential signals.

The SY89835U can drive long lengths of coaxial cables and FR4 traces. Table 1 below shows typical lengths of cables driven at different clock and data rates.

Clock/Data Rate	Coaxial Cable Length ⁽¹⁾	FR4 Cable Length ⁽²⁾
100MHz	4.5m	1.40m
622MHz	3.5m	0.85m
1.25Gbps	3.8m	0.80m
2.50Gbps	3.3m	0.50m

Table 1. Typical Lengths of Coaxial and FR4 Traces

Notes:

- Specifications for the center conductor of the coaxial cables used are "19 1/19 spcw OD .037 inch ± 0.001". These are 1m cables, p/n SB-142 manufactured by Harbour Industries. www.harbourind.com.
- The FR4 traces are 6.25mil wide and 6mil thick. Horizontal distance between adjacent traces is 7.75mil. These traces are fabricated on a Molex GBX Reference Backplane. www.molex.com.



Figure 2a. LVDS Differential Measurement



Figure 2b. LVDS Common Mode Measurement



Figure 2c. Single-Ended Swing



Figure 2d. Differential Swing

Input Interface Applications



Figure 3. LVDS Input Interface

Related Product and Support Documents

Part Number	Function	Data Sheet Link
SY89542U	2.5V, 3.2Gbps Dual, Differential 2:1 LVDS Multiplexer with Internal Termination	http://www.micrel.com/_PDF/HBW/sy89542u.pdf
SY89543L	3.3V, 3.2Gbps Dual, Differential 2:1 LVDS Multiplexer with Internal Termination	http://www.micrel.com/_PDF/HBW/sy89543u.pdf
SY89544U	2.5V, 3.2Gbps Differential 4:1 LVDS Multiplexer with Internal Input Termination	http://www.micrel.com/_PDF/HBW/sy89544u.pdf
	MLF™ Manufacturing Guidelines Exposed Pad Application Notes	http://www.amkor.com/products/notes- papers/MLF_appnote_0301.pdf
HBW Solutions	New Products and Termination Application Notes	http://www.micrel.com/product-info/products/sy89830u.shtml

Package Information



MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB http://www.micrel.com

The information furnished by Micrel in this data sheet is believed to be accurate and reliable. However, no responsibility is assumed by Micrel for

its use. Micrel reserves the right to change circuitry and specifications at any time without notification to the customer. Micrel Products are not designed or authorized for use as components in life support appliances, devices or systems where malfunction of a product can reasonably be expected to result in personal injury. Life support devices or systems are devices or systems that (a) are intended for surgical implant into the body or (b) support or sustain life, and whose failure to perform can be reasonably expected to result in a significant injury to the user. A Purchaser's use or sale of Micrel Products for use in life support appliances, devices or systems is a Purchaser's own risk

and Purchaser agrees to fully indemnify Micrel for any damages resulting from such use or sale.

© 2006 Micrel, Incorporated.