

- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input and Output Levels
- Outputs Are Precharged by Bias Voltage to Minimize Signal Distortion During Live Insertion
- Package Options Include Plastic Shrink Small-Outline (DB), Small-Outline (DW), and Thin Shrink Small-Outline (PW) Packages

description

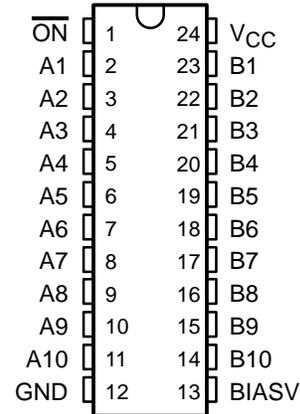
The SN74CBT6800 provides ten bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows bidirectional connections to be made while adding near-zero propagation delay. The device also precharges the B port to a user-selectable bias voltage (BIASV) to minimize live-insertion noise.

The SN74CBT6800 is organized as one 10-bit switch with a single enable (\overline{ON}) input. When \overline{ON} is low, the switch is on and port A is connected to port B. When \overline{ON} is high, the switch between port A and port B is open and the B port is precharged to BIASV through the equivalent of a 10-kΩ resistor.

The SN74CBT6800 is available in TI's shrink small-outline (DB) and thin shrink small-outline (PW) packages, which provide the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74CBT6800 is characterized for operation from -40°C to 85°C.

DB, DW, OR PW PACKAGE
(TOP VIEW)



FUNCTION TABLE

\overline{ON}	B1-B10	FUNCTION
L	A1-A10	Connect
H	BIASV	Precharge

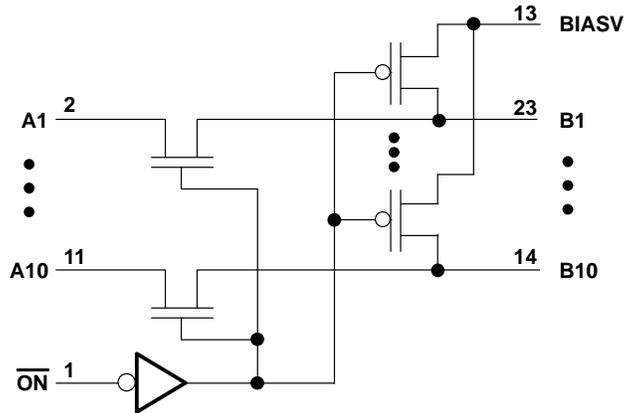


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SN74CBT6800
10-BIT BUS SWITCH
WITH PRECHARGED OUTPUTS FOR LIVE INSERTION

SCDS005G – MARCH 1993 – REVISED AUGUST 1996

logic diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Bias voltage range, BIASV	-0.5 V to 6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Continuous channel current	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2):	
DB package	0.6 W
DW package	1.7 W
PW package	0.7 W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
BIASV	Supply voltage	1.3	V_{CC}	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
T_A	Operating free-air temperature	-40	85	°C



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT	
V_{IK}		$V_{CC} = 4.5\text{ V}$,	$I_I = -18\text{ mA}$			-1.2	V	
I_I		$V_{CC} = 5.5\text{ V}$,	$V_I = 5.5\text{ V}$ or GND			±5	μA	
I_O		$V_{CC} = 4.5\text{ V}$,	BIASV = 2.4 V, $V_O = 0$	0.25			mA	
I_{CC}		$V_{CC} = 5.5\text{ V}$,	$I_O = 0$, $V_I = V_{CC}$ or GND			50	μA	
$\Delta I_{CC}‡$	Control pins	$V_{CC} = 3.6\text{ V}$,	One input at 2.7 V, Other inputs at V_{CC} or GND			2.5	mA	
C_i	Control pins	$V_I = 3\text{ V}$ or 0			3.5		pF	
$C_{O(OFF)}$		$V_O = 3\text{ V}$ or 0, Switch off			4.5		pF	
$r_{on}§$		$V_{CC} = 4\text{ V}$,	$V_I = 2.4\text{ V}$, $I_I = 15\text{ mA}$		14	20	Ω	
		$V_{CC} = 4.5\text{ V}$	$V_I = 0$,	$I_I = 64\text{ mA}$		5		7
			$V_I = 0$,	$I_I = 30\text{ mA}$		5		7
			$V_I = 2.4\text{ V}$,	$I_I = 15\text{ mA}$		10		15

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

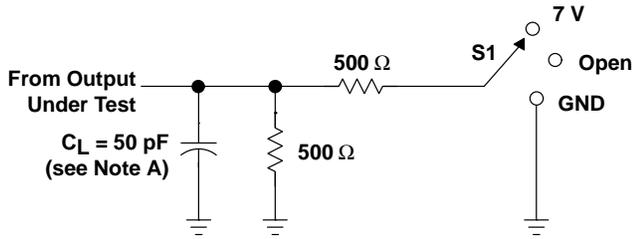
PARAMETER	TEST CONDITIONS	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		$V_{CC} = 4\text{ V}$		UNIT
				MIN	MAX	MIN	MAX	
$t_{pd}¶$		A or B	B or A		0.25		0.25	ns
t_{PZH}	BIASV = GND	\overline{ON}	A or B	3.1	8.1		9.1	ns
t_{PZL}	BIASV = 3 V			3.6	8.6		9.6	
t_{PHZ}	BIASV = GND	\overline{ON}	A or B	2.7	6.1		5.9	ns
t_{PLZ}	BIASV = 3 V			3	7.3		6.4	

¶ This parameter is warranted but not production tested. The propagation delay is based on the RC time constant of the typical on-state resistance of the switch and a load capacitance of 50 pF, when driven by an ideal voltage source (zero output impedance).

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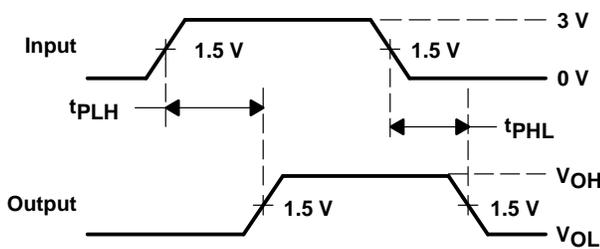
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PARAMETER MEASUREMENT INFORMATION

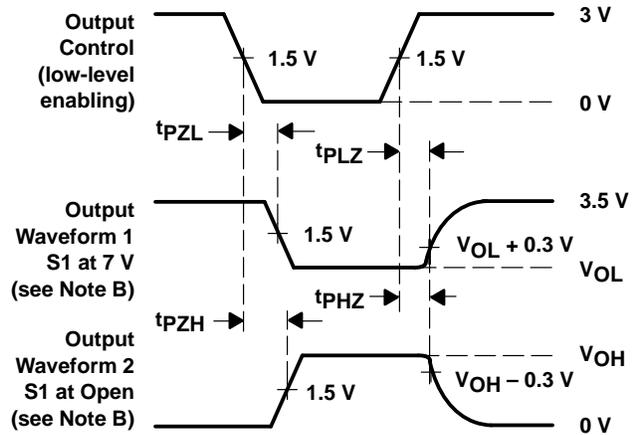


LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES**

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

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