

Aug 2012

FDB9403 F085

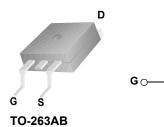
N-Channel Power Trench® MOSFET **40V, 110A, 1.2m**Ω

Features

- Typ $r_{DS(on)}$ = 1m Ω at V_{GS} = 10V, I_D = 80A
- Typ $Q_{g(tot)}$ = 164nC at V_{GS} = 10V, I_D = 80A
- UIS Capability
- RoHS Compliant
- Qualified to AEC Q101

Applications

- Automotive Engine Control
- Powertrain Management
- Solenoid and Motor Drivers
- Electronic Steering
- Integrated Starter/alternator
- Distributed Power Architectures and VRM
- Primary Switch for 12V Systems



FDB SERIES



MOSFET Maximum Ratings $T_J = 25$ °C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain to Source Voltage		40	V
V_{GS}	Gate to Source Voltage		±20	V
1	Drain Current - Continuous (V _{GS} =10) (Note 1)	T _C = 25°C	110	А
ID	Pulsed Drain Current	T _C = 25°C	See Figure4	^
E _{AS}	Single Pulse Avalanche Energy	(Note 2)	968	mJ
D	Power Dissipation		333	W
P_D	Derate above 25°C		2.22	W/°C
T _J , T _{STG}	Operating and Storage Temperature		-55 to + 175	°C
$R_{\theta JC}$	Thermal Resistance Junction to Case		0.45	°C/W
$R_{\theta JA}$	Maximum Thermal Resistance Junction to Ambient	(Note 3)	43	°C/W

Package Marking and Ordering Information

Device Markin	g Device	Package	Reel Size	Tape Width	Quantity
FDB9403	FDB9403_F085	TO-263AB	330mm	24mm	800 units

- Current is limited by bondwire configuration. Please see Fairchild AN 9757-1 for details on test method.
 Starting T_J = 25°C, L = 0.47mH, I_{AS} = 64A, V_{DD} = 40V during inductor charging and V_{DD} = 0V during time in avalanche.
 R_{0JA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design. The maximum rating presented here is based on mounting on a 1 in² pad of 2oz copper.

Electrical Characteristics $T_J = 25$ °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Cha	aracteristics					

B _{VDSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	40	-	-	V
1	Drain to Source Leakage Current	$V_{DS} = 40V$, $T_{J} = 29$	5°C -	-	1	μΑ
IDSS	Drain to Source Leakage Current	$V_{GS} = 0V$ $T_J = 17$	75°C(Note 4) -	-	1	mA
I _{GSS}	Gate to Source Leakage Current	V _{GS} = ±20V	-	-	±100	nA

On Characteristics

V _{GS(th)}	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_{D}$	= 250uA	2.0	3.13	4.0	٧
r	rpovery Urain to Source On Resistance	I _D = 80A,	$T_{J} = 25^{\circ}C$	-	1.0	1.2	$m\Omega$
'DS(on)		V _{GS} = 10V	$T_J = 175^{\circ}C(Note 4)$	ı	1.63	1.96	$m\Omega$

Dynamic Characteristics

C _{iss}	Input Capacitance)/ OF)/)/	0) /	-	12700	-	pF
C _{oss}	Output Capacitance		V _{DS} = 25V, V _{GS} = 0V, f = 1MHz		3195	-	pF
C _{rss}	Reverse Transfer Capacitance	1 - 1101112			493	-	pF
R_g	Gate Resistance	f = 1MHz		-	2.9	-	Ω
$Q_{g(ToT)}$	Total Gate Charge at 10V	V _{GS} = 0 to 10V	V _{DD} = 20V	-	164	213	nC
$Q_{g(th)}$	Threshold Gate Charge	$V_{GS} = 0$ to 2V	I _D = 80A	-	23	30	nC
Q_{gs}	Gate to Source Gate Charge		_	-	59	-	nC
Q _{gd}	Gate to Drain "Miller" Charge			-	25	-	nC

Switching Characteristics

t _{on}	Turn-On Time		-	-	56	ns
t _{d(on)}	Turn-On Delay Time		-	16	-	ns
t _r	Rise Time	V _{DD} = 20V, I _D = 80A,	-	19.5	-	ns
t _{d(off)}	Turn-Off Delay Time	$V_{GS} = 10V, R_{GS} = 1.5\Omega$	-	61	-	ns
t _f	Fall Time		-	46	-	ns
t _{off}	Turn-Off Time		-	-	171	ns

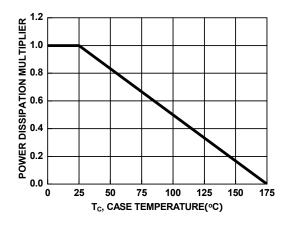
Drain-Source Diode Characteristics

V Course to Drain Diade Voltage	I _{SD} = 35A, V _{GS} = 0V	-	-	0.85	V	
V_{SD}	Source to Drain Diode Voltage	$I_{SD} = 15A, V_{GS} = 0V$	-	-	0.80	V
T _{rr}	Reverse Recovery Time	-I _F = 80A, dI _{SD} /dt = 100A/μs	-	96	125	ns
Q _{rr}	Reverse Recovery Charge	- IF - 60A, αι _{SD} /αι - 100A/μS	-	149	194	nC

Notes

4: The maximum value is specified by design at TJ = 175°C. Product is not tested to this condition in production.

Typical Characteristics



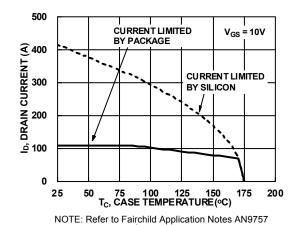


Figure 1. Normalized Power Dissipation vs Case Temperature

Figure 2. Maximum Continuous Drain Current vs Case Temperature

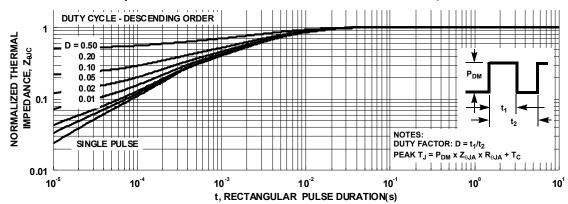


Figure 3. Normalized Maximum Transient Thermal Impedance

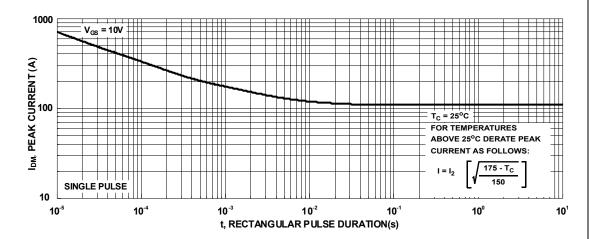


Figure 4. Peak Current Capability

10000 VE 1000 100 OPERATION IN THIS AREA MAY BE LIMITED BY rDS(on) TO = 25°C 1 100 VDS, DRAIN TO SOURCE VOLTAGE (V)

Typical Characteristics

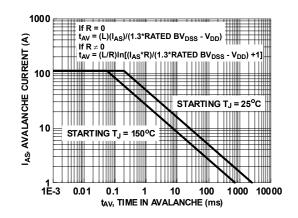
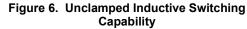
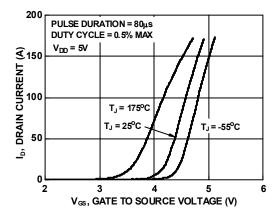


Figure 5. Forward Bias Safe Operating Area

NOTE: Refer to Fairchild Application Notes AN7514 and AN7515





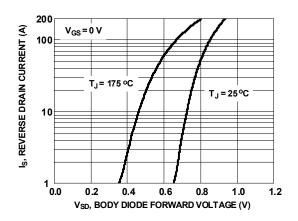
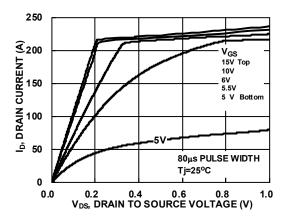


Figure 7. Transfer Characteristics

Figure 8. Forward Diode Characteristics



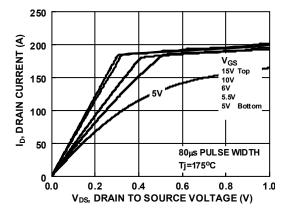


Figure 9. Saturation Characteristics

Figure 10. Saturation Characteristics

Typical Characteristics

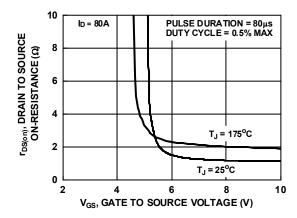


Figure 11. Rdson vs Gate Voltage

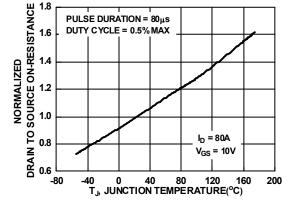


Figure 12. Normalized Rdson vs Junction Temperature

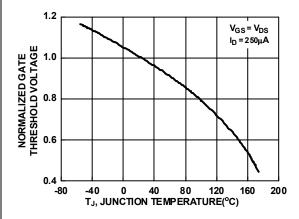


Figure 13. Normalized Gate Threshold Voltage vs Temperature

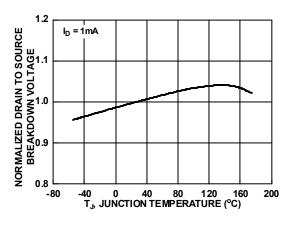


Figure 14. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

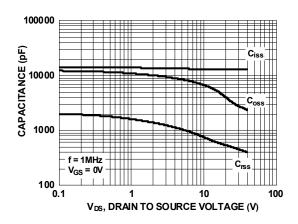


Figure 15. Capacitance vs Drain to Source Voltage

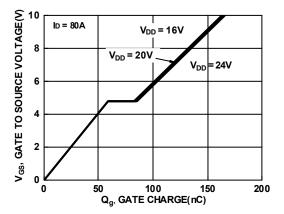


Figure 16. Gate Charge vs Gate to Source Voltage





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