

VALUE

600

10

6.1

HALOGEN

UNIT

V

Ω

nC

N-Channel Power MOSFET

600V, 1A, 10Ω

FEATURES

- Advanced planar process
- 100% avalanche tested
- Low R_{DS(ON)} 8Ω (Typ.)
- Low gate charge typical @ 6.1 nC (Typ.)
- Low Crss typical @4.2pF (Typ.)

APPLICATION

- Power Supply
- Lighting
- Charger



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KEY PERFORMANCE PARAMETERS

PARAMETER

 V_{DS}

R_{DS(on)} (max)

 Q_{g}

Notes: MSL 3 (Moisture Sensitivity Level) for TO-252 (D-PAK), SOT-223 per J-STD-020

PARAMETER	SYMBOL	IPAK/DPAK	SOT-223	UNIT
Drain-Source Voltage	V _{DS}	60	V	
Gate-Source Voltage	V _{GS}	±30		V
Continuous Drain Current ^(Note 1) $\frac{T_{C} = 25^{\circ}C}{T_{C} = 100^{\circ}C}$	- I _D	1	7	A
Pulsed Drain Current (Note 2)	I _{DM}	4		А
Total Power Dissipation @ $T_C = 25^{\circ}C$	P _{DTOT}	39	2.1	W
Single Pulsed Avalanche Energy (Note 3)	E _{AS}	5		mJ
Single Pulsed Avalanche Current (Note 3)	I _{AS}	1		А
Peak Diode Recovery dv/dt ^(Note 4)	dv/dt	4.	5	V/ns
Operating Junction and Storage Temperature Range	T _J , T _{STG}	- 55 to	+150	°C

PARAMETER	SYMBOL	IPAK/DPAK	SOT-223	UNIT		
Junction to Case Thermal Resistance	R _{ejc}	2.87		°C/W		
Junction to Ambient Thermal Resistance	R _{OJA}	110	60	°C/W		

Notes: $R_{\Theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins. $R_{\Theta JA}$ is guaranteed by design while $R_{\Theta CA}$ is determined by the user's board design. $R_{\Theta JA}$ shown below for single device operation on FR-4 PCB in still air.



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PARAMETER	CONDITIONS	SYMBOL	MIN	ТҮР	MAX	UNIT
Static (Note 5)						•
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250 \mu A$	BV _{DSS}	600			V
Drain-Source On-State Resistance	$V_{GS} = 10V, I_D = 0.5A$	R _{DS(ON)}		8	10	Ω
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	V _{GS(TH)}	2.5	3.5	4.5	V
Zero Gate Voltage Drain Current	$V_{DS} = 600V, V_{GS} = 0V$	I _{DSS}			10	μA
Gate Body Leakage	$V_{GS} = \pm 30V, V_{DS} = 0V$	I _{GSS}			±100	nA
Forward Transfer Conductance	$V_{DS} = 10V, I_{D} = 0.5A$	g _{fs}		0.8		S
Dynamic (Note 6)						
Total Gate Charge		Qg		6.1		
Gate-Source Charge	$V_{DS} = 480V, I_D = 1A,$	Q _{gs}		1.4		nC
Gate-Drain Charge	V _{GS} = 10V	Q _{gd}		3.3		
Input Capacitance		C _{iss}		138		
Output Capacitance	$V_{DS} = 25V, V_{GS} = 0V,$ f = 1.0MHz	C _{oss}		17.1		pF
Reverse Transfer Capacitance		C _{rss}		4.2		
Gate Resistance	F = 1MHz, open drain	R _g		12.5		Ω
Switching (Note 7)						
Turn-On Delay Time		t _{d(on)}		7.7		
Turn-On Rise Time	$V_{DD} = 300V, R_{G} = 25\Omega$	t _r		6.8		
Turn-Off Delay Time	$I_{\rm D} = 1$ A, $V_{\rm GS} = 10$ V	t _{d(off)}		15.3		ns
Turn-Off Fall Time	-	t _f		14.9		
Source-Drain Diode (Note 5)	·					
Diode Forward Voltage	$I_{\rm S}$ = 1A, $V_{\rm GS}$ = 0V	V _{SD}		0.9	1.4	V
Source Current	Integral reverse diode	I _S			1	
Source Current (Pulse)	In the MOSFET	I _{SM}			4	A

Notes:

1. Current limited by package.

- 2. Pulse width limited by the maximum junction temperature.
- 3. L = 10mH, I_{AS} = 1A, V_{DD} = 50V, R_G = 25 Ω , Starting T_J = 25^oC.
- 4. $I_{SD} \le 1A$, $V_{DD} \le BV_{DSS}$, di/dt $\le 200A/us$, Starting $T_J = 25^{\circ}C$.
- 5. Pulse test: $PW \le 300\mu s$, duty cycle $\le 2\%$.
- 6. For DESIGN AID ONLY, not subject to production testing.
- 7. Switching time is essentially independent of operating temperature.



ORDERING INFORMATION

PART NO.	PACKAGE	PACKING
TSM1NB60CH C5G	TO-251	75 pcs / Tube
TSM1NB60CP ROG	TO-252	2,500 pcs / 13" Reel
TSM1NB60CW RPG	SOT-223	2,500 pcs / 13" Reel

Note:

1. Compliant to RoHS Directive 2011/65/EU and in accordance to WEEE 2002/96/EC

2. Halogen-free according to IEC 61249-2-21 definition





MARKING DIAGRAM

#1

	Y = Year Code
50	M = Month Code for Halogen Free Product
1NB60 YML	O =Jan P =Feb Q =Mar R =Apr
	S =May T =Jun U =Jul V =Aug
	W =Sep X =Oct Y =Nov Z =Dec
	L = Lot Code (1~9, A~Z)
#1	





TO-252



SUGGESTED PAD LAYOUT



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SUGGESTED PAD LAYOUT (Unit: Millimeters)



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SUGGESTED PAD LAYOUT



MARKING DIAGRAM

1N YN	B60 /IL	
#1		

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