

LVPECL Divide by 1, Divide by 2 Clock Generator w/ Tri-State Compatible Outputs MLP8

FEATURES

- Selectable Divide Ratio
- Selectable Enable Priority and Threshold (CMOS or PECL)
- Tristate Compatible Outputs
- Input Buffer Powers Down when Disabled
- High BW [1.5GHz (± 1), 3.0GHz ($\div 2$)]
- 3V to 5.5V Power Supply
- -145dBc/Hz ($\div 1$) Typ Noise Floor
- -151dBc/Hz ($\div 2$) Typ Noise Floor
- RoHS Compliant Pb Free Packages

DESCRIPTION

The CTSLV394 is a $\div 1$ or $\div 2$ clock generation part specifically designed to accommodate Colpitts or Pierce based oscillators. The tri-state compatible outputs allow for on-the-fly switching of multiple oscillators on a common bus. Other features are incorporated to reduce board components. A voltage reference and input biasing allows for easy oscillator interface.

The CTSLV394 provides a $\div 2$ mode of operation for more frequency options and is selectable with a single connection. A selectable enable is also provided which doubles as a reset when the CTSLV394 is in $\div 2$ mode. With a single connection, the enable can be selected to operate as active high or active low.

ENGINEERING NOTES

The CTSLV394 is a specialized $\div 1$ or $\div 2$ clock generation part including an enable/reset function. The divide ratio is selected with the DIV-SEL pin/pad. When DIV-SEL is open (NC), the CTSLV394 functions as a standard receiver. If DIV-SEL is connected to V_{EE} , it functions as a $\div 2$ divider.

Enable (EN) functionality is selected with the EN-SEL pin/pad which has three valid states: open (NC), V_{EE} , or connected to V_{EE} via a $20\text{k}\Omega \pm 20\%$ resistor. Leaving EN-SEL open or connecting it to V_{EE} allows the EN pin/pad to function as an active high CMOS/TTL enable. When EN-SEL is open, an internal $75\text{k}\Omega$ pull-up resistor is selected which enables the outputs whenever EN is left open. When EN-SEL is connected to V_{EE} , an internal $75\text{k}\Omega$ pull-down resistor is selected which disables the outputs whenever EN is left open.

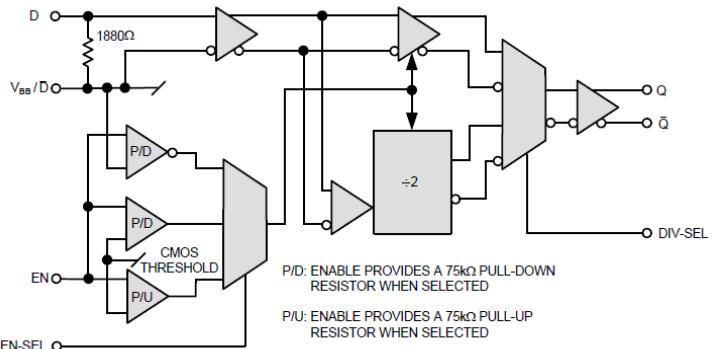
Connecting the EN-SEL to V_{EE} with a $20\text{k}\Omega$ resistor will allow the EN pin/pad to function as an active low PECL/ECL enable with an internal $75\text{k}\Omega$ pull-down resistor. In this mode, outputs are enabled when EN is left open (NC). The default logic condition can be overridden by connecting the EN to V_{CC} with an external resistor of $\leq 20\text{k}\Omega$. If the enable signal is CMOS (rail-to-rail) and the logic sense is active low (EN-SEL connected to V_{EE} with a $20\text{k}\Omega$ resistor), the EN pin/pad voltage swing must be reduced using two external resistors. Contact the factory for details.

When the CTSLV394 is disabled, the Q and \bar{Q} outputs are forced LOW and the input buffer is powered down to minimize feed through. This feature allows tri-state compatible parallel output connections. Multiple CTSLV394 chip outputs can be wired together. Since both outputs are forced LOW in the disable mode, an enabled CTSLV394 can drive the output lines without interference from the unselected units. In addition, the CTSLV394 can be used in parallel connection with PECL/ECL parts whose outputs are high impedance when disabled.

The EN pin/pad also functions as a reset when the $\div 2$ mode is selected. In the $\div 2$ mode, the counter resets when the outputs are disabled.

The CTSLV394 provides a V_{BB} with an 1880Ω internal bias resistor from D to V_{BB} . This feature allows AC coupling with minimal external components. The V_{BB} pin supports 1.5mA sink/source current and should be bypassed to ground or V_{CC} with a $0.01\text{ }\mu\text{F}$ capacitor.

BLOCK DIAGRAM



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ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings are those values beyond which device life may be impaired.

| Symbol | Characteristic | Condition | Rating | Unit |
|---------------------|---|----------------------|-------------|------|
| V _{CC} | PECL Power Supply | V _{EE} = 0V | 0 to + 6.0 | V |
| V _{I_PECL} | PECL Input Voltage | V _{EE} = 0V | 0 to + 6.0 | V |
| V _{EE} | ECL Power Supply | V _{CC} = 0V | -6.0 to 0 | V |
| V _{I_ECL} | ECL Input Supply | V _{CC} = 0V | -6.0 to 0 | V |
| I _{HGOUT} | Output Current | Continuous | 50 | mA |
| | | Surge | 100 | |
| T _A | Operating Temperature Range | - | -40 to +85 | °C |
| T _{STG} | Storage Temperature Range | - | -65 to +150 | °C |
| ESD _{HBM} | Human Body Model Electro Static Discharge | - | 2500 | V |
| ESD _{MM} | Machine Model Electro Static Discharge | - | 200 | V |
| ESD _{CDM} | Charged Device Model Electro Static Discharge | - | 2000 | V |

100K ECL DC Characteristics (V_{EE} = -3.0V to -5.5V, V_{CC} = GND)

| Symbol | Characteristic | -40°C | | 0°C | | 25°C | | 85°C | | Unit |
|-----------------|--|-----------------------|----------------------|-----------------------|----------------------|-----------------------|----------------------|-----------------------|----------------------|------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| V _{OH} | Output HIGH Voltage ¹ | -1085 | -880 | -1025 | -880 | -1025 | -880 | -1025 | -880 | mV |
| V _{OL} | Output LOW Voltage ¹ | -1900 | -1555 | -1900 | -1620 | -1900 | -1620 | -1900 | -1620 | mV |
| V _{IH} | Input HIGH Voltage D,EN (ECL) ² | -1165 | -740 | -1165 | -740 | -1165 | -740 | -1165 | -740 | mV |
| | Input HIGH Voltage EN (CMOS) ³ | V _{EE} +2000 | V _{CC} | mV |
| V _{IL} | Input LOW Voltage D,EN (ECL) ² | -1900 | -1475 | -1900 | -1475 | -1900 | -1475 | -1900 | -1475 | mV |
| | Input LOW Voltage EN (CMOS) ³ | V _{EE} | V _{EE} +800 | mV |
| V _{BB} | Reference Voltage | -1390 | -1250 | -1390 | -1250 | -1390 | -1250 | -1390 | -1250 | mV |
| I _{IH} | Input HIGH Current EN | | 150 | | 150 | | 150 | | 150 | µA |
| I _{IL} | Input LOW Current EN (ECL) ² | 0.5 | | 0.5 | | 0.5 | | 0.5 | | µA |
| | Input LOW Current EN (CMOS) ³ | -150 | | -150 | | -150 | | -150 | | |
| I _{EE} | Power Supply Current ¹ | | 34 | | 34 | | 34 | | 37 | mA |

¹ Specified with each output terminated through 50Ω resistors to V_{CC} -2V.

² EN-SEL connected to V_{EE} through a 20kΩ resistor.

³ EN-SEL connected to V_{EE} or left open (NC).

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100K LVPECL DC Characteristics ($V_{EE} = GND$, $V_{CC} = +3.3V$)

| Symbol | Characteristic | -40°C | | 0°C | | 25°C | | 85°C | | Unit |
|----------|--|-------|----------|------|----------|------|----------|------|----------|---------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| V_{OH} | Output HIGH Voltage ^{1,2} | 2215 | 2420 | 2275 | 2420 | 2275 | 2420 | 2275 | 2420 | mV |
| V_{OL} | Output LOW Voltage ^{1,2} | 1400 | 1745 | 1400 | 1680 | 1400 | 1680 | 1400 | 1680 | mV |
| V_{IH} | Input HIGH Voltage D,EN (ECL) ³ | 2135 | 2560 | 2135 | 2560 | 2135 | 2560 | 2135 | 2560 | mV |
| | Input HIGH Voltage EN (CMOS) ⁴ | 2000 | V_{CC} | 2000 | V_{CC} | 2000 | V_{CC} | 2000 | V_{CC} | mV |
| V_{IL} | Input LOW Voltage D,EN (ECL) ³ | 1400 | 1825 | 1400 | 1825 | 1400 | 1825 | 1400 | 1825 | mV |
| | Input LOW Voltage EN (CMOS) ⁴ | GND | 800 | GND | 800 | GND | 800 | GND | 800 | mV |
| V_{BB} | Reference Voltage ¹ | 1910 | 2050 | 1910 | 2050 | 1910 | 2050 | 1910 | 2050 | mV |
| I_{IH} | Input HIGH Current EN | | 150 | | 150 | | 150 | | 150 | μA |
| I_{IL} | Input LOW Current EN (ECL) ³ | 0.5 | | 0.5 | | 0.5 | | 0.5 | | μA |
| | Input LOW Current EN (CMOS) ⁴ | -150 | | -150 | | -150 | | -150 | | |
| I_{EE} | Power Supply Current ² | | 34 | | 34 | | 34 | | 37 | mA |

¹ For supply voltages other than 3.3V, use the ECL table values and ADD supply voltage value.

² Specified with each output terminated through 50Ω resistors to V_{CC} -2V.

³ EN-SEL connected to V_{EE} through a 20kΩ resistor.

⁴ EN-SEL connected to V_{EE} or left open (NC).

100K PECL DC Characteristics ($V_{EE} = GND$, $V_{CC} = +5.0V$)

| Symbol | Characteristic | -40°C | | 0°C | | 25°C | | 85°C | | Unit |
|----------|--|-------|----------|------|----------|------|----------|------|----------|---------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| V_{OH} | Output HIGH Voltage ^{1,2} | 3915 | 4120 | 3975 | 4120 | 3975 | 4120 | 3975 | 4120 | mV |
| V_{OL} | Output LOW Voltage ^{1,2} | 3100 | 3445 | 3100 | 3380 | 3100 | 3380 | 3100 | 3380 | mV |
| V_{IH} | Input HIGH Voltage D,EN (ECL) ³ | 3835 | 4260 | 3835 | 4260 | 3835 | 4260 | 3835 | 4260 | mV |
| | Input HIGH Voltage EN (CMOS) ⁴ | 2000 | V_{CC} | 2000 | V_{CC} | 2000 | V_{CC} | 2000 | V_{CC} | mV |
| V_{IL} | Input LOW Voltage D,EN (ECL) ³ | 3100 | 3525 | 3100 | 3525 | 3100 | 3525 | 3100 | 3525 | mV |
| | Input LOW Voltage EN (CMOS) ⁴ | GND | 800 | GND | 800 | GND | 800 | GND | 800 | mV |
| V_{BB} | Reference Voltage ¹ | 3610 | 3750 | 3610 | 3750 | 3610 | 3750 | 3610 | 3750 | mV |
| I_{IH} | Input HIGH Current EN | | 150 | | 150 | | 150 | | 150 | μA |
| I_{IL} | Input LOW Current EN (ECL) ³ | 0.5 | | 0.5 | | 0.5 | | 0.5 | | μA |
| | Input LOW Current EN (CMOS) ⁴ | -150 | | -150 | | -150 | | -150 | | |
| I_{EE} | Power Supply Current ² | | 34 | | 34 | | 34 | | 37 | mA |

¹ For supply voltages other than 3.3V, use the ECL table values and ADD supply voltage value.

² Specified with each output terminated through 50Ω resistors to V_{CC} -2V.

³ EN-SEL connected to V_{EE} through a 20kΩ resistor.

⁴ EN-SEL connected to V_{EE} or left open (NC).

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AC Characteristics ($V_{EE} = -3.0V$ to $-5.5V$; $V_{CC} = GND$ or $V_{EE} = GND$; $V_{CC} = +3.0V$ to $+5.5V$)

| Symbol | Characteristic | -40°C | | | 0°C | | | 25°C | | | 85°C | | | Unit |
|-------------------|--|-------|-----|------|-----|-----|------|------|-----|------|------|-----|------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| t_{PLH}/t_{PHL} | D to Q/ \bar{Q} ¹ | | | 450 | | | 450 | | | 450 | | | 450 | ps |
| | EN to Q_{HG}/Q_{bHG} ^{1,2} | | | 3000 | | | 3000 | | | 3000 | | | 3000 | ps |
| t_{SKew} | Duty Cycle Skew ³ | | 5 | 20 | | 5 | 20 | | 5 | 20 | | 5 | 20 | ps |
| V_{PP} (AC) | Input Swing ⁴ | 150 | | 1000 | 150 | | 1000 | 150 | | 1000 | 150 | | 1000 | mV |
| t_R/t_F | Output Rise/Fall ¹ (20% - 80%) | 100 | | 240 | 100 | | 240 | 100 | | 240 | 100 | | 240 | ps |

¹ Specified with each output terminated through 50Ω resistors to $V_{CC} - 2V$.

² Specified from 50% EN input edge to V_{OH} min to V_{OL} max of the Q/ \bar{Q} outputs.

³ Duty cycle skew is the difference between a t_{PLH} and t_{PHL} propagation delay through a device.

⁴ V_{PP} is the peak-to-peak differential input swing for which AC parameters are guaranteed.

Tri-state Compatible Operation

The outputs of the CTSLV394 are emitter followers as shown in the left side of Figure 1. When a part is disabled, both outputs are set in the LOW state. This allows a HIGH output from an enabled part to override a disabled output and pull the combined line HIGH as seen in the right hand side of Figure 1. When the enabled part output is LOW, the combined line remains LOW. If all connected CTS94 parts are disabled, both output lines will be in the LOW state. As another feature, while disabled, the input buffer is powered down to minimize feed through.

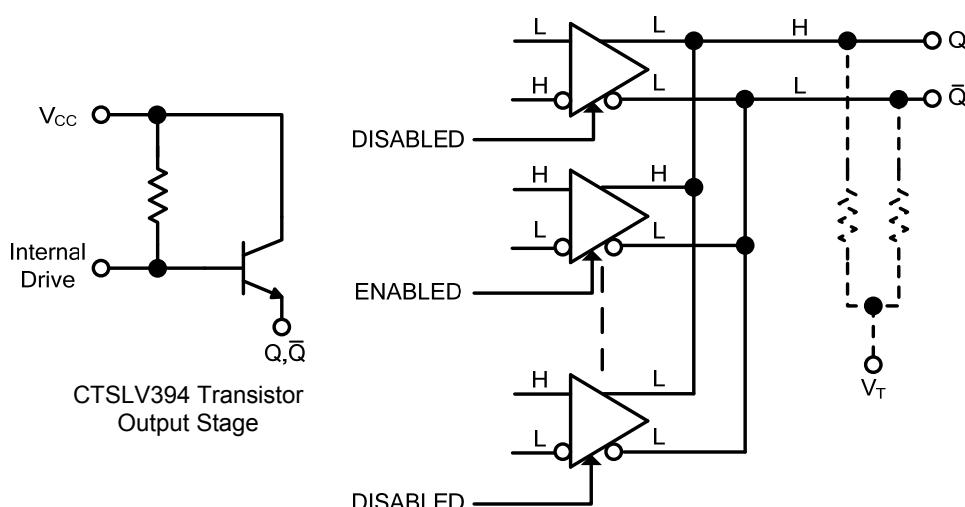


Figure 1: Typical Tri-state Operation

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Divide Truth Table

| DIV-SEL | ÷Ratio |
|------------------------------|--------|
| NC | ÷1 |
| V _{EE} ¹ | ÷2 |

¹ DIV-SEL connection must be $\leq 1W$.

Enable Truth Table

| EN-SEL | EN | Q | \bar{Q} |
|---------------------------------|----------------------------------|------|-----------|
| NC | CMOS Low or V _{EE} | Low | Low |
| | CMOS High, V _{CC} or NC | Data | Data |
| V _{EE} | CMOS Low, V _{EE} or NC | Low | Low |
| | CMOS High or V _{CC} | Data | Data |
| 20k Ω to V _{EE} | PECL Low, V _{EE} or NC | Low | Low |
| | PECL High or V _{CC} | Data | Data |

Figure 2 illustrates the timing sequences for the CTS LV394 in the $\div 1$ mode which is determined by leaving the DIV-SEL open (NC). It also illustrates the enable in the active High mode being controlled by a CMOS signal. This mode is determined by leaving the EN-SEL open (NC).

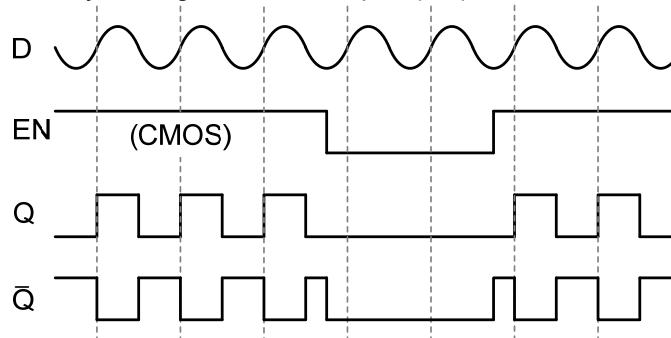


Figure 2

Figure 3 illustrates the timing sequences for the CTS LV394 in the $\div 2$ mode which is determined by connecting the DIV-SEL to V_{EE}. It also illustrates the enable in the active Low mode being controlled by a PECL signal. This mode is determined by connecting the EN-SEL to V_{EE} via a 20k Ω resistor.

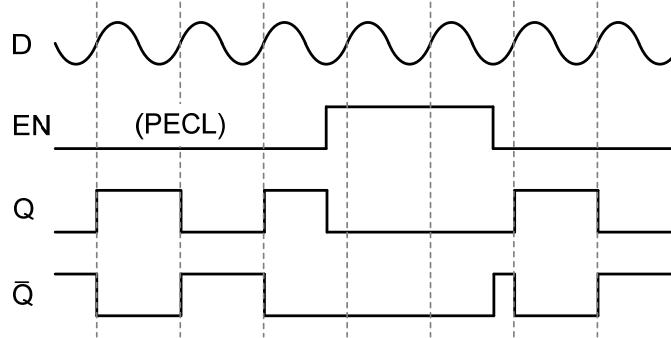
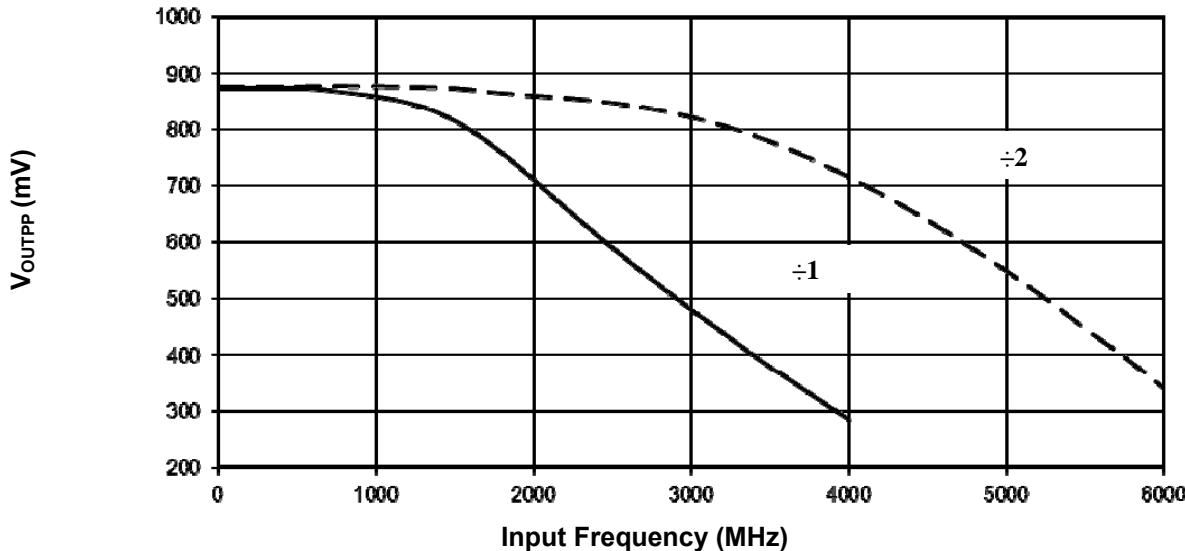


Figure 3

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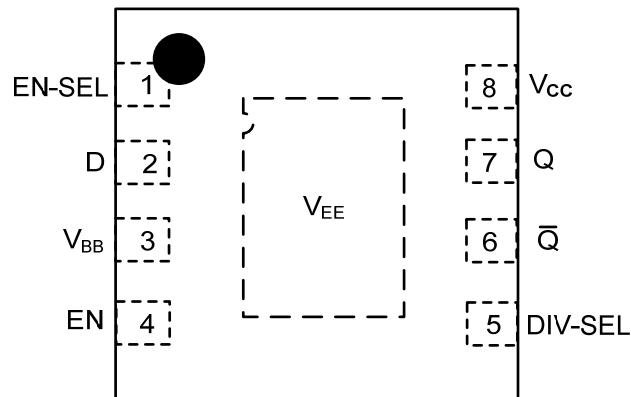


Typical Large Signal Output Swing
Measured with 750mV D input, Q/Q each terminated to V_{cc}-2V via 50Ω resistors.

Pin Description and Configuration

Pin Assignments

| Pin | Name | Type | Function |
|-----|-----------------|--------|------------------------|
| 1 | EN-SEL | Input | Enable Polarity Select |
| 2 | D | Input | Data Input |
| 3 | V _{BB} | Input | Reference Voltage |
| 4 | EN | Input | Output Enable |
| 5 | DIV-SEL | Input | Divide Select |
| 6 | Q̄ | Output | Inverted PECL Output |
| 7 | Q | Output | PECL Output |
| 8 | V _{CC} | Power | Positive Supply |
| 9 | V _{EE} | Power | Negative Supply |



PART ORDERING INFORMATION

| Part Number | Package | Marking |
|-------------|---------|-----------|
| CTSLV394NG | MLP8 | J4G / YWW |