AM273x Sitara™ Microcontrollers

1 Features

Processor Cores:

- Dual-core Arm® Cortex®-R5F MCU subsystem operating up to 400 MHz, highly-integrated for real-time processing
  - Dual-core Arm® Cortex®-R5F cluster supports dual-core and single-core operation
  - 32KB ICache and 32KB DCache per R5F core with SECDED ECC on all memories
  - Single-core: 128KB TCM per cluster (128KB TCM per R5F core)
  - Dual-core: 128KB TCM per cluster (64KB TCM per R5F core)
- TMS320C66x DSP core
  - Single core, 32-bit, floating point DSP
  - Operating at 450 MHz (14.4 GMAC)

Memory subsystem:

- Up to 5.0 MB On Chip RAM (OCSRAM)
  - Memory space sharable between DSP, MCU, and shared L3
  - 3.5625MB shared L3 memory
  - 960KB dedicated to Main subsystem
  - 384KB dedicated to DSP subsystem
- External Memory Interfaces (EMIF)
  - QSPI interface operating up to 67 MHz

System on Chip (SoC) Services and Architecture:

- 12x EDMA for various subsystems, MCU, DSP and Accelerator cores
- 5x Real-Time Interrupt (RTI) modules
- Mailbox system for Interprocessor Communication (IPC)
- JTAG/Trace interfaces for device debugging
- Clock source
  - 40.0 MHz crystal with internal oscillator
  - Supports external oscillator at 40/50 MHz
  - Supports externally driven clock (Square/Sine) at 40/50 MHz

High-speed Serial Interfaces:

- 10/100 Mbps Ethernet (RGMII/RMII/MII)
- Input: 2x 4-lane MIPI D-PHY CSI 2.0 Data
- Output: 4-lane Aurora/LVDS

General Connectivity Peripherals:

- General Purpose Analog to Digital Converters (GPADC)
  - 1x 9-channel ADC supporting up to 625 Ksps
- Digital Connectivity
  - 4x Serial Peripheral Interface (SPI) controllers operating up to 25 MHz
  - 3x Inter-Integrated Circuit (I2C) ports
  - 4x Universal Asynchronous Receiver-Transmitters (UART)

Industrial and control interfaces:

- 3x Enhanced Pulse-Width Modulator (ePWM)
- 1x Enhanced Capture Module (eCAP)
- 2x Modular Controller Area Network (MCAN) modules with CAN-FD support

Power Management:

- Simplified power sequencing and reduced number of power supply rails
- Dual voltage digital I/O supporting 3.3V and 1.8V operation

Security:

- Device Security
  - Programmable embedded Hardware Security Module (HSM)
  - Secure authenticated and encrypted boot support
  - Customer programmable root keys, symmetric keys (256 bit), Asymmetric keys (up to RSA-4K or ECC-512) with Key revocation capability
  - Crypto hardware accelerators - PKA with ECC, AES (up to 256 bit), TRNG/DRBG

Functional Safety:

- Functional Safety-Compliant targeted
  - Developed for functional safety applications
  - Documentation will be available to aid ISO 26262 functional safety system design
  - Hardware integrity up to ASIL B targeted
  - Safety-related certification
    - ISO 26262 certification by TÜV SÜD planned
- AEC-Q100 qualification targeted
- Operating Conditions
  - Automotive grade temperature range supported
  - Industrial grade temperature range supported

Package options:

- ZCE (285-pin) nFBGA package 13mm x 13mm, 0.65 mm pitch
- 45-nm technology
- Compact solution size

2 Applications

- Robotics
- Factory Automation Safety Guards
- Building Automation
- Automotive Audio
- Traffic Monitoring
- Machine Vision
- Avionics
- Industrial Transport

3 Description

The AM273x family of microcontrollers is a highly-integrated, high-performance microcontroller based on the Arm Cortex-R5F and a C66x floating-point DSP cores. The device enables Original-Equipment Manufacturers (OEM) and Original-Design Manufacturers (ODM) to quickly bring to market devices with robust software support, rich user interfaces, and high performance, through the maximum flexibility of a fully integrated, mixed processor solution.

With an integrated Hardware Security Module (HSM) and functional safety support built in, large, integrated RAM on die and a wide temperature range, the AM273x offers a safe, secure and cost effective solution for many industrial and automotive applications.

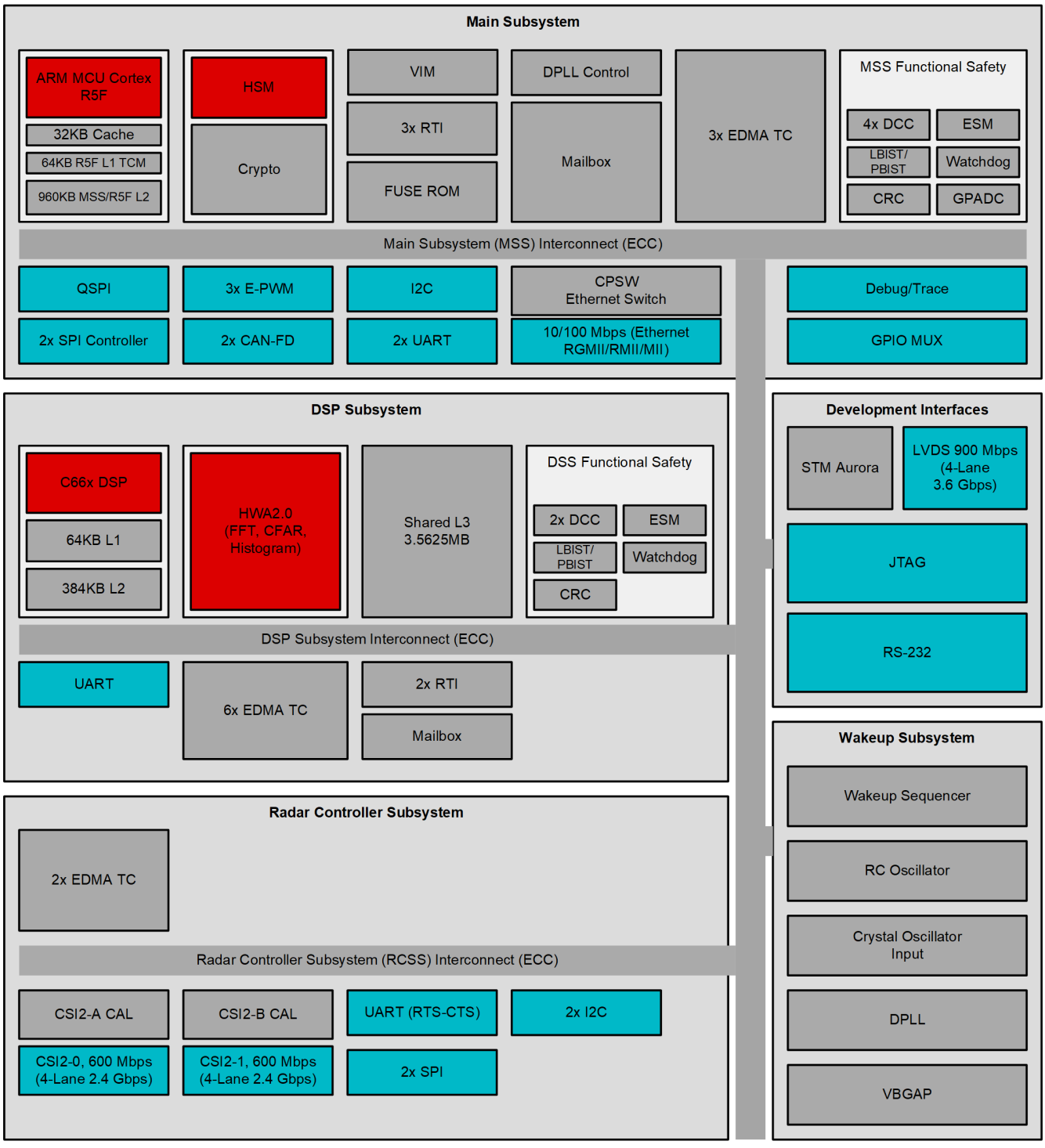
The AM273x device is provided as part of a complete platform solution including hardware reference designs, software drivers, DSP library, sample software configurations/applications, API guide, and user documentation.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE
AM2732ADRFGAZCER	nFBGA (285)	13 mm x 13 mm
AM2732ADRFGQZCERQ1	nFBGA (285)	13 mm x 13 mm

(1) For more information, see Section 11, *Mechanical, Packaging, and Orderable Information*.

3.1 Functional Block Diagram



Denotes associated peripheral interface

Note: For additional information on supported subsystems and peripherals please see the device comparison table in the datasheet.

Figure 3-1. AM273x Functional Block Diagram

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4 Revision History

Changes from December 17, 2021 to February 28, 2022 (from Revision * (December 2021) to Revision A (February 2022)) **Page**

- (Device Comparison): Added Q1, automotive device product links....5
- (ESD Ratings - Automotive): Updating HBM tolerance to +/-2kV....42
- (Power-On Hours (POH): Added extended industrial POH data. Modified automotive/industrial table formatting....42
- (Power-On Hours (POH)): Added automotive temperature profile table....42
- (Power-On Hours (POH)): Added industrial temperature profile table....43
- (Operating Performance Points): Changing order of device grades....45
- (Power Supply Sequencing and Reset Timing): Added further detail to the power-on/off sequence diagram. Added power-on/off sequence timing table for further clarification....47

5 Device Comparison

Table 5-1. Device Comparison

FUNCTION	AM2732	AM2732-Q1
On-chip memory	3.625 Mbytes	3.625 Mbytes
ASIL	B-Targeted	
PROCESSORS		
MCU Arm Cortex (R5F)	Yes	
DSP (C66x)	Yes	
RADAR FEATURES		
Hardware Accelerator 2.0	No	
PERIPHERALS		
Ethernet Interface RGMII, RMII, MII (10/100 ONLY)	Yes	
Serial Peripheral Interface (SPI) ports	4	
Quad Serial Peripheral Interface (QSPI)	1	
Inter-Integrated Circuit (I^2C) Interface	3	
Modular Controller Area Network (MCAN) modules with CAN-FD	2	
Universal Asynchronous Receiver-Transmitters (UART)	4	
Enhanced Pulse-Width Modulator (ePWM)	3	
Enhanced Capture Module (eCAP)	Yes	
Hardware in Loop (HIL/DMM)	Yes	
General Purpose ADC (9 Channels)	1	
4-lane Aurora/LVDS Debug	Yes	
4-lane MIPI D-PHY CSI2.0 (CSI2_RX0 and CSI2_RX1)	2	
JTAG/Trace	Yes	

5.1 Related Products

Sitara™ processors Broad family of scalable processors based on Arm® Cortex® cores with flexible accelerators, peripherals, connectivity and unified software support – perfect for sensors to servers. Sitara™ processors have the reliability needed for use in industrial applications.

AM273x Sitara™ microcontrollers AM273x microcontrollers enable industrial Ethernet networks, robust operation with extensive ECC on memories, and enhanced security features.

Sitara™ processors - Evaluation Modules TI provides Evaluation Modules (EVM) are also provided to help kick-start product development. See the AM273x GP EVM for more information.

Products to complete your design Review products that are frequently purchased or used in conjunction with this product to complete your design. See the following:

- 4x 5-A (20-A) multiphase buck converter PMIC with functional safety features for automotive SoCs LP8764-Q1
- Extended temperature, robust low-latency gigabit Ethernet PHY transceiver DP83867E
- Automotive high-speed CAN transceiver TCAN1044-Q1

6 Terminal Configuration and Functions

6.1 Pin Diagram

Figure 6-1 shows the pin locations for the 285-pin NanoFree™ (nFBGA) package (ZCE). Figure 6-2, Figure 6-3, Figure 6-4, and Figure 6-5 show the same pins, but split into four quadrants.

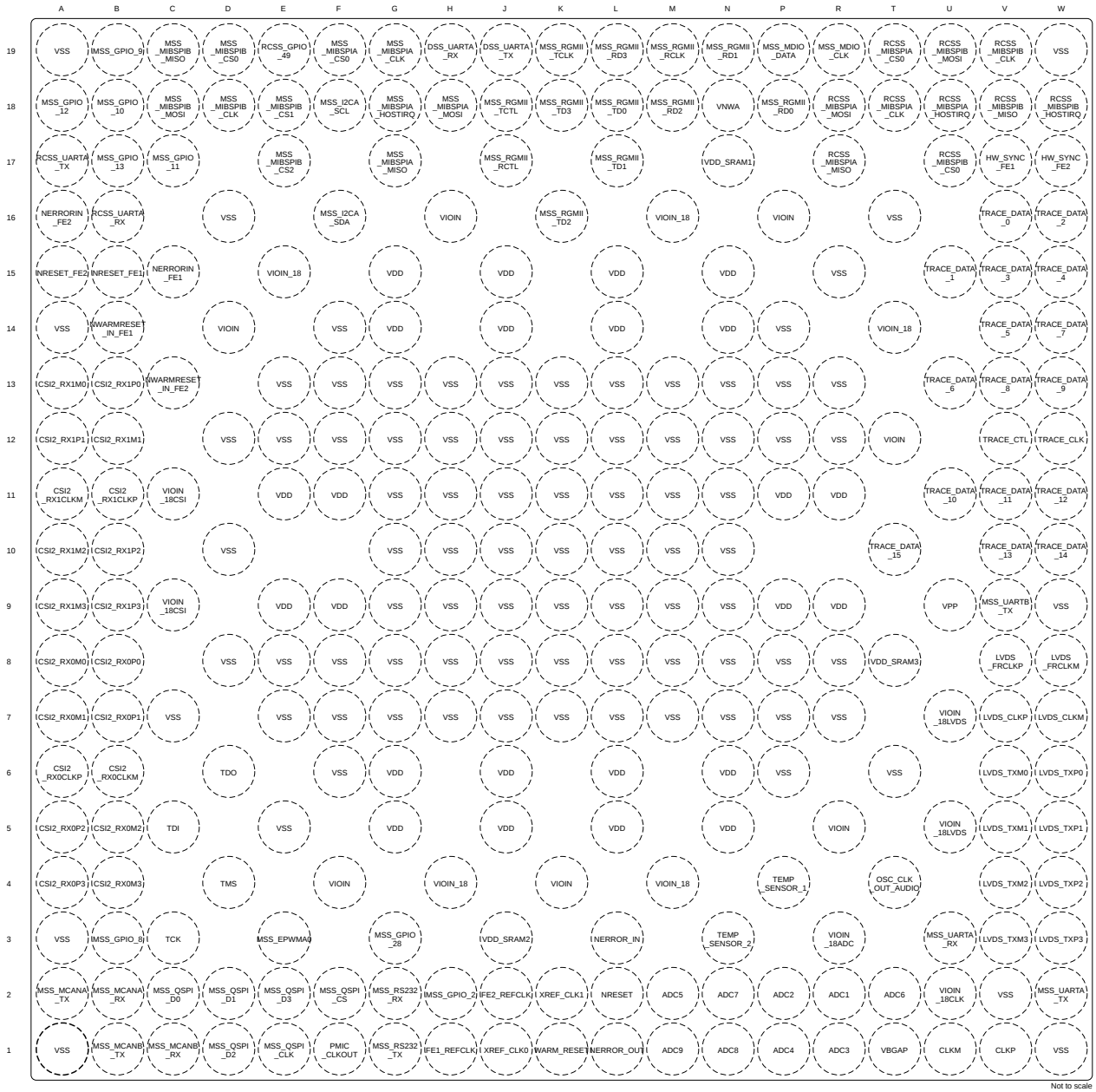


Figure 6-1. Pin Diagram (Top View)

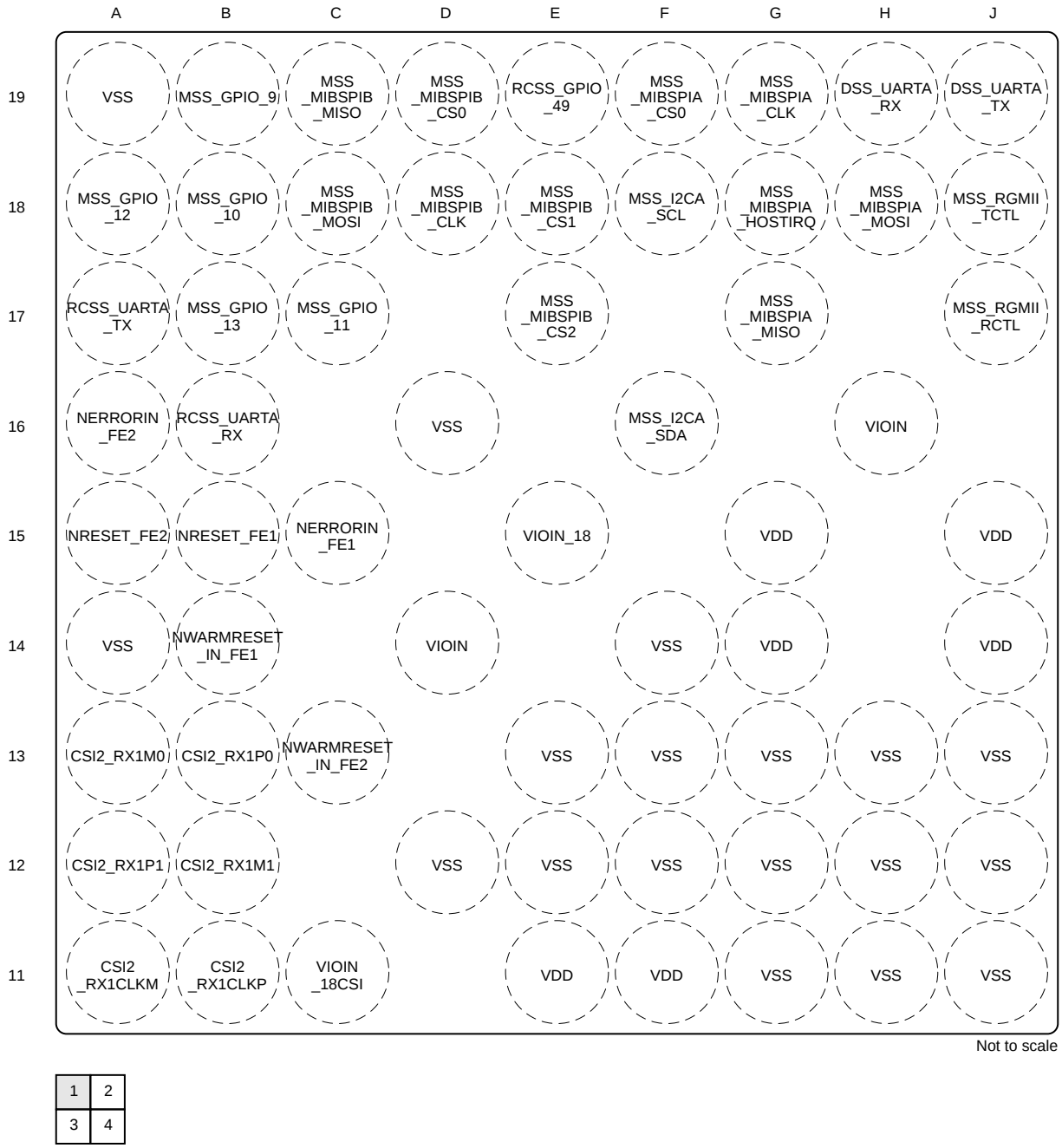


Figure 6-2. Top Left Quadrant (Top View)

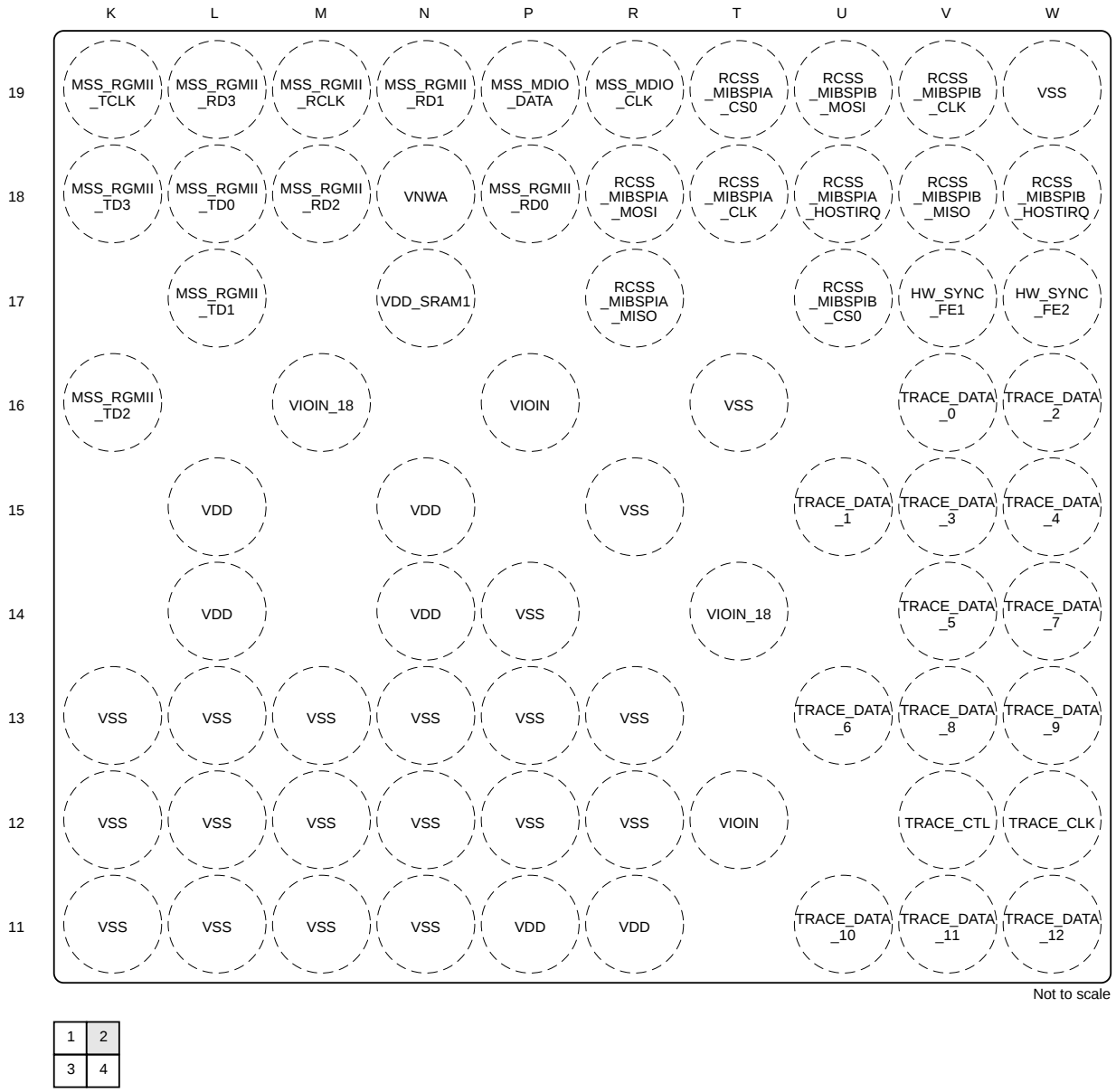


Figure 6-3. Top Right Quadrant (Top View)

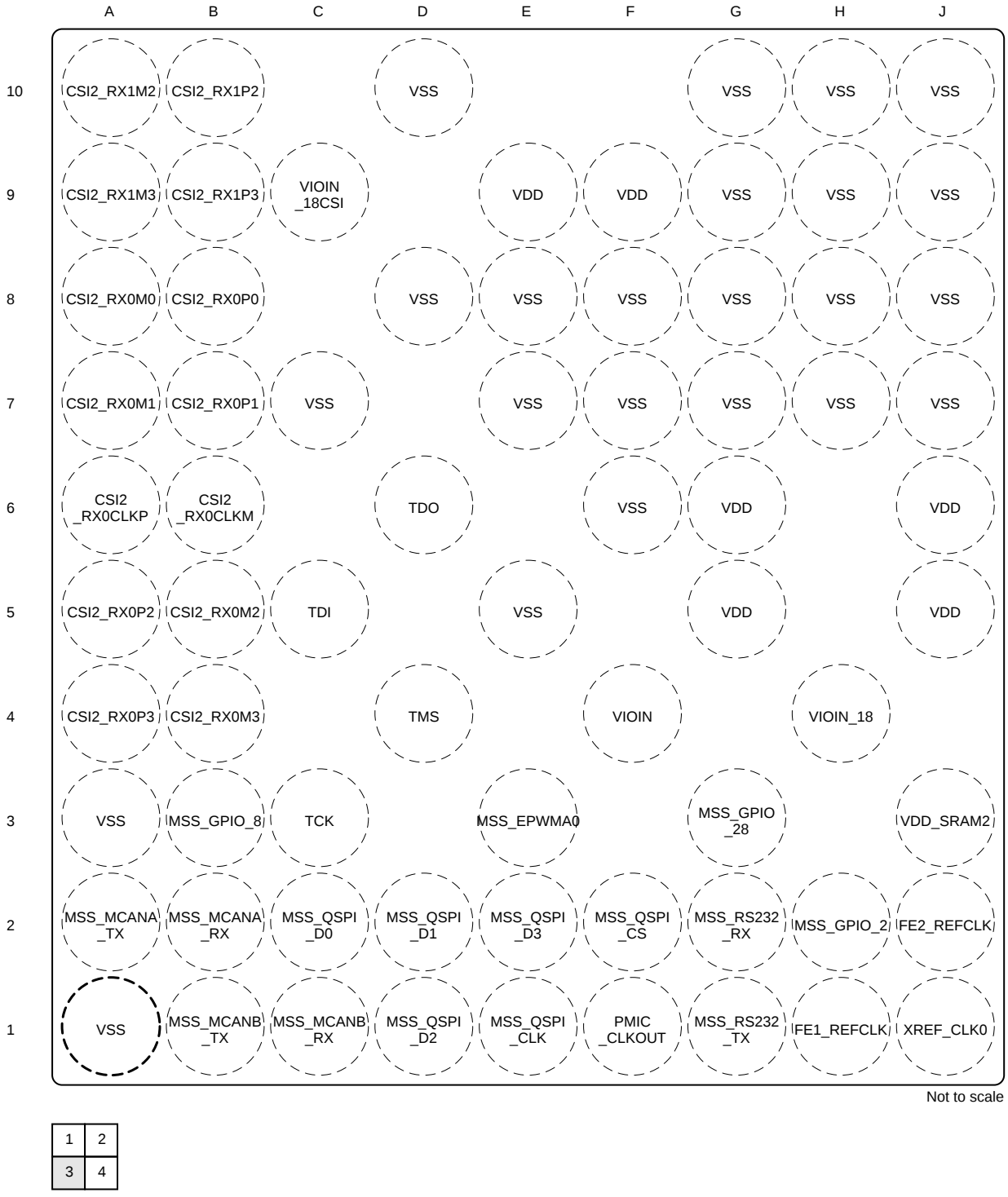


Figure 6-4. Bottom Left Quadrant (Top View)

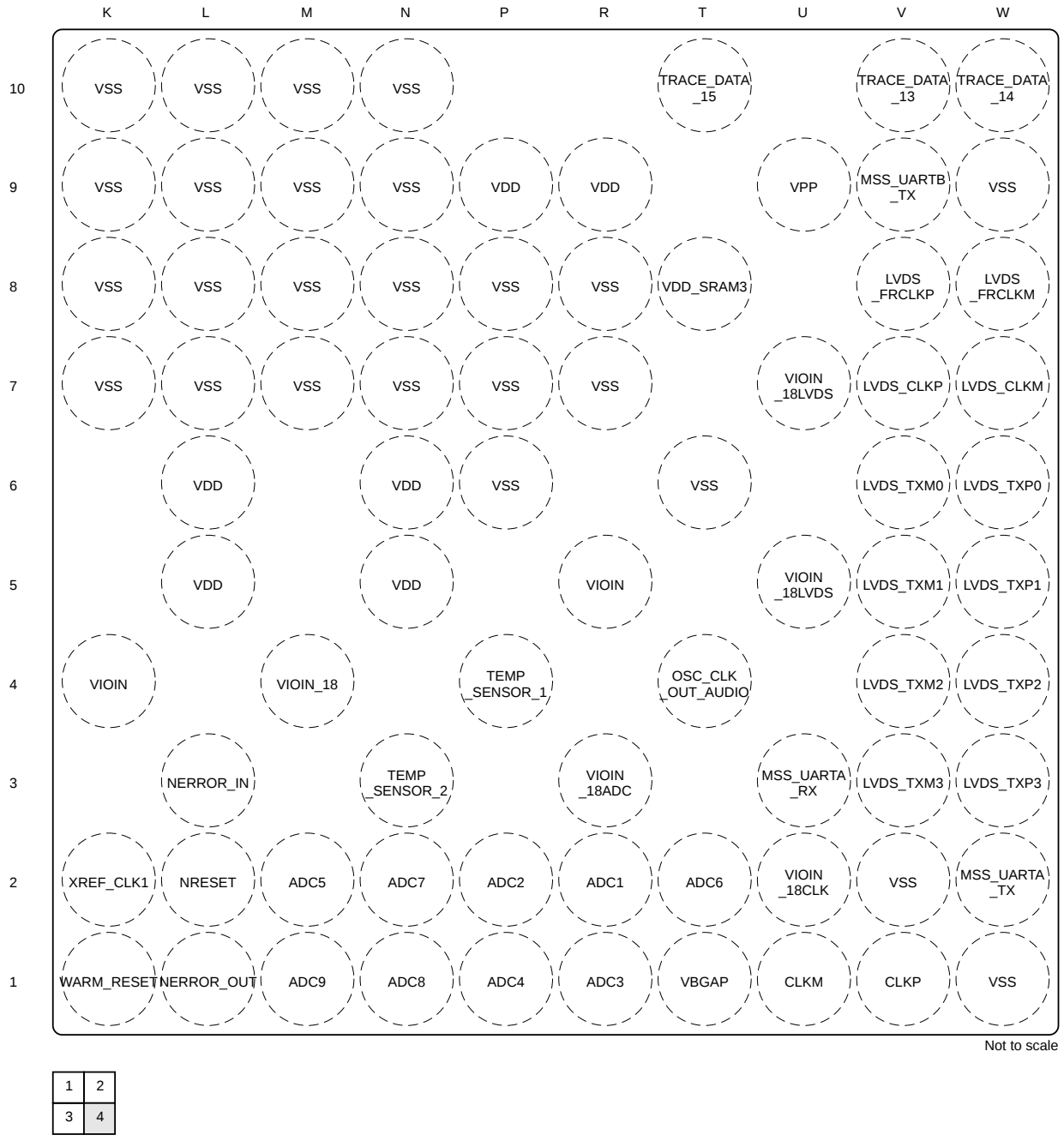


Figure 6-5. Bottom Right Quadrant (Top View)

6.2 Pin Attributes

The following list describes the contents of each column in Table 6-1, *Pin Attributes*:

1. **BALL NUMBER**: BGA coordinate of signal
2. **PAD NAME**: Associated pinmux pad coordinate for each BGA. The specific PINCNTL address register will be prefixed with this name. See the associated device-specific TRM for more information.
3. **BALL NAME**: Default signal name of BGA. Based on the default MUXMODE selection after reset release.
4. **SIGNAL NAME**: Each specific MUXMODE signal name.
5. **PINCNTL ADDRESS**: MSS_IOMUX register address for each pad control register.
6. **MUX MODE**: Supported FUNC_SEL field names in associated MSS_IOMUX configuration register.
7. **TYPE**: IO buffer type and direction associated with specific MSS_IOMUX FUNC_SEL field selection.
8. **BALL RESET STATE**: State of the terminal at power-on reset, during while **NRESET** is asserted.
9. **PULL TYPE (UP/DOWN)**: IO buffer default internal pull direction and type.
10. Modes and values marked RSVD are reserved and not available for customer configuration.

Table 6-1. Pin Attributes (ZCE285A Package)

BALL NUMBER[1]	PAD NAME[2]	BALL NAME[3]	SIGNAL NAME[4] [10]	PINCNTL ADDRESS[5]	MUX MODE[6] [10]	TYPE[7]	BALL RESET STATE[8]	PULL TYPE[9]
E18	PADAA	MSS_MIBSPIB_CS1	MSS_GPIO_12	0x020C 0000	0	IO	Output Disabled	Pull Down
			MSS_MIBSPIA_HOSTIRQ		1	I		
			RSVD		2	RSVD		
			RSVD		3	RSVD		
			RSVD		4	RSVD		
			RSVD		5	RSVD		
			MSS_MIBSPIB_CS1		6	O		
H1	PADAB	FE1_REFCLK	MSS_GPIO_13	0x020C 0004	0	IO	Output Disabled	Pull Down
			MSS_GPIO_0		1	IO		
			PMIC_CLKOUT		2	O		
			MSS_EPWM_TZ2		3	O		
			RSVD		4	RSVD		
			RSVD		5	RSVD		
			RSVD		6	RSVD		
			FE1_REFCLK		7	I		
			RSVD		8	RSVD		
			RSVD		9	RSVD		
			MSS_EPWMA1		10	O		
			MSS_EPWMB0		11	O		
J2	PADAC	FE2_REFCLK	MSS_GPIO_16	0x020C 0008	0	IO	Output Disabled	Pull Down
			MSS_GPIO_1		1	IO		
			RSVD		2	RSVD		
			MSS_EPWM_TZ1		3	I		
			RSVD		4	RSVD		
			RSVD		5	RSVD		
			RSVD		6	RSVD		
			FE2_REFCLK		7	I		
			RSVD		8	RSVD		
			RSVD		9	RSVD		
			RSVD		10	RSVD		
			RSVD		11	RSVD		
			DMM_MUX_IN		12	I		
			MSS_MIBSPIB_CS1		13	O		
			MSS_MIBSPIB_CS2		14	O		
			MSS_EPWMA_SYNCI		15	I		
C1	PADAD	MSS_MCANB_RX	MSS_GPIO_19	0x020C 000C	0	IO	Output Disabled	Pull Up
			MSS_MIBSPIA_MOSI		1	O		
			MSS_MCANA_RX		2	I		

Table 6-1. Pin Attributes (ZCE285A Package) (continued)

BALL NUMBER[1]	PAD NAME[2]	BALL NAME[3]	SIGNAL NAME[4] [10]	PINCNTL ADDRESS[5]	MUX MODE[6] [10]	TYPE[7]	BALL RESET STATE[8]	PULL TYPE[9]
			RSVD		3	RSVD		
			RSVD		4	RSVD		
			RSVD		5	RSVD		
			RSVD		6	RSVD		
			RSVD		7	RSVD		
			DSS_UARTA_TX		8	O		
			MSS_MCANB_RX		9	IO		
			MSS_I2CA_SCL		10	IO		
B1	PADAE	MSS_MCANB_TX	MSS_GPIO_20	0x020C 0010	0	IO	Output Disabled	Pull Up
			MSS_MIBSPIA_MISO		1	I		
			MSS_MCANA_TX		2	O		
			RSVD		3	RSVD		
			RSVD		4	RSVD		
			RSVD		5	RSVD		
			RSVD		6	RSVD		
			RSVD		7	RSVD		
			RSVD		8	RSVD		
			MSS_MCANB_TX		9	IO		
			MSS_I2CA_SDA		10	IO		
B2	PADAF	MSS_MCANA_RX	MSS_GPIO_3	0x020C 0014	0	IO	Output Disabled	Pull Up
			MSS_MIBSPIA_CLK		1	O		
			RCOSC_CLK		2	O		
			RSVD		3	RSVD		
			RSVD		4	RSVD		
			RSVD		5	RSVD		
			MSS_MCANB_RX		6	IO		
			DSS_UARTA_TX		7	O		
			RSVD		8	RSVD		
			MSS_MCANA_RX		9	I		
A2	PADAG	MSS_MCANA_TX	MSS_GPIO_30	0x020C 0018	0	IO	Output Disabled	Pull Up
			MSS_MIBSPIA_CS0		1	O		
			RCOSC_CLK		2	O		
			RSVD		3	RSVD		
			RSVD		4	RSVD		
			RSVD		5	RSVD		
			MSS_MCANB_TX		6	O		
			RSVD		7	RSVD		
			RSVD		8	RSVD		
			MSS_MCANA_TX		9	IO		
C18	PADAH	MSS_MIBSPIB_MOSI	MSS_GPIO_21	0x020C 001C	0	IO	Output Disabled	Pull Up
			MSS_MIBSPIB_MOSI		1	O		
			MSS_I2CA_SDA		2	IO		
			MSS_EPWMA0		3	O		
			RSVD		4	RSVD		
			RSVD		5	RSVD		
			RSVD		6	RSVD		
			MSS_MCANB_RX		7	I		
C19	PADAI	MSS_MIBSPIB_MISO	MSS_GPIO_22	0x020C 0020	0	IO	Output Disabled	Pull Up
			MSS_MIBSPIB_MISO		1	I		
			MSS_I2CA_SCL		2	IO		
			MSS_EPWMB0		3	O		
			RSVD		4	RSVD		
			RSVD		5	RSVD		
			DSS_UARTA_TX		6	O		

Table 6-1. Pin Attributes (ZCE285A Package) (continued)

BALL NUMBER[1]	PAD NAME[2]	BALL NAME[3]	SIGNAL NAME[4] [10]	PINCNTL ADDRESS[5]	MUX MODE[6] [10]	TYPE[7]	BALL RESET STATE[8]	PULL TYPE[9]
			MSS_MCANB_TX		7	O		
D18	PADAJ	MSS_MIBSPIB_CLK	MSS_GPIO_5	0x020C 0024	0	IO	Output Disabled	Pull Up
			MSS_MIBSPIB_CLK		1	O		
			MSS_UARTA_RX		2	I		
			MSS_EPWMC0		3	O		
			RSVD		4	RSVD		
			RSVD		5	RSVD		
			MSS_UARTB_TX		6	O		
			RSVD		7	RSVD		
			MSS_MCANA_RX		8	I		
D19	PADAK	MSS_MIBSPIB_CS0	MSS_GPIO_4	0x020C 0028	0	IO	Output Disabled	Pull Up
			MSS_MIBSPIB_CS0		1	O		
			MSS_UARTA_TX		2	O		
			RSVD		3	RSVD		
			RSVD		4	RSVD		
			RSVD		5	RSVD		
			MSS_UARTB_TX		6	O		
			RSVD		7	RSVD		
			RSVD		8	RSVD		
			MSS_MCANA_TX		9	O		
C2	PADAL	MSS_QSPI_D0	MSS_GPIO_8	0x020C 002C	0	IO	Output Disabled	Pull Down
			MSS_QSPI_D0		1	IO		
			MSS_MIBSPIB_MISO		2	I		
			RSVD		3	RSVD		
			RSVD		4	RSVD		
			RSVD		5	RSVD		
			RSVD		6	RSVD		
			RSVD		7	RSVD		
D2	PADAM	MSS_QSPI_D1	MSS_GPIO_9	0x020C 0030	0	IO	Output Disabled	Pull Down
			MSS_QSPI_D1		1	IO		
			MSS_MIBSPIB_MOSI		2	O		
			RSVD		3	RSVD		
			RSVD		4	RSVD		
			RSVD		5	RSVD		
			RSVD		6	RSVD		
			RSVD		7	RSVD		
			MSS_MIBSPIB_CS2		8	O		
D1	PADAN	MSS_QSPI_D2	MSS_GPIO_10	0x020C 0034	0	IO	Output Disabled	Pull Up
			MSS_QSPI_D2		1	IO		
			RSVD		2	RSVD		
			RSVD		3	RSVD		
			RSVD		4	RSVD		
			RSVD		5	RSVD		
			RSVD		6	RSVD		
			RSVD		7	RSVD		
			MSS_MCANA_TX		8	O		
E2	PADAO	MSS_QSPI_D3	MSS_GPIO_11	0x020C 0038	0	IO	Output Disabled	Pull Up
			MSS_QSPI_D3		1	IO		
			RSVD		2	RSVD		
			RSVD		3	RSVD		
			RSVD		4	RSVD		
			RSVD		5	RSVD		
			RSVD		6	RSVD		
			RSVD		7	RSVD		

Table 6-1. Pin Attributes (ZCE285A Package) (continued)

BALL NUMBER[1]	PAD NAME[2]	BALL NAME[3]	SIGNAL NAME[4] [10]	PINCNTL ADDRESS[5]	MUX MODE[6] [10]	TYPE[7]	BALL RESET STATE[8]	PULL TYPE[9]
			MSS_MCANA_RX		8	I		
E1	PADAP	MSS_QSPI_CLK	MSS_GPIO_7	0x020C 003C	0	IO	Output Disabled	Pull Down
			MSS_QSPI_CLK		1	O		
			MSS_MIBSPIB_CLK		2	O		
			RSVD		3	RSVD		
			RSVD		4	RSVD		
			RSVD		5	RSVD		
			DSS_UARTA_TX		6	O		
F2	PADAQ	MSS_QSPI_CS	MSS_GPIO_6	0x020C 0040	0	IO	Output Disabled	Pull Up
			MSS_QSPI_CS		1	O		
			MSS_MIBSPIB_CS0		2	O		
L3	PADAR	NERROR_IN	NERROR_IN	0x020C 0044	0	I	Hi-Z (Open-Drain)	Pull Disabled
K1	PADAS	WARM_RESET	WARM_RESET	0x020C 0048	0	IO	Hi-Z (Open-Drain)	Pull Disabled
L1	PADAT	NERROR_OUT	NERROR_OUT	0x020C 004C	0	O	Hi-Z (Open-Drain)	Pull Disabled
C3	PADAU	TCK	MSS_GPIO_17	0x020C 0050	0	IO	Output Disabled	Pull Down
			TCK		1	I		
			MSS_UARTB_TX		2	O		
			RSVD		3	RSVD		
			RSVD		4	RSVD		
			RSVD		5	RSVD		
			RSVD		6	RSVD		
			RSVD		7	RSVD		
			MSS_MCANA_TX		8	O		
D4	PADAV	TMS	MSS_GPIO_18	0x020C 0054	0	IO	Output Disabled	Pull Up
			TMS		1	I		
			RSVD		2	RSVD		
			RSVD		3	RSVD		
			RSVD		4	RSVD		
			RSVD		5	RSVD		
			MSS_MCANA_RX		6	I		
C5	PADAW	TDI	MSS_GPIO_23	0x020C 0058	0	IO	Output Disabled	Pull Up
			TDI		1	I		
			MSS_UARTA_RX		2	I		
			RSVD		3	RSVD		
			RSVD		4	RSVD		
			RSVD		5	RSVD		
			RSVD		6	RSVD		
			DSS_UARTA_RX		7	I		
D6	PADAX	TDO	MSS_GPIO_24	0x020C 005C	0	IO	Output Enabled	Pull Disabled
			TDO		1	O		
			MSS_UARTA_TX		2	O		
			RSVD		3	RSVD		
			RSVD		4	RSVD		
			RSVD		5	RSVD		
			MSS_UARTB_TX		6	O		
			RSVD		7	RSVD		
			RSVD		8	RSVD		
			NDMM_EN		9	I		
E3	PADAY	MSS_EPWMA0	MSS_GPIO_25	0x020C 0060	0	IO	Output Disabled	Pull Down
			MCU_CLKOUT		1	O		
			RSVD		2	RSVD		
			RSVD		3	RSVD		

Table 6-1. Pin Attributes (ZCE285A Package) (continued)

BALL NUMBER[1]	PAD NAME[2]	BALL NAME[3]	SIGNAL NAME[4] [10]	PINCNTL ADDRESS[5]	MUX MODE[6] [10]	TYPE[7]	BALL RESET STATE[8]	PULL TYPE[9]
			RSVD		4	RSVD		
			RSVD		5	RSVD		
			RSVD		6	RSVD		
			RSVD		7	RSVD		
			RSVD		8	RSVD		
			RSVD		9	RSVD		
			RSVD		10	RSVD		
			RSVD		11	RSVD		
			MSS_EPWMA0		12	IO		
			RSVD		13	RSVD		
			RSVD		14	RSVD		
			OBS_CLKOUT		15	O		
H2	PADAZ	MSS_GPIO_2	MSS_GPIO_26	0x020C 0064	0	IO	Output Disabled	Pull Down
			MSS_GPIO_2		1	IO		
			RSVD		2	RSVD		
			RSVD		3	RSVD		
			RSVD		4	RSVD		
			RSVD		5	RSVD		
			RSVD		6	RSVD		
			MSS_UARTB_TX		7	O		
			RCSS_GPIO_34		8	IO		
			RSVD		9	RSVD		
			PMIC_CLKOUT		10	O		
			RSVD		11	RSVD		
			RSVD		12	RSVD		
			RSVD		13	RSVD		
			MSS_EPWM_TZ0		14	I		
F1	PADBA	PMIC_CLKOUT	MSS_GPIO_27	0x020C 0068	0	IO	Output Disabled	Pull Down
			PMIC_CLKOUT		1	O		
			OBS_CLKOUT		2	O		
			RSVD		3	RSVD		
			RSVD		4	RSVD		
			RSVD		5	RSVD		
			RSVD		6	RSVD		
			RSVD		7	RSVD		
			RSVD		8	RSVD		
			RSVD		9	RSVD		
			RSVD		10	RSVD		
			MSS_EPWMA1		11	O		
			MSS_EPWMB0		12	O		
G3	PADBB	MSS_GPIO_28	MSS_GPIO_28	0x020C 006C	0	IO	Output Disabled	Pull Down
			SYNC_IN		1	I		
			RSVD		2	RSVD		
			RCSS_MCASPB_AHCLKR		3	I		
			RSVD		4	RSVD		
			RSVD		5	RSVD		
			MSS_UARTB_RX		6	I		
			DMM_MUX_IN		7	I		
			DSS_UARTA_RX		8	I		
E17	PADBC	MSS_MIBSPIB_CS2	MSS_GPIO_29	0x020C 0070	0	IO	Output Disabled	Pull Down
			RSVD		1	RSVD		
			RCOSC_CLK		2	I		
			RSVD		3	RSVD		
			RSVD		4	RSVD		

Table 6-1. Pin Attributes (ZCE285A Package) (continued)

BALL NUMBER[1]	PAD NAME[2]	BALL NAME[3]	SIGNAL NAME[4] [10]	PINCNTL ADDRESS[5]	MUX MODE[6] [10]	TYPE[7]	BALL RESET STATE[8]	PULL TYPE[9]
			RSVD		5	RSVD		
			RSVD		6	RSVD		
			RSVD		7	RSVD		
			RSVD		8	RSVD		
			DMM_MUX_IN		9	I		
			MSS_MIBSPIB_CS1		10	O		
			MSS_MIBSPIB_CS2		11	O		
			MSS_EPWMB0		12	O		
			MSS_EPWMB1		13	O		
G2	PADBD	MSS_RS232_RX	MSS_GPIO_15	0x020C 0074	0	IO	Output Disabled	Pull Up
			MSS_RS232_RX		1	I		
			MSS_UARTA_RX		2	I		
			RSVD		3	RSVD		
			RSVD		4	RSVD		
			RSVD		5	RSVD		
			RSVD		6	RSVD		
			MSS_UARTB_RX		7	I		
			MSS_MCANA_RX		8	I		
			MSS_I2CA_SCL		9	IO		
			MSS_EPWMB0		10	O		
			MSS_EPWMB1		11	O		
			MSS_EPWMC0		12	O		
G1	PADBE	MSS_RS232_TX	MSS_GPIO_14	0x020C 0078	0	IO	Output Enabled	Pull Disabled
			MSS_RS232_TX		1	O		
			RSVD		2	RSVD		
			RSVD		3	RSVD		
			RSVD		4	RSVD		
			MSS_UARTA_TX		5	O		
			MSS_UARTB_TX		6	O		
			RSVD		7	RSVD		
			RSVD		8	RSVD		
			RSVD		9	RSVD		
			MSS_MCANA_TX		10	O		
			MSS_I2CA_SDA		11	IO		
			MSS_EPWMA0		12	O		
			MSS_EPWMA1		13	O		
			NDMM_EN		14	I		
			MSS_EPWMB0		15	O		
V16	PADBF	TRACE_DATA_0	TRACE_DATA_0	0x020C 007C	0	IO	Output Disabled	Pull Down
			MSS_GPIO_31		1	IO		
			DMM0		2	I		
			RSVD		3	RSVD		
			MSS_UARTA_TX		4	O		
			RSVD		5	RSVD		
			RSVD		6	RSVD		
			RCSS_MCASPC_DAT1		7	IO		
			RSVD		8	RSVD		
			RSVD		9	RSVD		
			MSS_I2CA_SDA		10	IO		
U15	PADBG	TRACE_DATA_1	TRACE_DATA_1	0x020C 0080	0	IO	Output Disabled	Pull Down
			RCSS_GPIO_32		1	IO		
			DMM1		2	I		
			MSS_EPWMC_SYNCI		3	I		
			MSS_UARTA_RX		4	I		

Table 6-1. Pin Attributes (ZCE285A Package) (continued)

BALL NUMBER[1]	PAD NAME[2]	BALL NAME[3]	SIGNAL NAME[4] [10]	PINCNTL ADDRESS[5]	MUX MODE[6] [10]	TYPE[7]	BALL RESET STATE[8]	PULL TYPE[9]
			RSVD		5	RSVD		
			RSVD		6	RSVD		
			RCSS_MCASPC_DAT0		7	IO		
			RSVD		8	RSVD		
			RSVD		9	RSVD		
			MSS_I2CA_SCL		10	IO		
W16	PADBH	TRACE_DATA_2	TRACE_DATA_2	0x020C 0084	0	IO	Output Disabled	Pull Down
			RCSS_GPIO_33		1	IO		
			DMM2		2	I		
			MSS_EPWMB_SYNCI		3	I		
			RSVD		4	RSVD		
			RSVD		5	RSVD		
			RSVD		6	RSVD		
			RCSS_MCASPC_FSR		7	IO		
V15	PADBI	TRACE_DATA_3	TRACE_DATA_3	0x020C 0088	0	IO	Output Disabled	Pull Down
			RCSS_GPIO_34		1	IO		
			DMM3		2	I		
			RSVD		3	RSVD		
			MSS_EPWMC_SYNCO		4	O		
			RSVD		5	RSVD		
			RSVD		6	RSVD		
			RCSS_MCASPC_ACLKR		7	I		
W15	PADBJ	TRACE_DATA_4	TRACE_DATA_4	0x020C 008C	0	IO	Output Disabled	Pull Down
			RCSS_GPIO_35		1	IO		
			DMM4		2	I		
			RSVD		3	RSVD		
			MSS_EPWMB_SYNCO		4	O		
			RSVD		5	RSVD		
			RSVD		6	RSVD		
			RCSS_MCASPC_FSX		7	IO		
V14	PADBK	TRACE_DATA_5	TRACE_DATA_5	0x020C 0090	0	IO	Output Disabled	Pull Down
			RCSS_GPIO_36		1	IO		
			DMM5		2	I		
			RSVD		3	RSVD		
			MSS_EPWM_TZ2		4	I		
			MSS_UARTB_TX		5	O		
			RSVD		6	RSVD		
			RCSS_MCASPC_ACLKX		7	IO		
U13	PADBL	TRACE_DATA_6	TRACE_DATA_6	0x020C 0094	0	IO	Output Disabled	Pull Down
			RCSS_GPIO_37		1	IO		
			DMM6		2	I		
			RSVD		3	RSVD		
			MSS_EPWM_TZ1		4	I		
			RSVD		5	RSVD		
			RSVD		6	RSVD		
			RCSS_MCASPC_AHCLKX		7	O		
W14	PADBM	TRACE_DATA_7	TRACE_DATA_7	0x020C 0098	0	IO	Output Disabled	Pull Down
			RCSS_GPIO_38		1	IO		
			DMM7		2	I		
			RSVD		3	RSVD		
			MSS_EPWM_TZ0		4	I		
			DSS_UARTA_TX		5	O		
			RSVD		6	RSVD		
			RCSS_MCASPB_ACLKX		7	IO		

Table 6-1. Pin Attributes (ZCE285A Package) (continued)

BALL NUMBER[1]	PAD NAME[2]	BALL NAME[3]	SIGNAL NAME[4] [10]	PINCNTL ADDRESS[5]	MUX MODE[6] [10]	TYPE[7]	BALL RESET STATE[8]	PULL TYPE[9]
V13	PADBN	TRACE_DATA_8	TRACE_DATA_8	0x020C 009C	0	IO	Output Disabled	Pull Down
			RCSS_GPIO_39		1	IO		
			DMM8		2	I		
			RSVD		3	RSVD		
			MSS_MCANA_TX		4	O		
			MSS_EPWMA_SYNCI		5	I		
			RSVD		6	RSVD		
			RCSS_MCASPB_FSX		7	IO		
W13	PADBO	TRACE_DATA_9	TRACE_DATA_9	0x020C 00A0	0	IO	Output Disabled	Pull Down
			RCSS_GPIO_40		1	IO		
			DMM9		2	I		
			RSVD		3	RSVD		
			MSS_MCANA_RX		4	I		
			MSS_EPWMA_SYNCO		5	O		
			RSVD		6	RSVD		
			RCSS_MCASPB_ACLKR		7	I		
U11	PADBP	TRACE_DATA_10	TRACE_DATA_10	0x020C 00A4	0	IO	Output Disabled	Pull Down
			RCSS_GPIO_41		1	IO		
			DMM10		2	I		
			RSVD		3	RSVD		
			MSS_EPWMC0		4	O		
			RSVD		5	RSVD		
			RSVD		6	RSVD		
			RCSS_MCASPB_FSR		7	IO		
V11	PADBQ	TRACE_DATA_11	TRACE_DATA_11	0x020C 00A8	0	IO	Output Disabled	Pull Down
			RCSS_GPIO_42		1	IO		
			DMM11		2	I		
			RSVD		3	RSVD		
			MSS_EPWMC1		4	O		
			RSVD		5	RSVD		
			RSVD		6	RSVD		
			RCSS_MCASPB_DAT0		7	IO		
W11	PADBR	TRACE_DATA_12	TRACE_DATA_12	0x020C 00AC	0	IO	Output Disabled	Pull Down
			RCSS_GPIO_43		1	IO		
			DMM12		2	I		
			RSVD		3	RSVD		
			MSS_EPWMA0		4	O		
			MSS_MCANB_TX		5	O		
			RSVD		6	RSVD		
			RCSS_MCASPB_DAT1		7	IO		
V10	PADBS	TRACE_DATA_13	TRACE_DATA_13	0x020C 00B0	0	IO	Output Disabled	Pull Down
			RCSS_GPIO_44		1	IO		
			DMM13		2	I		
			RSVD		3	RSVD		
			MSS_EPWMA1		4	O		
			MSS_MCANB_RX		5	I		
			RSVD		6	RSVD		
			RCSS_MCASPB_DAT2		7	IO		
W10	PADBT	TRACE_DATA_14	TRACE_DATA_14	0x020C 00B4	0	IO	Output Disabled	Pull Down
			RCSS_GPIO_45		1	IO		
			DMM14		2	I		
			RSVD		3	RSVD		
			MSS_EPWMB0		4	O		
			RSVD		5	RSVD		

Table 6-1. Pin Attributes (ZCE285A Package) (continued)

BALL NUMBER[1]	PAD NAME[2]	BALL NAME[3]	SIGNAL NAME[4] [10]	PINCNTL ADDRESS[5]	MUX MODE[6] [10]	TYPE[7]	BALL RESET STATE[8]	PULL TYPE[9]
			RSVD		6	RSVD		
			RCSS_MCASPB_DAT3		7	IO		
T10	PADBU	TRACE_DATA_15	TRACE_DATA_15	0x020C 00B8	0	IO	Output Disabled	Pull Down
			RCSS_GPIO_46		1	IO		
			DMM15		2	I		
			RSVD		3	RSVD		
			MSS_EPWMB1		4	O		
			RSVD		5	RSVD		
			RSVD		6	RSVD		
			RCSS_MCASPB_DAT4		7	IO		
			RSVD		8	RSVD		
			RSVD		9	RSVD		
			RSVD		10	RSVD		
			RCSS_I2CA_SDA		11	IO		
W12	PADBV	TRACE_CLK	TRACE_CLK	0x020C 00BC	0	O	Output Disabled	Pull Down
			RCSS_GPIO_47		1	IO		
			DMM_CLK		2	I		
			HW_SYNC_FE1		3	O		
			HW_SYNC_FE2		4	O		
			RSVD		5	RSVD		
			RSVD		6	RSVD		
			RCSS_MCASPB_DAT5		7	IO		
			RSVD		8	RSVD		
			RSVD		9	RSVD		
			DSS_UARTA_RX		10	I		
			RCSS_I2CA_SCL		11	IO		
V12	PADBW	TRACE_CTL	TRACE_CTL	0x020C 00C0	0	IO	Output Disabled	Pull Down
			RCSS_GPIO_48		1	IO		
			DMM_SYNC		2	I		
			HW_SYNC_FE2		3	O		
			HW_SYNC_FE1		4	O		
			RSVD		5	RSVD		
			RSVD		6	RSVD		
			RCSS_MCASPB_AHCLKX		7	O		
			RSVD		8	RSVD		
			RSVD		9	RSVD		
			DSS_UARTA_TX		10	O		
E19	PADBX	RCSS_GPIO_49	RCSS_GPIO_49	0x020C 00C4	0	IO	Output Disabled	Pull Down
			MSS_MII_COL		1	I		
			MSS_RMII_REFCLK		2	I		
			RSVD		3	RSVD		
			RCSS_MCASPA_DAT3		4	IO		
			RSVD		5	RSVD		
			MSS_EPWMA1		6	O		
F16	PADBY	MSS_I2CA_SDA	RCSS_GPIO_50	0x020C 00C8	0	IO	Output Disabled	Pull Down
			MSS_MII_CRS		1	I		
			MSS_RMII_CRS_DV		2	I		
			MSS_I2CA_SDA		3	IO		
			RCSS_MCASPA_DAT2		4	IO		
			RSVD		5	RSVD		
			MSS_EPWMB1		6	O		
F18	PADBZ	MSS_I2CA_SCL	RCSS_GPIO_51	0x020C 00CC	0	IO	Output Disabled	Pull Down
			MSS_MII_RXER		1	I		
			MSS_RMII_RXER		2	I		

Table 6-1. Pin Attributes (ZCE285A Package) (continued)

BALL NUMBER[1]	PAD NAME[2]	BALL NAME[3]	SIGNAL NAME[4] [10]	PINCNTL ADDRESS[5]	MUX MODE[6] [10]	TYPE[7]	BALL RESET STATE[8]	PULL TYPE[9]
			MSS_I2CA_SCL		3	IO		
			RCSS_MCASPA_DAT1		4	IO		
			RSVD		5	RSVD		
			MSS_EPWMC1		6	O		
J18	PADCA	MSS_RGMII_TCTL	RCSS_GPIO_52	0x020C 00D0	0	IO	Output Disabled	Pull Down
			MSS_MII_TXEN		1	O		
			MSS_RMII_TXEN		2	O		
			MSS_RGMII_TCTL		3	O		
			RCSS_MCASPA_DAT0		4	IO		
			RSVD		5	RSVD		
			MSS_EPWMA0		6	O		
J17	PADCB	MSS_RGMII_RCTL	RCSS_GPIO_53	0x020C 00D4	0	IO	Output Disabled	Pull Down
			MSS_MII_RXDV		1	I		
			RSVD		2	RSVD		
			MSS_RGMII_RCTL		3	O		
			RCSS_MCASPA_FSR		4	IO		
			MSS_UARTB_RX		5	I		
			MSS_EPWMB0		6	O		
K18	PADCC	MSS_RGMII_TD3	RCSS_GPIO_54	0x020C 00D8	0	IO	Output Disabled	Pull Down
			MSS_MII_TXD3		1	O		
			RSVD		2	RSVD		
			MSS_RGMII_TD3		3	O		
			RCSS_MCASPA_ACLKR		4	I		
			MSS_UARTB_TX		5	O		
			MSS_EPWMC0		6	O		
K16	PADCD	MSS_RGMII_TD2	RCSS_GPIO_55	0x020C 00DC	0	IO	Output Disabled	Pull Down
			MSS_MII_TXD2		1	O		
			RSVD		2	RSVD		
			MSS_RGMII_TD2		3	O		
			RCSS_MCASPA_FSX		4	IO		
L17	PADCE	MSS_RGMII_TD1	RCSS_GPIO_56	0x020C 00E0	0	IO	Output Disabled	Pull Down
			MSS_MII_TXD1		1	O		
			MSS_RMII_TXD1		2	O		
			MSS_RGMII_TD1		3	O		
			RCSS_MCASPA_ACLKX		4	IO		
L18	PADCF	MSS_RGMII_TD0	RCSS_GPIO_57	0x020C 00E4	0	IO	Output Disabled	Pull Down
			MSS_MII_TXD0		1	O		
			MSS_RMII_TXD0		2	O		
			MSS_RGMII_TD0		3	O		
			RCSS_MCASPA_AHCLKX		4	O		
K19	PADCG	MSS_RGMII_TCLK	RCSS_GPIO_58	0x020C 00E8	0	IO	Output Disabled	Pull Down
			MSS_MII_TXCLK		1	O		
			RSVD		2	RSVD		
			MSS_RGMII_TCLK		3	O		
			RCSS_MCASPB_AHCLKX		4	O		
			RCSS_I2CA_SDA		5	IO		
M19	PADCH	MSS_RGMII_RCLK	RCSS_GPIO_59	0x020C 00EC	0	IO	Output Disabled	Pull Down
			MSS_MII_RXCLK		1	I		
			RSVD		2	RSVD		
			MSS_RGMII_RCLK		3	I		
			RCSS_MCASPB_AHCLKR		4	I		
			RCSS_I2CA_SCL		5	IO		
L19	PADCI	MSS_RGMII_RD3	RCSS_GPIO_60	0x020C 00F0	0	IO	Output Disabled	Pull Down
			MSS_MII_RXD3		1	I		

Table 6-1. Pin Attributes (ZCE285A Package) (continued)

BALL NUMBER[1]	PAD NAME[2]	BALL NAME[3]	SIGNAL NAME[4] [10]	PINCNTL ADDRESS[5]	MUX MODE[6] [10]	TYPE[7]	BALL RESET STATE[8]	PULL TYPE[9]
			RSVD		2	RSVD		
			MSS_RGMII_RD3		3	I		
			RCSS_MCASPB_ACLKX		4	IO		
			RCSS_I2CB_SDA		5	IO		
M18	PADCJ	MSS_RGMII_RD2	RCSS_GPIO_61	0x020C 00F4	0	IO	Output Disabled	Pull Down
			MSS_MII_RXD2		1	I		
			RSVD		2	RSVD		
			MSS_RGMII_RD2		3	I		
			RCSS_MCASPB_FSX		4	IO		
			RCSS_I2CB_SCL		5	IO		
N19	PADCK	MSS_RGMII_RD1	RCSS_GPIO_62	0x020C 00F8	0	IO	Output Disabled	Pull Down
			MSS_MII_RXD1		1	I		
			MSS_RMII_RXD1		2	I		
			MSS_RGMII_RD1		3	I		
			RCSS_MCASPB_ACLKR		4	I		
P18	PADCL	MSS_RGMII_RD0	RCSS_GPIO_63	0x020C 00FC	0	IO	Output Disabled	Pull Down
			MSS_MII_RXD0		1	I		
			MSS_RMII_RXD0		2	I		
			MSS_RGMII_RD0		3	I		
			RCSS_MCASPB_FSR		4	IO		
P19	PADCM	MSS_MDIO_DATA	MSS_GPIO_30	0x020C 0100	0	IO	Output Disabled	Pull Up
			MSS_MDIO_DATA		1	IO		
			RSVD		2	RSVD		
			RSVD		3	RSVD		
			RCSS_MCASPB_DAT0		4	IO		
R19	PADCN	MSS_MDIO_CLK	MSS_GPIO_31	0x020C 0104	0	IO	Output Disabled	Pull Up
			MSS_MDIO_CLK		1	IO		
			RSVD		2	RSVD		
			RSVD		3	RSVD		
			RCSS_MCASPB_DAT1		4	IO		
R18	PADCO	RCSS_MIBSPIA_MOSI	RCSS_GPIO_32	0x020C 0108	0	IO	Output Disabled	Pull Up
			RCSS_MIBSPIA_MOSI		1	O		
			RCSS_I2CA_SDA		2	IO		
			RSVD		3	RSVD		
			RSVD		4	RSVD		
			MSS_MIBSPIA_MOSI		5	O		
R17	PADCP	RCSS_MIBSPIA_MISO	RCSS_GPIO_33	0x020C 010C	0	IO	Output Disabled	Pull Up
			RCSS_MIBSPIA_MISO		1	I		
			RCSS_I2CA_SCL		2	IO		
			RSVD		3	RSVD		
			RSVD		4	RSVD		
			MSS_MIBSPIA_MISO		5	I		
T18	PADCQ	RCSS_MIBSPIA_CLK	RCSS_GPIO_34	0x020C 0110	0	IO	Output Disabled	Pull Up
			RCSS_MIBSPIA_CLK		1	IO		
			RCSS_I2CB_SDA		2	IO		
			RSVD		3	RSVD		
			RSVD		4	RSVD		
			MSS_MIBSPIA_CLK		5	O		
T19	PADCR	RCSS_MIBSPIA_CS0	RCSS_GPIO_35	0x020C 0114	0	IO	Output Disabled	Pull Up
			RCSS_MIBSPIA_CS0		1	IO		
			RCSS_I2CB_SCL		2	IO		
			RSVD		3	RSVD		
			RSVD		4	RSVD		
			MSS_MIBSPIA_CS0		5	O		

Table 6-1. Pin Attributes (ZCE285A Package) (continued)

BALL NUMBER[1]	PAD NAME[2]	BALL NAME[3]	SIGNAL NAME[4] [10]	PINCNTL ADDRESS[5]	MUX MODE[6] [10]	TYPE[7]	BALL RESET STATE[8]	PULL TYPE[9]
U18	PADCS	RCSS_MIBSPIA_HOSTIRQ	RCSS_GPIO_36	0x020C 0118	0	IO	Output Disabled	Pull Down
			RCSS_MIBSPIA_CS1		1	O		
			MSS_GPIO_2		2	IO		
			MSS_GPIO_8		3	IO		
			RSVD		4	RSVD		
			MSS_MIBSPIA_HOSTIRQ		5	I		
			MSS_MIBSPIB_CS2		6	O		
			RCSS_GPIO_34		7	IO		
			RSVD		8	RSVD		
			RSVD		9	RSVD		
			RCSS_GPIO_40		10	IO		
U19	PADCT	RCSS_MIBSPIB_MOSI	RCSS_GPIO_37	0x020C 011C	0	IO	Output Disabled	Pull Up
			RCSS_MIBSPIB_MOSI		1	O		
			RCSS_I2CA_SDA		2	IO		
			MSS_CPTS0_HW1TSPUSH		3	I		
			RSVD		4	RSVD		
			MSS_MIBSPIB_MOSI		5	O		
V18	PADCU	RCSS_MIBSPIB_MISO	RCSS_GPIO_38	0x020C 0120	0	IO	Output Disabled	Pull Up
			RCSS_MIBSPIB_MISO		1	I		
			RCSS_I2CA_SCL		2	IO		
			MSS_CPTS0_HW2TSPUSH		3	I		
			RSVD		4	RSVD		
			MSS_MIBSPIB_MISO		5	I		
V19	PADCV	RCSS_MIBSPIB_CLK	RCSS_GPIO_39	0x020C 0124	0	IO	Output Disabled	Pull Up
			RCSS_MIBSPIB_CLK		1	O		
			RCSS_I2CB_SDA		2	IO		
			MSS_CPTS0_TS_SYNC		3	O		
			RSVD		4	RSVD		
			MSS_MIBSPIB_CLK		5	O		
U17	PADCW	RCSS_MIBSPIB_CS0	RCSS_GPIO_40	0x020C 0128	0	IO	Output Disabled	Pull Up
			RCSS_MIBSPIB_CS0		1	O		
			RCSS_I2CB_SCL		2	O		
			MSS_CPTS0_TS_COMP		3	O		
			RCSS_MCASPC_DAT5		4	IO		
			MSS_MIBSPIB_CS0		5	O		
W18	PADCX	RCSS_MIBSPIB_HOSTIRQ	RCSS_GPIO_41	0x020C 012C	0	IO	Output Disabled	Pull Down
			RCSS_MIBSPIB_CS1		1	O		
			RSVD		2	RSVD		
			MSS_CPTS0_TS_GENF		3	O		
			RCSS_MCASPC_DAT4		4	IO		
			MSS_MIBSPIB_CS1		5	O		
			MSS_GPIO_3		6	IO		
			MSS_GPIO_9		7	IO		
			RSVD		8	RSVD		
			RSVD		9	RSVD		
			RCSS_GPIO_35		10	IO		
V17	PADCY	HW_SYNC_FE1	RCSS_GPIO_43	0x020C 0130	0	IO	Output Disabled	Pull Down
			MSS_CPTS0_TS_COMP		1	O		
			HW_SYNC_FE1		2	O		
			HW_SYNC_FE2		3	O		
			RCSS_MCASPC_DAT2		4	IO		
W17	PADCZ	HW_SYNC_FE2	RCSS_GPIO_43	0x020C 0134	0	IO	Output Disabled	Pull Down
			MSS_CPTS0_TS_COMP		1	O		
			HW_SYNC_FE1		2	O		

Table 6-1. Pin Attributes (ZCE285A Package) (continued)

BALL NUMBER[1]	PAD NAME[2]	BALL NAME[3]	SIGNAL NAME[4] [10]	PINCNTL ADDRESS[5]	MUX MODE[6] [10]	TYPE[7]	BALL RESET STATE[8]	PULL TYPE[9]
			HW_SYNC_FE2		3	O		
			RCSS_MCASPC_DAT2		4	IO		
U3	PADDA	MSS_UARTA_RX	RCSS_GPIO_44	0x020C 0138	0	IO	Output Disabled	Pull Up
			MSS_CPTS0_TS_SYNC		1	O		
			RSVD		2	RSVD		
			RSVD		4	RSVD		
			MSS_UARTB_TX		5	O		
			MSS_UARTA_RX		6	I		
			DSS_UARTA_TX		7	O		
W2	PADDB	MSS_UARTA_TX	RCSS_GPIO_45	0x020C 013C	0	IO	Output Disabled	Pull Up
			MSS_CPTS0_HW2TSPUSH		1			
			RSVD		2	RSVD		
			RSVD		3	RSVD		
			MSS_UARTB_RX		4	I		
			MSS_UARTA_TX		5	O		
			DSS_UARTA_RX		6	I		
J19	PADDC	DSS_UARTA_TX	RCSS_GPIO_46	0x020C 0140	0	IO	Output Disabled	Pull Up
			MSS_CPTS0_HW1TSPUSH		1	I		
			RSVD		2	RSVD		
			RSVD		3	RSVD		
			DSS_UARTA_TX		4	IO		
			RCSS_UARTA_RX		5	I		
			MSS_UARTA_RX		6	I		
H19	PADDD	DSS_UARTA_RX	RCSS_GPIO_47	0x020C 0144	0	IO	Output Disabled	Pull Up
			DSS_UARTA_RX		1	IO		
			RSVD		2	RSVD		
			RSVD		4	RSVD		
			RSVD		5	RSVD		
			RCSS_UARTA_TX		6	O		
			MSS_UARTA_TX		7	O		
V9	PADDE	MSS_UARTB_TX	MSS_GPIO_0	0x020C 0148	0	IO	Output Disabled	Pull Up
			DSS_UARTA_TX		1	O		
			RSVD		2	RSVD		
			MSS_EPWMB_SYNCI		3	I		
			FE1_REFCLK		4	I		
			MSS_UARTA_TX		5	O		
			MSS_UARTB_TX		6	O		
			RSVD		7	RSVD		
			RSVD		8	RSVD		
			RSVD		9	RSVD		
			RSVD		10	RSVD		
			RSVD		11	RSVD		
			RCSS_GPIO_32		12	IO		
J1	PADDF	XREF_CLK0	MSS_GPIO_1	0x020C 014C	0	IO	Output Disabled	Pull Down
			XREF_CLK0		1	I		
			RSVD		2	RSVD		
			RSVD		3	RSVD		
			FE2_REFCLK		4	I		
			RSVD		5	RSVD		
			MCU_CLKOUT		6	O		
			RSVD		7	RSVD		
			RSVD		8	RSVD		
			RSVD		9	RSVD		
			RSVD		10	RSVD		

Table 6-1. Pin Attributes (ZCE285A Package) (continued)

BALL NUMBER[1]	PAD NAME[2]	BALL NAME[3]	SIGNAL NAME[4] [10]	PINCNTL ADDRESS[5]	MUX MODE[6] [10]	TYPE[7]	BALL RESET STATE[8]	PULL TYPE[9]
			RSVD		11	RSVD		
			RCSS_GPIO_33		12	IO		
K2	PADDG	XREF_CLK1	MSS_GPIO_2	0x020C 0150	0	IO	Output Disabled	Pull Down
			XREF_CLK1		1	I		
			RSVD		2	RSVD		
			RCSS_ECAPA_CAPIN_PWMO		3	O		
			RSVD		4	RSVD		
			RSVD		5	RSVD		
			RSVD		6	RSVD		
			PMIC_CLKOUT		7	O		
			RSVD		8	RSVD		
			RSVD		9	RSVD		
			RSVD		10	RSVD		
			RSVD		11	RSVD		
			RCSS_GPIO_34		12	IO		
H18	PADDH	MSS_MIBSPIA_MOSI	MSS_GPIO_3	0x020C 0154	0	IO	Output Disabled	Pull Up
			OBS_CLKOUT		1	O		
			RCSS_ATL_CLK0		2	I		
			RSVD		3	RSVD		
			RCSS_I2CB_SDA		4	IO		
			MSS_EPWMA1		5	O		
			RSVD		6	RSVD		
			RSVD		7	RSVD		
			RSVD		8	RSVD		
			RCSS_UARTA_RTS		9	O		
			MSS_MIBSPIA_MOSI		10	O		
			RSVD		11	RSVD		
			RCSS_GPIO_35		12	IO		
G17	PADDI	MSS_MIBSPIA_MISO	MSS_GPIO_4	0x020C 0158	0	IO	Output Disabled	Pull Up
			HW_SYNC_FE1		1	O		
			MSS_CPTS0_TS_GENF		2	O		
			RCSS_ATL_CLK1		3	I		
			RCSS_I2CB_SCL		4	O		
			MSS_EPWMB1		5	O		
			MSS_EPWMB0		6	O		
			HW_SYNC_FE2		7	O		
			OBS_CLKOUT		8	O		
			RCSS_UARTA_CTS		9	I		
			MSS_MIBSPIA_MISO		10	IO		
			RSVD		11	RSVD		
			RCSS_GPIO_36		12	IO		
G19	PADDJ	MSS_MIBSPIA_CLK	MSS_GPIO_5	0x020C 015C	0	IO	Output Disabled	Pull Up
			HW_SYNC_FE2		1	O		
			MSS_CPTS0_TS_COMP		2	O		
			MSS_EPWMB1		3	O		
			RCSS_ECAPA_CAPIN_PWMO		4	O		
			RCSS_I2CA_SDA		5	IO		
			MSS_UARTB_TX		6	O		
			HW_SYNC_FE1		7	O		
			RSVD		8	RSVD		
			RSVD		9	RSVD		
			MSS_MIBSPIA_CLK		10	O		
			RSVD		11	RSVD		
			RCSS_GPIO_37		12	IO		

Table 6-1. Pin Attributes (ZCE285A Package) (continued)

BALL NUMBER[1]	PAD NAME[2]	BALL NAME[3]	SIGNAL NAME[4] [10]	PINCNTL ADDRESS[5]	MUX MODE[6] [10]	TYPE[7]	BALL RESET STATE[8]	PULL TYPE[9]
F19	PADDK	MSS_MIBSPIA_CS0	MSS_GPIO_6	0x020C 0160	0	IO	Output Disabled	Pull Up
			MSS_EPWMA_SYNCI		1	I		
			RSVD		2	RSVD		
			HW_SYNC_FE1		3	O		
			MSS_EPWMA0		4	O		
			RCSS_I2CA_SCL		5	O		
			MSS_UARTB_RX		6	I		
			MSS_CPTS0_TS_GENF		7	O		
			RSVD		8	RSVD		
			HW_SYNC_FE2		9	O		
			MSS_MIBSPIA_CS0		10	O		
			RSVD		11	RSVD		
			RCSS_GPIO_38		12	IO		
G18	PADDL	MSS_MIBSPIA_HOSTIRQ	MSS_GPIO_7	0x020C 0164	0	IO	Output Disabled	Pull Down
			MSS_EPWMA_SYNCO		1	O		
			MSS_EPWMC1		2	O		
			HW_SYNC_FE2		3	O		
			MSS_EPWMB0		4	O		
			RCSS_I2CB_SDA		5	IO		
			MSS_UARTA_RX		6	I		
			MSS_CPTS0_TS_COMP		7	O		
			RCSS_ECAPA_SYNCIN		8	I		
			HW_SYNC_FE1		9	O		
			MSS_MIBSPIA_HOSTIRQ		10	I		
			RSVD		11	RSVD		
			RCSS_GPIO_39		12	IO		
B3	PADDM	MSS_GPIO_8	MSS_GPIO_8	0x020C 0168	0	IO	Output Disabled	Pull Down
			FE1_REFCLK		1	I		
			MSS_EPWMA_SYNCO		2	O		
			MSS_EPWMB_SYNCI		3	I		
			MSS_EPWMC0		4	O		
			RCSS_I2CB_SCL		5	O		
			MSS_UARTA_TX		6	O		
			MSS_CPTS0_TS_SYNC		7	O		
			RCSS_ECAPA_SYNCOUT		8	O		
			RSVD		9	RSVD		
			RSVD		10	RSVD		
			RSVD		11	RSVD		
			RCSS_GPIO_40		12	IO		
B19	PADDN	MSS_GPIO_9	MSS_GPIO_9	0x020C 016C	0	IO	Output Disabled	Pull Down
			FE2_REFCLK		1	O		
			RCSS_UARTA_TX		2	O		
			MSS_EPWMB_SYNCO		3	O		
			MSS_EPWMA1		4	O		
			RSVD		5	RSVD		
			DSS_UARTA_TX		6	O		
			MSS_CPTS0_HW2TSPUSH		7	I		
			RCSS_MCASPA_AHCLKX		8	O		
			RSVD		9	RSVD		
			RSVD		10	RSVD		
			RCSS_ATL_CLK0		11	I		
			RCSS_GPIO_41		12	IO		
B18	PADDO	MSS_GPIO_10	MSS_GPIO_10	0x020C 0170	0	IO	Output Disabled	Pull Down
			RSVD		1	RSVD		

Table 6-1. Pin Attributes (ZCE285A Package) (continued)

BALL NUMBER[1]	PAD NAME[2]	BALL NAME[3]	SIGNAL NAME[4] [10]	PINCNTL ADDRESS[5]	MUX MODE[6] [10]	TYPE[7]	BALL RESET STATE[8]	PULL TYPE[9]
			RCSS_UARTA_RX		2	I		
			MSS_EPWMC_SYNCI		3	I		
			MSS_EPWMB1		4	O		
			RSVD		5	RSVD		
			DSS_UARTA_RX		6	I		
			MSS_CPTS0_HW1TSPUSH		7	I		
			RCSS_MCASPA_ACLKX		8	IO		
			RSVD		9	RSVD		
			RSVD		10	RSVD		
			RSVD		11	RSVD		
			RCSS_GPIO_42		12	IO		
C17	PADDP	MSS_GPIO_11	MSS_GPIO_11	0x020C 0174	0	IO	Output Disabled	Pull Down
			RSVD		1	RSVD		
			RCSS_UARTA_RTS		2	O		
			MSS_EPWMC_SYNCO		4	O		
			MSS_EPWMC1		5	O		
			MSS_I2CA_SDA		6	IO		
			MSS_UARTB_TX		7	O		
			RSVD		8	RSVD		
			RCSS_MCASPA_FSX		9	IO		
			RSVD		10	RSVD		
			RSVD		11	RSVD		
			RSVD		12	RSVD		
			RCSS_GPIO_43		13	IO		
A18	PADDQ	MSS_GPIO_12	MSS_GPIO_12	0x020C 0178	0	IO	Output Disabled	Pull Down
			MSS_I2CA_SCL		1	O		
			RCSS_UARTA_CTS		2	I		
			HW_SYNC_FE1		3	O		
			RCSS_ECAPA_CAPIN_PWMO		4	O		
			MSS_CPTS0_TS_GENF		5	O		
			MSS_UARTB_RX		6	I		
			RCSS_ECAPA_CAPIN_PWMO		7	O		
			RCSS_MCASPA_ACLKR		8	I		
			RSVD		9	RSVD		
			RSVD		10	RSVD		
			MSS_RS232_RX		11	I		
			RCSS_GPIO_44		12	IO		
B17	PADDR	MSS_GPIO_13	MSS_GPIO_13	0x020C 017C	0	IO	Output Disabled	Pull Down
			MSS_I2CA_SDA		1	IO		
			MSS_CPTS0_TS_COMP		2	O		
			HW_SYNC_FE2		3	O		
			RCSS_UARTA_TX		4	O		
			MSS_UARTA_TX		5	O		
			MSS_UARTB_TX		6	O		
			DSS_UARTA_TX		7	O		
			RCSS_MCASPA_FSR		8	IO		
			RSVD		9	RSVD		
			RSVD		10	RSVD		
			MSS_RS232_TX		11	O		
			RCSS_GPIO_45		12	IO		
A17	PADDS	RCSS_UARTA_TX	MSS_GPIO_14	0x020C 0180	0	IO	Output Disabled	Pull Up
			RSVD		1	RSVD		
			RCSS_UARTA_TX		2	O		
			RCSS_I2CB_SDA		3	IO		

Table 6-1. Pin Attributes (ZCE285A Package) (continued)

BALL NUMBER[1]	PAD NAME[2]	BALL NAME[3]	SIGNAL NAME[4] [10]	PINCNTL ADDRESS[5]	MUX MODE[6] [10]	TYPE[7]	BALL RESET STATE[8]	PULL TYPE[9]
			RSVD		4	RSVD		
			RSVD		5	RSVD		
			RSVD		6	RSVD		
			RCSS_MCASPA_DAT8		7	IO		
			RCSS_MCASPA_DAT0		8	IO		
			RSVD		9	RSVD		
			RSVD		10	RSVD		
			RSVD		11	RSVD		
			RCSS_GPIO_46		12	IO		
B16	PADDT	RCSS_UARTA_RX	MSS_GPIO_15	0x020C 0184	0	IO	Output Disabled	Pull Up
			RSVD		1	RSVD		
			RCSS_UARTA_RX		2	I		
			RCSS_I2CB_SCL		3	O		
			RSVD		4	RSVD		
			RSVD		5	RSVD		
			RSVD		6	RSVD		
			RCSS_MCASPA_DAT9		7	IO		
			RCSS_MCASPA_DAT1		8	IO		
			RSVD		9	RSVD		
			RSVD		10	RSVD		
			RSVD		11	RSVD		
			RCSS_GPIO_47		12	IO		
C15	PADDU	NERRORIN_FE1	MSS_GPIO_16	0x020C 0188	0	IO	Output Disabled	Pull Down
			RSVD		1	RSVD		
			RSVD		2	RSVD		
			RSVD		3	RSVD		
			RSVD		4	RSVD		
			RSVD		5	RSVD		
			RSVD		6	RSVD		
			RCSS_MCASPA_DAT10		7	IO		
			RCSS_MCASPA_DAT2		8	IO		
			RSVD		9	RSVD		
			RSVD		10	RSVD		
			RSVD		11	RSVD		
			RCSS_GPIO_48		12	IO		
A16	PADDV	NERRORIN_FE2	MSS_GPIO_17	0x020C 018C	0	IO	Output Disabled	Pull Down
			RSVD		1	RSVD		
			RSVD		2	RSVD		
			RSVD		3	RSVD		
			RSVD		4	RSVD		
			RSVD		5	RSVD		
			RSVD		6	RSVD		
			RCSS_MCASPA_DAT11		7	IO		
			RCSS_MCASPA_DAT3		8	IO		
			RSVD		9	RSVD		
			RSVD		10	RSVD		
			RSVD		11	RSVD		
			RCSS_GPIO_49		12	IO		
B15	PADDW	NRESET_FE1	MSS_GPIO_18	0x020C 0190	0	IO	Output Disabled	Pull Down
			RSVD		1	RSVD		
			RSVD		2	RSVD		
			RSVD		3	RSVD		
			RSVD		4	RSVD		
			RSVD		5	RSVD		

Table 6-1. Pin Attributes (ZCE285A Package) (continued)

BALL NUMBER[1]	PAD NAME[2]	BALL NAME[3]	SIGNAL NAME[4] [10]	PINCNTL ADDRESS[5]	MUX MODE[6] [10]	TYPE[7]	BALL RESET STATE[8]	PULL TYPE[9]
			RSVD		6	RSVD		
			RCSS_MCASPA_DAT12		7	IO		
			RCSS_MCASPA_DAT4		8	IO		
			RSVD		9	RSVD		
			RSVD		10	RSVD		
			RSVD		11	RSVD		
			RCSS_GPIO_50		12	IO		
A15	PADDX	NRESET_FE2	MSS_GPIO_19	0x020C 0194	0	IO	Output Disabled	Pull Down
			RSVD		1	RSVD		
			RSVD		2	RSVD		
			RCSS_I2CA_SDA		3	IO		
			RSVD		4	RSVD		
			RSVD		5	RSVD		
			RSVD		6	RSVD		
			RCSS_MCASPA_DAT13		7	IO		
			RCSS_MCASPA_DAT5		8	IO		
			RSVD		9	RSVD		
			RSVD		10	RSVD		
			RSVD		11	RSVD		
			RCSS_GPIO_51		12	IO		
B14	PADDY	NWARMRESET_IN_FE1	MSS_GPIO_20	0x020C 0198	0	IO	Output Disabled	Pull Down
			RSVD		1	RSVD		
			RSVD		2	RSVD		
			RCSS_I2CA_SCL		3	IO		
			RSVD		4	RSVD		
			RSVD		5	RSVD		
			RSVD		6	RSVD		
			RCSS_MCASPA_DAT14		7	IO		
			RCSS_MCASPA_DAT6		8	IO		
			RSVD		9	RSVD		
			RSVD		10	RSVD		
			RSVD		11	RSVD		
			RCSS_GPIO_52		12	IO		
C13	PADDZ	NWARMRESET_IN_FE2	MSS_GPIO_21	0x020C 019C	0	IO	Output Disabled	Pull Down
			RSVD		1	RSVD		
			RSVD		2	RSVD		
			RSVD		3	RSVD		
			RCSS_ECAPA_CAPIN_PWMO		4	O		
			RSVD		5	RSVD		
			RSVD		6	RSVD		
			RCSS_MCASPA_DAT15		7	IO		
			RCSS_MCASPA_DAT7		8	IO		
			RSVD		9	RSVD		
			RSVD		10	RSVD		
			RSVD		11	RSVD		
			RCSS_GPIO_53		12	IO		

The MSS_IOMUX registers contol the individual pin states and MUX mapping described in Table 6-1. The following Table 6-2 provides a reference for these registers and power on reset values. For more information on programming the MSS_IOMUX registers, see the device-specific TRM.

Table 6-2. PAD IO Configuration Registers (MSS_IOMUX)

Register Name	Type	Register Width (Bits)	Register Reset	Address Offset	Physical Address
PADAA_CFG_REG	RW	32	0x0000 00C1	0x0000 0000	0x020C 0000
PADAB_CFG_REG	RW	32	0x0000 00C1	0x0000 0004	0x020C 0004
PADAC_CFG_REG	RW	32	0x0000 00C1	0x0000 0008	0x020C 0008
PADAD_CFG_REG	RW	32	0x0000 02C1	0x0000 000C	0x020C 000C
PADAE_CFG_REG	RW	32	0x0000 02C1	0x0000 0010	0x020C 0010
PADAF_CFG_REG	RW	32	0x0000 02C1	0x0000 0014	0x020C 0014
PADAG_CFG_REG	RW	32	0x0000 02C1	0x0000 0018	0x020C 0018
PADAH_CFG_REG	RW	32	0x0000 02C1	0x0000 001C	0x020C 001C
PADAI_CFG_REG	RW	32	0x0000 02C1	0x0000 0020	0x020C 0020
PADAJ_CFG_REG	RW	32	0x0000 02C1	0x0000 0024	0x020C 0024
PADAK_CFG_REG	RW	32	0x0000 02C1	0x0000 0028	0x020C 0028
PADAL_CFG_REG	RW	32	0x0000 00C1	0x0000 002C	0x020C 002C
PADAM_CFG_REG	RW	32	0x0000 00C1	0x0000 0030	0x020C 0030
PADAN_CFG_REG	RW	32	0x0000 02C1	0x0000 0034	0x020C 0034
PADAO_CFG_REG	RW	32	0x0000 02C1	0x0000 0038	0x020C 0038
PADAP_CFG_REG	RW	32	0x0000 00C1	0x0000 003C	0x020C 003C
PADAQ_CFG_REG	RW	32	0x0000 02C1	0x0000 0040	0x020C 0040
PADAR_CFG_REG	RW	32	0x0000 0100	0x0000 0044	0x020C 0044
PADAS_CFG_REG	RW	32	0x0000 0100	0x0000 0048	0x020C 0048
PADAT_CFG_REG	RW	32	0x0000 0100	0x0000 004C	0x020C 004C
PADAU_CFG_REG	RW	32	0x0000 00C1	0x0000 0050	0x020C 0050
PADAV_CFG_REG	RW	32	0x0000 02C1	0x0000 0054	0x020C 0054
PADAW_CFG_REG	RW	32	0x0000 02C1	0x0000 0058	0x020C 0058
PADAX_CFG_REG	RW	32	0x0000 0101	0x0000 005C	0x020C 005C
PADAY_CFG_REG	RW	32	0x0000 00C1	0x0000 0060	0x020C 0060
PADAZ_CFG_REG	RW	32	0x0000 00C1	0x0000 0064	0x020C 0064
PADBA_CFG_REG	RW	32	0x0000 00C1	0x0000 0068	0x020C 0068
PADBB_CFG_REG	RW	32	0x0000 00C1	0x0000 006C	0x020C 006C
PADBC_CFG_REG	RW	32	0x0000 00C1	0x0000 0070	0x020C 0070
PADBD_CFG_REG	RW	32	0x0000 02C1	0x0000 0074	0x020C 0074
PADBE_CFG_REG	RW	32	0x0000 0301	0x0000 0078	0x020C 0078
PADBF_CFG_REG	RW	32	0x0000 00C1	0x0000 007C	0x020C 007C
PADBG_CFG_REG	RW	32	0x0000 00C1	0x0000 0080	0x020C 0080
PADBH_CFG_REG	RW	32	0x0000 00C1	0x0000 0084	0x020C 0084
PADBI_CFG_REG	RW	32	0x0000 00C1	0x0000 0088	0x020C 0088
PADBJ_CFG_REG	RW	32	0x0000 00C1	0x0000 008C	0x020C 008C
PADBK_CFG_REG	RW	32	0x0000 00C1	0x0000 0090	0x020C 0090
PADBL_CFG_REG	RW	32	0x0000 00C1	0x0000 0094	0x020C 0094
PADBM_CFG_REG	RW	32	0x0000 00C1	0x0000 0098	0x020C 0098
PADBN_CFG_REG	RW	32	0x0000 00C1	0x0000 009C	0x020C 009C
PADBO_CFG_REG	RW	32	0x0000 00C1	0x0000 00A0	0x020C 00A0
PADBP_CFG_REG	RW	32	0x0000 00C1	0x0000 00A4	0x020C 00A4
PADBQ_CFG_REG	RW	32	0x0000 00C1	0x0000 00A8	0x020C 00A8
PADBR_CFG_REG	RW	32	0x0000 00C1	0x0000 00AC	0x020C 00AC
PADBS_CFG_REG	RW	32	0x0000 00C1	0x0000 00B0	0x020C 00B0

Table 6-2. PAD IO Configuration Registers (MSS_IOMUX) (continued)

Register Name	Type	Register Width (Bits)	Register Reset	Address Offset	Physical Address
PADBT_CFG_REG	RW	32	0x0000 00C1	0x0000 00B4	0x020C 00B4
PADBU_CFG_REG	RW	32	0x0000 00C1	0x0000 00B8	0x020C 00B8
PADBV_CFG_REG	RW	32	0x0000 00C1	0x0000 00BC	0x020C 00BC
PADBW_CFG_REG	RW	32	0x0000 00C1	0x0000 00C0	0x020C 00C0
PADBX_CFG_REG	RW	32	0x0000 00C1	0x0000 00C4	0x020C 00C4
PADBY_CFG_REG	RW	32	0x0000 00C1	0x0000 00C8	0x020C 00C8
PADBZ_CFG_REG	RW	32	0x0000 00C1	0x0000 00CC	0x020C 00CC
PADCA_CFG_REG	RW	32	0x0000 00C1	0x0000 00D0	0x020C 00D0
PADCB_CFG_REG	RW	32	0x0000 00C1	0x0000 00D4	0x020C 00D4
PADCC_CFG_REG	RW	32	0x0000 00C1	0x0000 00D8	0x020C 00D8
PADCD_CFG_REG	RW	32	0x0000 00C1	0x0000 00DC	0x020C 00DC
PADCE_CFG_REG	RW	32	0x0000 00C1	0x0000 00E0	0x020C 00E0
PADCF_CFG_REG	RW	32	0x0000 00C1	0x0000 00E4	0x020C 00E4
PADCG_CFG_REG	RW	32	0x0000 00C1	0x0000 00E8	0x020C 00E8
PADCH_CFG_REG	RW	32	0x0000 00C1	0x0000 00EC	0x020C 00EC
PADCI_CFG_REG	RW	32	0x0000 00C1	0x0000 00F0	0x020C 00F0
PADCJ_CFG_REG	RW	32	0x0000 00C1	0x0000 00F4	0x020C 00F4
PADCK_CFG_REG	RW	32	0x0000 00C1	0x0000 00F8	0x020C 00F8
PADCL_CFG_REG	RW	32	0x0000 00C1	0x0000 00FC	0x020C 00FC
PADCM_CFG_REG	RW	32	0x0000 02C1	0x0000 0100	0x020C 0100
PADCN_CFG_REG	RW	32	0x0000 02C1	0x0000 0104	0x020C 0104
PADCO_CFG_REG	RW	32	0x0000 02C1	0x0000 0108	0x020C 0108
PADCP_CFG_REG	RW	32	0x0000 02C1	0x0000 010C	0x020C 010C
PADCQ_CFG_REG	RW	32	0x0000 02C1	0x0000 0110	0x020C 0110
PADCR_CFG_REG	RW	32	0x0000 02C1	0x0000 0114	0x020C 0114
PADCS_CFG_REG	RW	32	0x0000 00C1	0x0000 0118	0x020C 0118
PADCT_CFG_REG	RW	32	0x0000 02C1	0x0000 011C	0x020C 011C
PADCU_CFG_REG	RW	32	0x0000 02C1	0x0000 0120	0x020C 0120
PADCV_CFG_REG	RW	32	0x0000 02C1	0x0000 0124	0x020C 0124
PADCW_CFG_REG	RW	32	0x0000 02C1	0x0000 0128	0x020C 0128
PADCX_CFG_REG	RW	32	0x0000 00C1	0x0000 012C	0x020C 012C
PADCY_CFG_REG	RW	32	0x0000 00C1	0x0000 0130	0x020C 0130
PADCZ_CFG_REG	RW	32	0x0000 00C1	0x0000 0134	0x020C 0134
PADDA_CFG_REG	RW	32	0x0000 02C1	0x0000 0138	0x020C 0138
PADDB_CFG_REG	RW	32	0x0000 02C1	0x0000 013C	0x020C 013C
PADDC_CFG_REG	RW	32	0x0000 02C1	0x0000 0140	0x020C 0140
PADDD_CFG_REG	RW	32	0x0000 02C1	0x0000 0144	0x020C 0144
PADDE_CFG_REG	RW	32	0x0000 02C1	0x0000 0148	0x020C 0148
PADDF_CFG_REG	RW	32	0x0000 00C1	0x0000 014C	0x020C 014C
PADDG_CFG_REG	RW	32	0x0000 00C1	0x0000 0150	0x020C 0150
PADDH_CFG_REG	RW	32	0x0000 02C1	0x0000 0154	0x020C 0154
PADDI_CFG_REG	RW	32	0x0000 02C1	0x0000 0158	0x020C 0158
PADDJ_CFG_REG	RW	32	0x0000 02C1	0x0000 015C	0x020C 015C
PADDK_CFG_REG	RW	32	0x0000 02C1	0x0000 0160	0x020C 0160
PADDL_CFG_REG	RW	32	0x0000 00C1	0x0000 0164	0x020C 0164

Table 6-2. PAD IO Configuration Registers (MSS_IOMUX) (continued)

Register Name	Type	Register Width (Bits)	Register Reset	Address Offset	Physical Address
PADDM_CFG_REG	RW	32	0x0000 00C1	0x0000 0168	0x020C 0168
PADDN_CFG_REG	RW	32	0x0000 00C1	0x0000 016C	0x020C 016C
PADDO_CFG_REG	RW	32	0x0000 00C1	0x0000 0170	0x020C 0170
PADDP_CFG_REG	RW	32	0x0000 00C1	0x0000 0174	0x020C 0174
PADDQ_CFG_REG	RW	32	0x0000 00C1	0x0000 0178	0x020C 0178
PADDR_CFG_REG	RW	32	0x0000 00C1	0x0000 017C	0x020C 017C
PADDS_CFG_REG	RW	32	0x0000 02C1	0x0000 0180	0x020C 0180
PADDT_CFG_REG	RW	32	0x0000 02C1	0x0000 0184	0x020C 0184
PADDU_CFG_REG	RW	32	0x0000 00C1	0x0000 0188	0x020C 0188
PADDV_CFG_REG	RW	32	0x0000 00C1	0x0000 018C	0x020C 018C
PADDW_CFG_REG	RW	32	0x0000 00C1	0x0000 0190	0x020C 0190
PADDX_CFG_REG	RW	32	0x0000 00C1	0x0000 0194	0x020C 0194
PADDY_CFG_REG	RW	32	0x0000 00C1	0x0000 0198	0x020C 0198
PADDZ_CFG_REG	RW	32	0x0000 00C1	0x0000 019C	0x020C 019C

6.3 Signal Descriptions

Note

All digital IO pins of the device (except NERROR IN, NERROR_OUT, and WARM_RESET) are non-failsafe; hence, care needs to be taken that they are not driven externally without the VIO supply being present to the device

Note

The GPIO state during the power supply ramp is not ensured. In case the GPIO is used in the application where the state of the GPIO is critical, even when NRESET is low, a tri-state buffer should be used to isolate the GPIO output from any attached device. An additional pull resister should be used to define the required state in the application. The NRESET signal could be used to control the output enable (OE) of the tri-state buffer.

Table 6-3. Signal Descriptions

FUNCTION	BALL NUMBER	SIGNAL NAME	TYPE	DEFAULT PULL STATUS	BUFFER TYPE	DESCRIPTION
ADC Interface	R2	ADC1	I	–	ADC Input	ADC Input Channel 1
ADC Interface	P2	ADC2	I	–	ADC Input	ADC Input Channel 2
ADC Interface	R1	ADC3	I	–	ADC Input	ADC Input Channel 3
ADC Interface	P1	ADC4	I	–	ADC Input	ADC Input Channel 4
ADC Interface	M2	ADC5	I	–	ADC Input	ADC Input Channel 5
ADC Interface	T2	ADC6	I	–	ADC Input	ADC Input Channel 6
ADC Interface	N2	ADC7	I	–	ADC Input	ADC Input Channel 7
ADC Interface	N1	ADC8	I	–	ADC Input	ADC Input Channel 8
ADC Interface	M1	ADC9	I	–	ADC Input	ADC Input Channel 9
Clocking	U1	CLKM	I	–	Clock Input	Primary crystal or oscillator input clock negative polarity.
Clocking	V1	CLKP	I	–	Clock Input	Primary crystal or oscillator input clock positive polarity.
Clocking	T4	OSC_CLK_OUT_AUDIO	O	–	Clock Output	Oscillator output reference clock
Clocking	J1	XREF_CLK0	IO	–	LVCMOS	Optional external reference input clock 0. Can be used as dedicated peripheral clock source for system synchronization. See TRM for details.
Clocking	K2	XREF_CLK1	IO	–	LVCMOS	Optional external reference input clock 1. Can be used as dedicated peripheral clock source for system synchronization. See TRM for details.
Clocking	F1	PMIC_CLKOUT	IO	–	LVCMOS	PMIC output reference clock
CSI2.0 Interface	B6	CSI2_RX0CLKM	I	–	MIPI D-PHY	CSI2.0 Receiver #1, Clock Input Negative Polarity
CSI2.0 Interface	A6	CSI2_RX0CLKP	I	–	MIPI D-PHY	CSI2.0 Receiver #1, Clock Input Positive Polarity
CSI2.0 Interface	A8	CSI2_RX0M0	I	–	MIPI D-PHY	CSI2.0 Receiver #1, Negative Polarity Lane 0
CSI2.0 Interface	A7	CSI2_RX0M1	I	–	MIPI D-PHY	CSI2.0 Receiver #1, Negative Polarity Lane 1
CSI2.0 Interface	B5	CSI2_RX0M2	I	–	MIPI D-PHY	CSI2.0 Receiver #1, Negative Polarity Lane 2

Table 6-3. Signal Descriptions (continued)

FUNCTION	BALL NUMBER	SIGNAL NAME	TYPE	DEFAULT PULL STATUS	BUFFER TYPE	DESCRIPTION
CSI2.0 Interface	B4	CSI2_RX0M3	I	–	MIPI D-PHY	CSI2.0 Receiver #1, Negative Polarity Lane 3
CSI2.0 Interface	B8	CSI2_RX0P0	I	–	MIPI D-PHY	CSI2.0 Receiver #1, Positive Polarity Lane 0
CSI2.0 Interface	B7	CSI2_RX0P1	I	–	MIPI D-PHY	CSI2.0 Receiver #1, Positive Polarity Lane 1
CSI2.0 Interface	A5	CSI2_RX0P2	I	–	MIPI D-PHY	CSI2.0 Receiver #1, Positive Polarity Lane 2
CSI2.0 Interface	A4	CSI2_RX0P3	I	–	MIPI D-PHY	CSI2.0 Receiver #1, Positive Polarity Lane 3
CSI2.0 Interface	A11	CSI2_RX1CLKM	I	–	MIPI D-PHY	CSI2.0 Receiver #2, Clock Input Negative Polarity
CSI2.0 Interface	B11	CSI2_RX1CLKP	I	–	MIPI D-PHY	CSI2.0 Receiver #2, Clock Input Positive Polarity
CSI2.0 Interface	A13	CSI2_RX1M0	I	–	MIPI D-PHY	CSI2.0 Receiver #2, Negative Polarity Lane 0
CSI2.0 Interface	B12	CSI2_RX1M1	I	–	MIPI D-PHY	CSI2.0 Receiver #2, Negative Polarity Lane 1
CSI2.0 Interface	A10	CSI2_RX1M2	I	–	MIPI D-PHY	CSI2.0 Receiver #2, Negative Polarity Lane 2
CSI2.0 Interface	A9	CSI2_RX1M3	I	–	MIPI D-PHY	CSI2.0 Receiver #2, Negative Polarity Lane 3
CSI2.0 Interface	B13	CSI2_RX1P0	I	–	MIPI D-PHY	CSI2.0 Receiver #2, Positive Polarity Lane 0
CSI2.0 Interface	A12	CSI2_RX1P1	I	–	MIPI D-PHY	CSI2.0 Receiver #2, Positive Polarity Lane 1
CSI2.0 Interface	B10	CSI2_RX1P2	I	–	MIPI D-PHY	CSI2.0 Receiver #2, Positive Polarity Lane 2
CSI2.0 Interface	B9	CSI2_RX1P3	I	–	MIPI D-PHY	CSI2.0 Receiver #2, Positive Polarity Lane 3
Debug Trace	W12	TRACE_CLK	IO	Pull Down	LVCMOS	ARM/DSP Trace Debug Interface Clock
Debug Trace	V12	TRACE_CTL	IO	Pull Down	LVCMOS	ARM/DSP Trace Debug Interface Control
Debug Trace	V16	TRACE_DATA_0	IO	Pull Down	LVCMOS	ARM/DSP Trace Debug Interface I/O
Debug Trace	U15	TRACE_DATA_1	IO	Pull Down	LVCMOS	ARM/DSP Trace Debug Interface I/O
Debug Trace	U11	TRACE_DATA_10	IO	Pull Down	LVCMOS	ARM/DSP Trace Debug Interface I/O
Debug Trace	V11	TRACE_DATA_11	IO	Pull Down	LVCMOS	ARM/DSP Trace Debug Interface I/O
Debug Trace	W11	TRACE_DATA_12	IO	Pull Down	LVCMOS	ARM/DSP Trace Debug Interface I/O
Debug Trace	V10	TRACE_DATA_13	IO	Pull Down	LVCMOS	ARM/DSP Trace Debug Interface I/O
Debug Trace	W10	TRACE_DATA_14	IO	Pull Down	LVCMOS	ARM/DSP Trace Debug Interface I/O
Debug Trace	T10	TRACE_DATA_15	IO	Pull Down	LVCMOS	ARM/DSP Trace Debug Interface I/O
Debug Trace	W16	TRACE_DATA_2	IO	Pull Down	LVCMOS	ARM/DSP Trace Debug Interface I/O
Debug Trace	V15	TRACE_DATA_3	IO	Pull Down	LVCMOS	ARM/DSP Trace Debug Interface I/O
Debug Trace	W15	TRACE_DATA_4	IO	Pull Down	LVCMOS	ARM/DSP Trace Debug Interface I/O
Debug Trace	V14	TRACE_DATA_5	IO	Pull Down	LVCMOS	ARM/DSP Trace Debug Interface I/O
Debug Trace	U13	TRACE_DATA_6	IO	Pull Down	LVCMOS	ARM/DSP Trace Debug Interface I/O
Debug Trace	W14	TRACE_DATA_7	IO	Pull Down	LVCMOS	ARM/DSP Trace Debug Interface I/O
Debug Trace	V13	TRACE_DATA_8	IO	Pull Down	LVCMOS	ARM/DSP Trace Debug Interface I/O

Table 6-3. Signal Descriptions (continued)

FUNCTION	BALL NUMBER	SIGNAL NAME	TYPE	DEFAULT PULL STATUS	BUFFER TYPE	DESCRIPTION
Debug Trace	W13	TRACE_DATA_9	IO	Pull Down	LVCMOS	ARM/DSP Trace Debug Interface I/O
DSS UART A	H19	DSS_UARTA_RX	IO	Pull Up	LVCMOS	DSS UART A Receiver
DSS UART A	J19	DSS_UARTA_TX	IO	Pull Up	LVCMOS	DSS UART A Receiver
Error Interface	L3	NERROR_IN	I	Pull Disabled	LVCMOS, Open-Drain, Failsafe	Error Interface Input
Error Interface	L1	NERROR_OUT	O	Pull Disabled	LVCMOS, Open-Drain, Failsafe	Error Interface Output
Ground	W1	VSS	–	–	Power	Ground Return
Ground	A1	VSS	–	–	Power	Ground Return
Ground	C7	VSS	–	–	Power	Ground Return
Ground	V2	VSS	–	–	Power	Ground Return
Ground	A3	VSS	–	–	Power	Ground Return
Ground	E5	VSS	–	–	Power	Ground Return
Ground	T6	VSS	–	–	Power	Ground Return
Ground	P6	VSS	–	–	Power	Ground Return
Ground	F6	VSS	–	–	Power	Ground Return
Ground	R7	VSS	–	–	Power	Ground Return
Ground	P7	VSS	–	–	Power	Ground Return
Ground	N7	VSS	–	–	Power	Ground Return
Ground	M7	VSS	–	–	Power	Ground Return
Ground	L7	VSS	–	–	Power	Ground Return
Ground	K7	VSS	–	–	Power	Ground Return
Ground	J7	VSS	–	–	Power	Ground Return
Ground	H7	VSS	–	–	Power	Ground Return
Ground	G7	VSS	–	–	Power	Ground Return
Ground	F7	VSS	–	–	Power	Ground Return
Ground	E7	VSS	–	–	Power	Ground Return
Ground	R8	VSS	–	–	Power	Ground Return
Ground	P8	VSS	–	–	Power	Ground Return
Ground	N8	VSS	–	–	Power	Ground Return
Ground	M8	VSS	–	–	Power	Ground Return
Ground	L8	VSS	–	–	Power	Ground Return
Ground	K8	VSS	–	–	Power	Ground Return
Ground	J8	VSS	–	–	Power	Ground Return
Ground	H8	VSS	–	–	Power	Ground Return
Ground	G8	VSS	–	–	Power	Ground Return
Ground	F8	VSS	–	–	Power	Ground Return
Ground	E8	VSS	–	–	Power	Ground Return
Ground	D8	VSS	–	–	Power	Ground Return
Ground	W9	VSS	–	–	Power	Ground Return
Ground	N9	VSS	–	–	Power	Ground Return
Ground	M9	VSS	–	–	Power	Ground Return
Ground	L9	VSS	–	–	Power	Ground Return

Table 6-3. Signal Descriptions (continued)

FUNCTION	BALL NUMBER	SIGNAL NAME	TYPE	DEFAULT PULL STATUS	BUFFER TYPE	DESCRIPTION
Ground	K9	VSS	–	–	Power	Ground Return
Ground	J9	VSS	–	–	Power	Ground Return
Ground	H9	VSS	–	–	Power	Ground Return
Ground	G9	VSS	–	–	Power	Ground Return
Ground	N10	VSS	–	–	Power	Ground Return
Ground	M10	VSS	–	–	Power	Ground Return
Ground	L10	VSS	–	–	Power	Ground Return
Ground	K10	VSS	–	–	Power	Ground Return
Ground	J10	VSS	–	–	Power	Ground Return
Ground	H10	VSS	–	–	Power	Ground Return
Ground	G10	VSS	–	–	Power	Ground Return
Ground	D10	VSS	–	–	Power	Ground Return
Ground	N11	VSS	–	–	Power	Ground Return
Ground	M11	VSS	–	–	Power	Ground Return
Ground	L11	VSS	–	–	Power	Ground Return
Ground	K11	VSS	–	–	Power	Ground Return
Ground	J11	VSS	–	–	Power	Ground Return
Ground	H11	VSS	–	–	Power	Ground Return
Ground	G11	VSS	–	–	Power	Ground Return
Ground	R12	VSS	–	–	Power	Ground Return
Ground	P12	VSS	–	–	Power	Ground Return
Ground	N12	VSS	–	–	Power	Ground Return
Ground	M12	VSS	–	–	Power	Ground Return
Ground	L12	VSS	–	–	Power	Ground Return
Ground	K12	VSS	–	–	Power	Ground Return
Ground	J12	VSS	–	–	Power	Ground Return
Ground	H12	VSS	–	–	Power	Ground Return
Ground	G12	VSS	–	–	Power	Ground Return
Ground	F12	VSS	–	–	Power	Ground Return
Ground	E12	VSS	–	–	Power	Ground Return
Ground	D12	VSS	–	–	Power	Ground Return
Ground	R13	VSS	–	–	Power	Ground Return
Ground	P13	VSS	–	–	Power	Ground Return
Ground	N13	VSS	–	–	Power	Ground Return
Ground	M13	VSS	–	–	Power	Ground Return
Ground	L13	VSS	–	–	Power	Ground Return
Ground	K13	VSS	–	–	Power	Ground Return
Ground	J13	VSS	–	–	Power	Ground Return
Ground	H13	VSS	–	–	Power	Ground Return
Ground	G13	VSS	–	–	Power	Ground Return
Ground	F13	VSS	–	–	Power	Ground Return
Ground	E13	VSS	–	–	Power	Ground Return
Ground	P14	VSS	–	–	Power	Ground Return
Ground	F14	VSS	–	–	Power	Ground Return

Table 6-3. Signal Descriptions (continued)

FUNCTION	BALL NUMBER	SIGNAL NAME	TYPE	DEFAULT PULL STATUS	BUFFER TYPE	DESCRIPTION
Ground	A14	VSS	–	–	Power	Ground Return
Ground	R15	VSS	–	–	Power	Ground Return
Ground	T16	VSS	–	–	Power	Ground Return
Ground	D16	VSS	–	–	Power	Ground Return
Ground	W19	VSS	–	–	Power	Ground Return
Ground	A19	VSS	–	–	Power	Ground Return
JTAG	C3	TCK	IO	Pull Down	LVCMOS	JTAG Test Clock
JTAG	C5	TDI	IO	Pull Up	LVCMOS	JTAG Test Data Input
JTAG	D6	TDO	IO	Pull Disabled	LVCMOS	JTAG Test Data Output
JTAG	D4	TMS	IO	Pull Up	LVCMOS	JTAG Test Data Mode Select
LVDS Interface	W7	LVDS_CLKM	O	–	LVDS	LVDS/Aurora Transmitter, Clock, Negative Polarity
LVDS Interface	V7	LVDS_CLKP	O	–	LVDS	LVDS/Aurora Transmitter, Clock, Positive Polarity
LVDS Interface	W8	LVDS_FRCLKM	O	–	LVDS	LVDS/Aurora Transmitter, Frame Clock, Negative Polarity
LVDS Interface	V8	LVDS_FRCLKP	O	–	LVDS	LVDS/Aurora Transmitter, Frame Clock, Positive Polarity
LVDS Interface	V6	LVDS_TXM0	O	–	LVDS	LVDS/Aurora Transmitter, Data Output, Negative Polarity, Lane 0
LVDS Interface	V5	LVDS_TXM1	O	–	LVDS	LVDS/Aurora Transmitter, Data Output, Negative Polarity, Lane 1
LVDS Interface	V4	LVDS_TXM2	O	–	LVDS	LVDS/Aurora Transmitter, Data Output, Negative Polarity, Lane 2
LVDS Interface	V3	LVDS_TXM3	O	–	LVDS	LVDS/Aurora Transmitter, Data Output, Negative Polarity, Lane 3
LVDS Interface	W6	LVDS_TXP0	O	–	LVDS	LVDS/Aurora Transmitter, Data Output, Positive Polarity, Lane 0
LVDS Interface	W5	LVDS_TXP1	O	–	LVDS	LVDS/Aurora Transmitter, Data Output, Positive Polarity, Lane 1
LVDS Interface	W4	LVDS_TXP2	O	–	LVDS	LVDS/Aurora Transmitter, Data Output, Positive Polarity, Lane 2
LVDS Interface	W3	LVDS_TXP3	O	–	LVDS	LVDS/Aurora Transmitter, Data Output, Positive Polarity, Lane 3
MSS CAN A	B2	MSS_MCANA_RX	IO	Pull Up	LVCMOS	MSS CAN Channel A, Receiver
MSS CAN A	A2	MSS_MCANA_TX	IO	Pull Up	LVCMOS	MSS CAN Channel A, Transmitter
MSS CAN B	C1	MSS_MCANB_RX	IO	Pull Up	LVCMOS	MSS CAN Channel B, Receiver
MSS CAN B	B1	MSS_MCANB_TX	IO	Pull Up	LVCMOS	MSS CAN Channel B, Transmitter
MSS EPWM	E3	MSS_EPWMA0	IO	Pull Down	LVCMOS	MSS Enhanced PWM A, Channel 0
MSS Ethernet	R19	MSS_MDIO_CLK	IO	Pull Up	LVCMOS	MSS Ethernet Manage Data Input/ Output Clock
MSS Ethernet	P19	MSS_MDIO_DATA	IO	Pull Up	LVCMOS	MSS Ethernet Manage Data Input/ Output Data
MSS Ethernet	M19	MSS_RGMII_RCLK	IO	Pull Down	LVCMOS	MSS Ethernet RGMII/GMII/MII Receive Clock
MSS Ethernet	P18	MSS_RGMII_RD0	IO	Pull Down	LVCMOS	MSS Ethernet RGMII/GMII/MII Receive Data 0
MSS Ethernet	N19	MSS_RGMII_RD1	IO	Pull Down	LVCMOS	MSS Ethernet RGMII/GMII/MII Receive Data 1

Table 6-3. Signal Descriptions (continued)

FUNCTION	BALL NUMBER	SIGNAL NAME	TYPE	DEFAULT PULL STATUS	BUFFER TYPE	DESCRIPTION
MSS Ethernet	M18	MSS_RGMII_RD2	IO	Pull Down	LVCMOS	MSS Ethernet RGMII/GMII/MII Receive Data 2
MSS Ethernet	L19	MSS_RGMII_RD3	IO	Pull Down	LVCMOS	MSS Ethernet RGMII/GMII/MII Receive Data 3
MSS Ethernet	K19	MSS_RGMII_TCLK	IO	Pull Down	LVCMOS	MSS Ethernet RGMII/GMII/MII Transmit Clock
MSS Ethernet	L18	MSS_RGMII_TD0	IO	Pull Down	LVCMOS	MSS Ethernet RGMII/GMII/MII Transmit Data 0
MSS Ethernet	L17	MSS_RGMII_TD1	IO	Pull Down	LVCMOS	MSS Ethernet RGMII/GMII/MII Transmit Data 1
MSS Ethernet	K16	MSS_RGMII_TD2	IO	Pull Down	LVCMOS	MSS Ethernet RGMII/GMII/MII Transmit Data 2
MSS Ethernet	K18	MSS_RGMII_TD3	IO	Pull Down	LVCMOS	MSS Ethernet RGMII/GMII/MII Transmit Data 3
MSS Ethernet	J17	MSS_RGMII_RCTL	IO	Pull Down	LVCMOS	MSS Ethernet RGMII/GMII/MII Transmit Data 3
MSS Ethernet	J18	MSS_RGMII_TCTL	IO	Pull Down	LVCMOS	MSS Ethernet RGMII/GMII/MII Transmit Data 3
MSS GPIO	B18	MSS_GPIO_10	IO	Pull Down	LVCMOS	MSS GPIO
MSS GPIO	C17	MSS_GPIO_11	IO	Pull Down	LVCMOS	MSS GPIO
MSS GPIO	A18	MSS_GPIO_12	IO	Pull Down	LVCMOS	MSS GPIO
MSS GPIO	B17	MSS_GPIO_13	IO	Pull Down	LVCMOS	MSS GPIO
MSS GPIO	H2	MSS_GPIO_2	IO	Pull Down	LVCMOS	MSS GPIO
MSS GPIO	G3	MSS_GPIO_28	IO	Pull Down	LVCMOS	MSS GPIO
MSS GPIO	B3	MSS_GPIO_8	IO	Pull Down	LVCMOS	MSS GPIO
MSS GPIO	B19	MSS_GPIO_9	IO	Pull Down	LVCMOS	MSS GPIO
MSS I2CA	F16	MSS_I2CA_SDA	IO	Pull Down	LVCMOS	12C A, Data
MSS I2CA	F18	MSS_I2CA_SCL	IO	Pull Down	LVCMOS	I2C A, Clock
MSS SPI A	G19	MSS_MIBSPIA_CLK	IO	Pull Up	LVCMOS	MSS SPI A, Clock Output
MSS SPI A	F19	MSS_MIBSPIA_CS0	IO	Pull Up	LVCMOS	MSS SPI A, Chip-Select Output
MSS SPI A	G18	MSS_MIBSPIA_HOSTIRQ	IO	Pull Down	LVCMOS	MSS SPI A ,Host Interrupt Input
MSS SPI A	G17	MSS_MIBSPIA_MISO	IO	Pull Up	LVCMOS	MSS SPI A, Host Master Input, Slave Output
MSS SPI A	H18	MSS_MIBSPIA_MOSI	IO	Pull Up	LVCMOS	MSS SPI A, Host Master Output, Slave Input
MSS SPI B	D18	MSS_MIBSPIB_CLK	IO	Pull Up	LVCMOS	MSS SPI B, Clock Output
MSS SPI B	D19	MSS_MIBSPIB_CS0	IO	Pull Up	LVCMOS	MSS SPI B, Chip-Select 0 Output
MSS SPI B	E18	MSS_MIBSPIB_CS1	IO	Pull Down	LVCMOS	MSS SPI B, Chip-Select 1 Output
MSS SPI B	E17	MSS_MIBSPIB_CS2	IO	Pull Down	LVCMOS	MSS SPI B, Chip-Select 2Output
MSS SPI B	C19	MSS_MIBSPIB_MISO	IO	Pull Up	LVCMOS	MSS SPI B, Host Master Input, Slave Output
MSS SPI B	C18	MSS_MIBSPIB_MOSI	IO	Pull Up	LVCMOS	MSS SPI B, Host Master Output, Slave Input
MSS UART A	U3	MSS_UARTA_RX	IO	Pull Up	LVCMOS	MSS UART A, Receive
MSS UART A	W2	MSS_UARTA_TX	IO	Pull Up	LVCMOS	MSS UART A, Transmit
MSS UART B	V9	MSS_UARTB_TX	IO	Pull Up	LVCMOS	MSS UART B, Transmit
Power, 1.2V Core Digital	N5	VDD	_	–	Power	1.2V Core Digital Power

Table 6-3. Signal Descriptions (continued)

FUNCTION	BALL NUMBER	SIGNAL NAME	TYPE	DEFAULT PULL STATUS	BUFFER TYPE	DESCRIPTION
Power, 1.2V Core Digital	L5	VDD	_	–	Power	1.2V Core Digital Power
Power, 1.2V Core Digital	J5	VDD	_	–	Power	1.2V Core Digital Power
Power, 1.2V Core Digital	G5	VDD	_	–	Power	1.2V Core Digital Power
Power, 1.2V Core Digital	N6	VDD	_	–	Power	1.2V Core Digital Power
Power, 1.2V Core Digital	L6	VDD	_	–	Power	1.2V Core Digital Power
Power, 1.2V Core Digital	J6	VDD	_	–	Power	1.2V Core Digital Power
Power, 1.2V Core Digital	G6	VDD	_	–	Power	1.2V Core Digital Power
Power, 1.2V Core Digital	R9	VDD	_	–	Power	1.2V Core Digital Power
Power, 1.2V Core Digital	P9	VDD	_	–	Power	1.2V Core Digital Power
Power, 1.2V Core Digital	F9	VDD	_	–	Power	1.2V Core Digital Power
Power, 1.2V Core Digital	E9	VDD	_	–	Power	1.2V Core Digital Power
Power, 1.2V Core Digital	R11	VDD	_	–	Power	1.2V Core Digital Power
Power, 1.2V Core Digital	P11	VDD	_	–	Power	1.2V Core Digital Power
Power, 1.2V Core Digital	F11	VDD	_	–	Power	1.2V Core Digital Power
Power, 1.2V Core Digital	E11	VDD	_	–	Power	1.2V Core Digital Power
Power, 1.2V Core Digital	N14	VDD	_	–	Power	1.2V Core Digital Power
Power, 1.2V Core Digital	L14	VDD	_	–	Power	1.2V Core Digital Power
Power, 1.2V Core Digital	J14	VDD	_	–	Power	1.2V Core Digital Power
Power, 1.2V Core Digital	G14	VDD	_	–	Power	1.2V Core Digital Power
Power, 1.2V Core Digital	N15	VDD	_	–	Power	1.2V Core Digital Power
Power, 1.2V Core Digital	L15	VDD	_	–	Power	1.2V Core Digital Power
Power, 1.2V Core Digital	J15	VDD	_	–	Power	1.2V Core Digital Power
Power, 1.2V Core Digital	G15	VDD	_	–	Power	1.2V Core Digital Power
Power, 1.2V Core Digital	N17	VDD_SRAM1	_	–	Power	1.2V SRAM Digital Power
Power, 1.2V Core Digital	J3	VDD_SRAM2	_	–	Power	1.2V SRAM Digital Power
Power, 1.2V Core Digital	T8	VDD_SRAM3	_	–	Power	1.2V SRAM Digital Power

Table 6-3. Signal Descriptions (continued)

FUNCTION	BALL NUMBER	SIGNAL NAME	TYPE	DEFAULT PULL STATUS	BUFFER TYPE	DESCRIPTION
Power, 1.2V Core Digital	N18	VNWA	_	–	Power	1.2V N-well bias
Power, 1.8V ADC	R3	VIOIN_18ADC	_	–	Power	1.8V ADC Power
Power, 1.8V Clocking	U2	VIOIN_18CLK	_	–	Power	1.8V Clock Power
Power, 1.8V I/O	M4	VIOIN_18	–	–	Power	1.8V Digital I/O Power
Power, 1.8V I/O	H4	VIOIN_18	–	–	Power	1.8V Digital I/O Power
Power, 1.8V I/O	T14	VIOIN_18	–	–	Power	1.8V Digital I/O Power
Power, 1.8V I/O	E15	VIOIN_18	–	–	Power	1.8V Digital I/O Power
Power, 1.8V I/O	M16	VIOIN_18	–	–	Power	1.8V Digital I/O Power
Power, 1.8V I/O LVDS	U5	VIOIN_18LVDS	_	–	Power	1.8V LVDS I/O Power
Power, 1.8V I/O LVDS	U7	VIOIN_18LVDS	_	–	Power	1.8V LVDS I/O Power
Power, 1.8V I/O MIPI D-PHY	C9	VIOIN_18CSI	_	–	Power	1.8V CSI2 I/O Power
Power, 1.8V I/O MIPI D-PHY	C11	VIOIN_18CSI	_	–	Power	1.8V CSI2 I/O Power
Power, 1.8V/3.3V I/O	K4	VIOIN	_	–	Power	1.8V/3.3V Digital I/O Power
Power, 1.8V/3.3V I/O	F4	VIOIN	_	–	Power	1.8V/3.3V Digital I/O Power
Power, 1.8V/3.3V I/O	R5	VIOIN	_	–	Power	1.8V/3.3V Digital I/O Power
Power, 1.8V/3.3V I/O	T12	VIOIN	_	–	Power	1.8V/3.3V Digital I/O Power
Power, 1.8V/3.3V I/O	D14	VIOIN	_	–	Power	1.8V/3.3V Digital I/O Power
Power, 1.8V/3.3V I/O	P16	VIOIN	_	–	Power	1.8V/3.3V Digital I/O Power
Power, 1.8V/3.3V I/O	H16	VIOIN	_	–	Power	1.8V/3.3V Digital I/O Power
Power, Bandgap Output	T1	VBGAP	_	–	Power	Bandgap Output
Power, E-fuse	U9	VPP	–	–	Power	E-fuse Programming Voltage
MSS QSPI	E1	MSS_QSPI_CLK	IO	Pull Down	LVCMOS	MSS QSPI Clock Output
MSS QSPI	F2	MSS_QSPI_CS	IO	Pull Up	LVCMOS	MSS QSPI Chip-Select Output
MSS QSPI	C1	MSS_QSPI_D0	IO	Pull Up	LVCMOS	MSS QSPI Data Input/Output 0
MSS QSPI	D2	MSS_QSPI_D1	IO	Pull Down	LVCMOS	MSS QSPI Data Input/Output 1
MSS QSPI	D1	MSS_QSPI_D2	IO	Pull Up	LVCMOS	MSS QSPI Data Input/Output 2
MSS QSPI	E2	MSS_QSPI_D3	IO	Pull Up	LVCMOS	MSS QSPI Data Input/Output 3
MSS UART	G1	MSS_RS232_TX	IO	Pull Disabled	LVCMOS	MSS Debug UART - Transmit Signal
MSS UART	G2	MSS_RS232_RX	IO	Pull Up	LVCMOS	MSS Debug UART - Receive Signal
Radar Front-End	H1	FE1_REFCLK	IO	Pull Down	Clocking	Radar Front-End 1, Reference Clock Input
Radar Front-End	J2	FE2_REFCLK	IO	Pull Down	Clocking	Radar Front-End 2, Reference Clock Input

Table 6-3. Signal Descriptions (continued)

FUNCTION	BALL NUMBER	SIGNAL NAME	TYPE	DEFAULT PULL STATUS	BUFFER TYPE	DESCRIPTION
Radar Front-End	V17	HW_SYNC_FE1	IO	Pull Down	Clocking	Radar Front-End 1, Frame Sync Output
Radar Front-End	W17	HW_SYNC_FE2	IO	Pull Down	Clocking	Radar Front-End 2, Frame Sync Output
Radar Front-End	C15	NERRORIN_FE1	IO	Pull Down	LVCMOS, Open-Drain	Radar Front-End 1, Error Input
Radar Front-End	A16	NERRORIN_FE2	IO	Pull Down	LVCMOS, Open-Drain	Radar Front-End 2, Error Input
Radar Front-End	B15	NRESET_FE1	IO	Pull Down	LVCMOS	Radar Front-End 1, Power-on-Reset Output
Radar Front-End	A15	NRESET_FE2	IO	Pull Down	LVCMOS	Radar Front-End 2, Power-on-Reset Output
Radar Front-End	B14	NWARMRESET_IN_FE1	IO	Pull Down	LVCMOS	Radar Front-End 1, Warm-Reset Output
Radar Front-End	C13	NWARMRESET_IN_FE2	IO	Pull Down	LVCMOS	Radar Front-End 2, Warm-Reset Output
RCSS GPIO	E19	RCSS_GPIO_49	IO	Pull Down	LVCMOS	General-purpose I/O
RCSS SPI A	T18	RCSS_MIBSPIA_CLK	IO	Pull Up	LVCMOS	Radar Control SPI A, Clock Output
RCSS SPI A	T19	RCSS_MIBSPIA_CS0	IO	Pull Up	LVCMOS	Radar Control SPI A, Chip-Select Output
RCSS SPI A	U18	RCSS_MIBSPIA_HOSTIRQ	IO	Pull Down	LVCMOS	Radar Control SPI A, Host Interrupt Input
RCSS SPI A	R17	RCSS_MIBSPIA_MISO	IO	Pull Up	LVCMOS	Radar Control SPI A, Master Input, Slave Output
RCSS SPI A	R18	RCSS_MIBSPIA_MOSI	IO	Pull Up	LVCMOS	Radar Control SPI A, Master Output, Slave Input
RCSS SPI B	V19	RCSS_MIBSPIB_CLK	IO	Pull Up	LVCMOS	Radar Control SPI B, Clock Output
RCSS SPI B	U17	RCSS_MIBSPIB_CS0	IO	Pull Up	LVCMOS	Radar Control SPI B, Chip-Select Output
RCSS SPI B	W18	RCSS_MIBSPIB_HOSTIRQ	IO	Pull Down	LVCMOS	Radar Control SPI B, Host Interrupt Input
RCSS SPI B	V18	RCSS_MIBSPIB_MISO	IO	Pull Up	LVCMOS	Radar Control SPI B, Master Input, Slave Output
RCSS SPI B	U19	RCSS_MIBSPIB_MOSI	IO	Pull Up	LVCMOS	Radar Control SPI B, Master Output, Slave Input
RCSS UART A	A17	RCSS_UARTA_TX	IO	Pull Up	LVCMOS	Radar Control UART A, Transmitter
RCSS UART A	B16	RCSS_UARTA_RX	IO	Pull Up	LVCMOS	Radar Control UART A, Receiver
Reset	L2	NRESET	I	–	LVCMOS, Open-Drain, Failsafe	AM273x Power-on-Reset Input
Reset	K1	WARM_RESET	IO	Pull Disabled	LVCMOS, Open-Drain	AM273x Warm-Reset Input
Reserved	P4	Reserved1	–	–	–	Reserved. Short to VSS on PCB.
Reserved	N3	Reserved2	–	–	–	Reserved. Short to VSS on PCB.

7 Specifications

7.1 Absolute Maximum Ratings

PARAMETER/PIN(1) (2)	DESCRIPTION		MIN	MAX	UNIT
VDD	1.2V digital power supply		-0.5	1.4	V
VIN_SRAM	1.2V power rail for internal SRAM		-0.5	1.4	V
VNWA	1.2V power rail for SRAM array back bias		-0.5	1.4	V
VIOIN	I/O Supply (3.3V or 1.8V): All LVCMOS1833 I/O would operate on this supply		-0.5	3.8	V
VIOIN_18	1.8V supply for CMOS I/O		-0.5	2	V
VIN_18CLK	1.8V supply for clock module		-0.5	2	V
VIOIN_18DIFF	1.8V supply for CSI2 and LVDS ports		-0.5	2	V
Input Voltage	Dual-voltage LVCMOS inputs, operated at 3.3V or 1.8V (Steady State)		-0.3V to VIOIN +0.3V		V
	Dual-voltage LVCMOS inputs, operated at 3.3V/1.8V (Transient Overshoot/Undershoot)		VIOIN +20% up to 20% of Signal Period		V
	CLKP/CLKN		-0.5	2	V
Clamp Current	Limit clamp current(3)		-20	20	mA
T_J	Operating junction temperature range	Automotive	-40	140	°C
		Industrial	-40	105	
T_{stg}	Storage temperature range after soldered onto PC Board		-55	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal GND.
(3) Specifies clamp current that will flow through the internal diode protection cells of the I/O in an overvoltage or undervoltage condition.

7.2 ESD Ratings - Automotive

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	ESD stress voltage HBM, per AEC Q100-002(1)	All pins	±2000	V
		ESD stress voltage CDM, per AEC Q100-011	All pins	±500	
			Corner Pins (A1, A19, W1, W19)	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Power-On Hours (POH)

PARAMETER(1)	EXTENDED INDUSTRIAL	EXTENDED AUTOMOTIVE
Operating Junction Temperature (T_j)	–40°C to 105°C	–40°C to 140°C
POH at Temperature Profile	See the Extended Industrial Temperature Profile	See the Extended Automotive Temperature Profile

(1) This information is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.

7.3.1 Automotive Temperature Profile

Table 7-1. Extended Automotive Temperature Profile

T_J (°C)	HOURS	DAYS	YEARS	PERCENT OF TIME
–40	1200	~50	~0.14	6%
75	4000	~167	~0.46	20%
95	13000	~541	~1.48	65%
130	1600	~67	~0.18	8%
140	200	~8.5	~0.023	1%

Table 7-1. Extended Automotive Temperature Profile (continued)

T_J (°C)	HOURS	DAYS	YEARS	PERCENT OF TIME
Total	20000	~833	~2.28	100%

7.3.2 Industrial Temperature Profile

Table 7-2. Extended Industrial Temperature Profile

T_J (°C)	TOTAL HOURS	TOTAL DAYS	TOTAL YEARS
95	100000	~4166	~11.41
105(1)	70000	~2916	~7.99

(1) Based on operating at CSI2.0 interface at 50% utilization

7.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

SUPPLY NAME	DESCRIPTION	MIN	NOM	MAX	UNIT
Power Supply Conditions					
VDD	1.2-V digital power supply	1.14	1.2	1.32	V
VIN-SRAM	1.2-V power rail for internal SRAM	1.14	1.2	1.32	V
VNWA	1.2-V power rail for SRAM array back bias	1.14	1.2	1.32	V
VIOIN	I/O Supply (3.3-V mode): ALL LVCMOS1833 I/O would operate on this supply	3.135	3.3	3.465	V
VIOIN	I/O Supply (1.8-V mode): ALL LVCMOS1833 I/O would operate on this supply	1.71	1.8	1.89	V
VIOIN_18	1.8V supply for LVCMOS1833 I/O	1.71	1.8	1.9	V
VIN_18CLK	1.8V supply for clock module	1.71	1.8	1.9	V
VIN_18ADC	1.8V supply for ADC module	1.71	1.8	1.9	V
VIN_18CSI	1.8V supply for CSI-2 D-PHY buffers	1.71	1.8	1.9	V
VIOIN_18LVDS	1.8V supply for LVDS buffers	1.71	1.8	1.9	V
VPP	1.7V supply for e-Fuse array	1.65	1.7	1.75	V
I/O Conditions					
LVCMOS V_{IH}	LVCMOS18/33 (1.8V mode) Voltage Input High	1.71			V
	LVCMOS18/33 (3.3V mode) Voltage Input High	2.25			V
LVCMOS V_{IL}	LVCMOS18/33 (1.8V mode) Voltage Input Low			0.3 × VIOIN	V
	LVCMOS18/33 (3.3V mode) Voltage Input Low			0.8 × VIOIN	V
LVCMOS V_{OH}	LVCMOS18/33 (1.8 and 3.3V mode) Voltage Output High (I_{OH} = 6 ma)	VIOIN - 0.450			V
LVCMOS V_{OL}	LVCMOS18/33 (1.8V and 3.3V mode) Voltage Output Low(I_{OL} = 6 ma)			0.45	V
NRESET, SOP[4:0] V_{IH}	NRESET, SOP[4:0], (1.8V mode) Voltage Input High	0.96			V
	NRESET, SOP[4:0], (3.3V mode) Voltage Input High	1.57			V
NRESET, SOP[4:0] V_{IL}	NRESET, SOP[4:0], (1.8V mode) Voltage Input Low			0.2	V
	NRESET, SOP[4:0], (3.3V mode) Voltage Input Low			0.3	V
LVDS TX V_{OH}	Voltage Output High			1.5	V
LVDS TX V_{OL}	Voltage Output Low	0.9			V
CSI2 RX V_{IH}(1)	Voltage Input High - LP Mode	0.74			V
CSI2 RX V_{IL}(1)	Voltage Input Low - LP Mode			0.55	V
CSI2 RX V_{IH}(1)	Voltage Input High - HS Mode			0.46	V

7.4 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

SUPPLY NAME	DESCRIPTION	MIN	NOM	MAX	UNIT
CSI2 RX V_{IL} (1)	Voltage Input Low - HS Mode	-0.04			V
OSC_CLKOUT	Voltage Output High		1.4		V
	Voltage Output Low		VSS		V

(1) CSI2 receivers compatible with MIPI D-PHY standard version 2.1.

7.5 Operating Performance Points

This section describes the operating conditions of the device. This section also contains the description of each Operating Performance Point (OPP) for processor clocks and device core clocks.

Note

The OPP voltage and frequency values may change following the silicon characterization result.

Table 7-3 describes the maximum supported frequency per speed grade for the device.

Table 7-3. Device Speed and Memory Grade

DEVICE	GRADE	RAM (MB)	DSP (MHz)	R5FSS (MHz)
AM2732, AM2732-Q1	D	3.625	450	400

7.6 Power Supply Specifications

Table 7-4 describes the four power rails provided from an external power supply and how they map to major sub-systems and power nets of the AM273x device.

Table 7-4. Power Supply Rails Characteristics

SUPPLY	DEVICE BLOCKS POWERED FROM THE SUPPLY	RELEVANT INPUT POWER NETS ON THE DEVICE
1.8 V	APLL, crystal oscillator, ADC, CSI2, LVDS	Input: VIN18CLK, VIN_18ADC, VIOIN_18DIFF, VIOIN_18LVDS, VIOIN_18CSI
3.3 V (or 1.8 V for 1.8 V I/O mode)	Digital I/O	Input: VIOIN
1.2 V	Core Digital and SRAMs	Input: VDD, VIN_SRAM1, VIN_SRAM2, VIN_SRAM3, VNWA

7.7 I/O Buffer Type and Voltage Rail Dependency

Table 7-5. Buffer Type

BUFFER TYPE (STANDARD)	DESCRIPTION	VOLTAGE RAIL	PERIPHERALS
LVCMOS	Dual voltage 1.8V/3.3V LVCMOS I/O buffer	**VIOIN, VIOIN_18**	**Resets, QSPI, UART, SPI, I^2C, CAN-FD, GPIO, RGMII, MDIO, ePWM, eCAP, JTAG, Trace, SOP, Safety, DMM**
GPADC	General Purpose ADC Input	**VIN_18ADC**	**GPADC**
Clock Subsystem	Clock subsystem crystal or 1.8V single-ended input buffer	**VIN_18CLK**	**CLKP/CLKM**
Clock Subsystem Output	Analog, low-jitter output from clock subsystem	**VIN_18CLK**	**OSC_CLKOUT**
LVDS TX	LVDS high-speed data, differential output buffer	**VIOIN_18DIFF**	**Aurora LVDS**
CSI2.0 RX	MIPI D-PHY CSI2.0 high-speed data, differential input buffer	**VIOIN_18DIFF**	**CSI2**

7.8 CPU Specifications

Table 7-6. CPU and Hardware Accelerator Specifications

	PARAMETER	MIN	NOM	MAX	UNIT
Main Subsystem (MSS)	**Dual-Core Cortex-R5F, ARMv7** (2)				
	L1 Program Memory Cache			16	kB
	L1 Data Memory Chache			16	kB
	L1 Tightly Coupled Memory(3) (TCM) with 32-bit ECC			64	kB
	L2 Memory			960	kB
DSP Subsystem (DSS)	**Single Core C66x DSP**				
	Clock Speed			450	MHz
	L1 Program Memory			32	kB
	L1 Data Memory			32	kB
	L2 Memory(1)			384	kB
Shared Memory	Shared L3 Memory (4)	2000		3625	kB

(1) C66x L2 memory includes up to 256kB configuration as RAM or cache
(2) R5F dual-cores configuration as single, redundant, lock-step device, or two independent cores
(3) L1 64kB tightly coupled memory shared between lock-step devices, or 32kB L1 for each core when operating in dual-core mode.
(4) Sharable across R5F, C66x, and HWA subsystems

7.9 Thermal Resistance Characteristics for nFBGA Package [ZCE285A]

THERMAL METRICS(1)		°C/W(2) (3)
$R\Theta_{JC}$	Junction-to-case	6.2
$R\Theta_{JB}$	Junction-to-board	5.7
$R\Theta_{JA}$	Junction-to-free air	17.3
Psi_{JT}	Junction-to-package top	1.0
Psi_{JB}	Junction-to-board	5.6

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.
(2) °C/W = degrees Celsius per watt.
(3) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

7.10 Power Consumption Summary

Table Table 7-7 summarizes average power consumption of the AM273x device for a set of typical application utilization and thermal parameters. Table Table 7-8 shows hypothetical peak current for the device. Both of these tables can be used to scale power regulator and PCB design. However, specific power utilization of the device is dependent on the software utilization of device cores, accelerators and peripherals and operating temperature. To facilitate accurate power planning, TI provides a power estimation tool (PET) spreadsheet which can be used for estimating device power utilization across a wide number of scenarios. Please see sprad10 for more information.

Table 7-7. Average Power and Current

PARAMETER	SUPPLY NAME	SUPPLY DESCRIPTION	AVERAGE POWER (mW)	AVERAGE CURRENT (mA)
Average Power and Current Consumption for Typical Control and Processing Use-Case: • C66x DSP: 450 MHz, 50% Utilization • R5F Dual Core: 400 MHz, 70% Utilization • CSI2-A/B: 4-Lane, 600 Mbps Operation • SPI: 10% Utilization • Ethernet: 100Mbps Operation, 70% Utilization • CAN: 8Mbps Operation, 10% Utilization • SPI: 25 Mbps Operation, 10% Utilization • T_J= 25 C	VDD	1.2V Core Digital Power	692	576
	VDD_SRAM	1.2V SRAM Power	3	3
	VIOIN	1.8V or 3.3V Digital I/O Power	12	4
	VIOIN_18	1.8V Digital I/O Power	0	0
	VIOIN_18CLK	1.8V Clocking Power	32	18
	VIOIN_18ADC	1.8V ADC Power	3	2
	VIOIN_18CSI	1.8V CSI Power	40	22
	VIOIN_18LVDS	1.8V LVDS Power	125	69
Total Power			907	

Table 7-8. Peak Current

SUPPLY NAME	SUPPLY DESCRIPTION	PEAK CURRENT (mA)
VDD	1.2V Core Digital Power	2315
VDD_SRAM	1.2V SRAM Power	75
VIOIN	1.8V or 3.3V Digital I/O Power	74
VIOIN_18	1.8V Digital I/O Power	1
VIOIN_18CLK	1.8V Clocking Power	18
VIOIN_18ADC	1.8V ADC Power	2
VIOIN_18CSI	1.8V CSI Power	23
VIOIN_18LVDS	1.8V LVDS Power	70

7.11 Timing and Switching Characteristics

7.11.1 Power Supply Sequencing and Reset Timing

The AM273x device expects all external voltage rails and SOP boot mode select lines to be stable before NRESET is de-asserted (brought from VSS level to VIOIN level). Likewise external voltage rails should only be powered down after NRESET is asserted (brought from VIOIN level to VSS level).Figure 7-1 describes the device wake-up and power-down sequence.

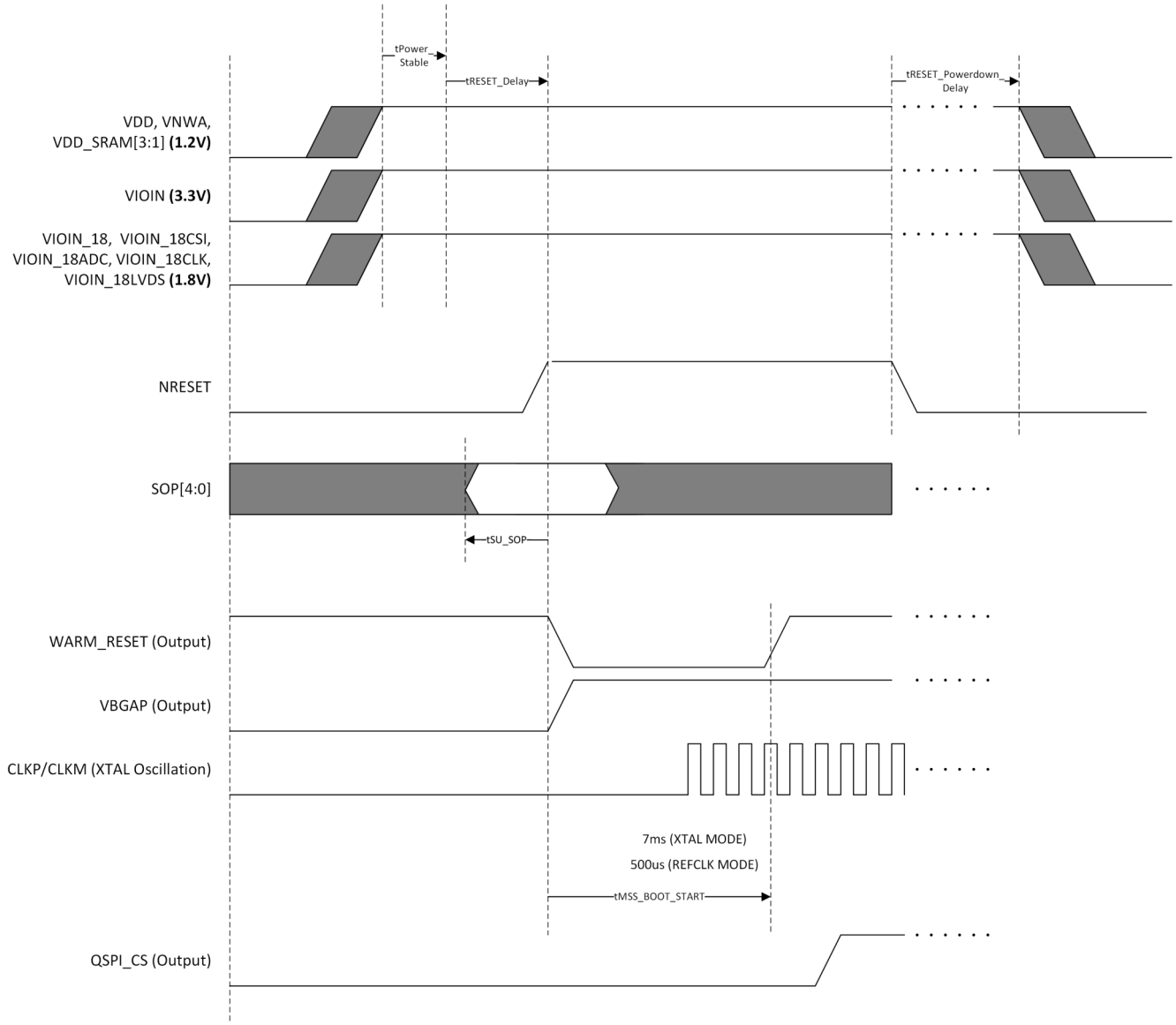


Figure 7-1. Device Wake-up and Power-Down Sequence

Table 7-9 lists the timing values shown in Figure 7-1.

Table 7-9. Device Wake-Up Sequence Timing

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{POWER_STABLE}	Settling time after initial power supply turn-on after which device power nets are at valid, recommended operating conditions. NRESET should not be de-asserted (brought from GND to VIOIN level) before all power pins are at recommended operating point. See Recommended Operating Conditions for recommended operating conditions of all device power pins.	0			ms
t_{RESET_DELAY}	Delay after device power nets are at valid, nominal values, when NRESET can be brought from VSS to VIOIN level. NRESET can be brought from VSS to VIOIN level anytime after power supplies are at recommended operating conditions.	0			ms

Table 7-9. Device Wake-Up Sequence Timing (continued)

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{SU_SOP}	Setup time for SOP signals to be sampled by the rising edge of NRESET. Device is ready to sample SOP pin states anytime after power supplies are at recommended operating conditions.	0			ms
$t_{MSS\_BOOT\_START}$	Typical delay after NRESET rising edge before boot ROM to begins MSS code execution. Value depends on whether device is operating directly from a crystal source or oscillator (REFCLK) source. Faster startup possible with the oscillator mode.	0.5		7.0	ms
$t_{RESET\_POWER\_DELAY}$	During power off events, delay after NRESET is brought from VIOIN to VSS level to when power pins can be powered off. Device power pins can be powered off anytime after NRESET is brought to VSS level.	0			ms

7.11.2 Clock Specifications

An external crystal is connected to the device pins. Figure 7-2 shows the crystal implementation.

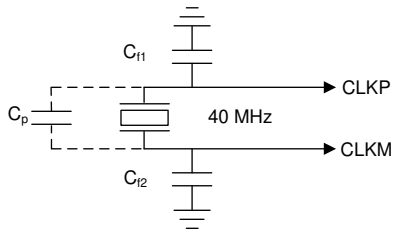


Figure 7-2. Crystal Implementation

Note

The load capacitors, C_{f1} and C_{f2} in Figure 7-2, should be chosen such that Equation 1 is satisfied. C_L in the equation is the load specified by the crystal manufacturer. All discrete components used to implement the oscillator circuit should be placed as close as possible to the associated oscillator CLKP and CLKM pins. Note that Cf1 and Cf2 include the parasitic capacitances due to PCB routing.

$$C_L = C_{f1} \times \frac{C_{f2}}{C_{f1} + C_{f2}} + C_P \quad (1)$$

Table 7-10 lists the electrical characteristics of the clock crystal.

Table 7-10. Crystal Electrical Characteristics (Oscillator Mode)

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
f_P	Parallel resonance crystal frequency		40		MHz
C_L	Crystal load capacitance	5	8	12	pF
ESR	Crystal ESR			50	Ω
Temperature range	Expected temperature range of operation	–40		150	°C
Frequency tolerance	Crystal frequency tolerance(1) (2) (3)	–200		200	ppm
Drive level			50	200	µW

(1) The crystal manufacturer's specification must satisfy this requirement.
(2) Includes initial tolerance of the crystal, drift over temperature, aging and frequency pulling due to incorrect load capacitance.
(3) Crystal tolerance affects sensor accuracy if AM273x used as clock source for attached sensors.

A non-crystal oscillator can also be used as the clock reference source. In this case the signal is fed to the CLKP pin only and CLKM is grounded. Table 7-11 lists the electrical, AC timing, and phase noise requirements of the external oscillator input signal.

Table 7-11. External Clock Mode Input Requirements

PARAMETER		SPECIFICATION			UNIT
		MIN	TYP	MAX	
Input Clock: External AC-coupled sine wave or DC-coupled square wave Phase Noise referrenced to 40 MHz	Frequency		40		MHz
	AC-Amplitude	700		1200	mV (pp)
	DC-V_{IL}	0.00		0.02	V
	DC-V_{IH}	1.40		1.95	V
	DC-$t_{rise/fall}$			10	ns
	Phase Noise at 1 kHz			–132	dBc/Hz
	Phase Noise at 10 kHz			–143	dBc/Hz
	Phase Noise at 100 kHz			–152	dBc/Hz
	Phase Noise at 1 MHz			–153	dBc/Hz
	Duty Cycle	35		65	%
	Freq Tolerance	–50		50	ppm

7.11.3 Peripheral *Information*

Initial peripheral descriptions and features are provided in the following sections. Additional peripheral details and interface timing information shall be provided in a later product preview or datasheet release.

7.11.3.1 QSPI Flash Memory Peripheral

AM273x includes a Quad-Serial Peripheral Interface for external flash memory access. Flash memory can be be utilized for many purposes including: Secondary boot-loader memory, application program memory, security keys storage, and long-term data logs for security and error conditions.

- ROM bootloader auto identification of supported flash through flash device ID (DEVID) register
- Loopback skew cancellation for clock signal to supported faster flash interface clock rates
- Two chip-select signals to connect two external flash devices
- Memory mapped 'direct' mode and software triggered 'indirect' mode of operation for performing flash data transfers
- 67 MHz operating clock supported

7.11.3.1.1 QSPI Timing Conditions

SPECIFICATION NUMBER	PARAMETER		MIN	TYP	MAX	UNIT
	Input Conditions					
1	t_R	Input rise time	1		3	ns
2	t_F	Input fall time	1		3	ns
	Output Conditions					
3	C_{LOAD}	Output load capacitance	2		15	pF

7.11.3.1.2 QSPI Timing Requirements

SPECIFICATION NUMBER	PARAMETER[1], [2], [3]		MIN	TYP	MAX	UNIT
Q12	$t_{su(D-SCLK)}$	Setup time, D[3:0] valid before falling SCLK edge	5			ns
Q13	$t_{h(SCLK-D)}$	Hold time, D[3:0] valid after falling SCLK edge	0			ns

SPECIFICATION NUMBER	PARAMETER[1], [2], [3]		MIN	TYP	MAX	UNIT
Q14	$t_{su(D-SCLK)}$	Setup time, final D[3:0] bit valid before final falling SCLK edge	5-P			ns
Q15	$t_{h(SCLK-D)}$	Hold time, final D[3:0] bit valid after final falling SCLK edge	0+P			ns

(1) Clock Mode 0 (clock polarity = 0 ; clockk phase = 0) is the mode of operation.
(2) The Device captures data on the falling clock edge in Clock Mode 0, as opposed to the traditional rising clock edge. Although nonstandard, The falling-edge-based setup and hold time timings have been designed to be compatible with standard SPI devices that launch data on the falling edge in Clock Mode 0.
(3) P = SCLK period in ns.

7.11.3.1.3 QSPI Switching Characteristics

SPECIFICATION NUMBER	PARAMETER[1], [2]		MIN	TYP	MAX	UNIT
Q1	$t_{c(SCLK)}$	Cycle time, sclk	14.9			ns
Q2	$t_{w(SCLKL)}$	Pulse duration, sclk low	0.5*P – 1.5			ns
Q3	$t_{w(SCLKH)}$	Pulse duration, sclk high	0.5*P – 1.5			ns
Q4	$t_{d(CS-SCLK)}$	Delay time, sclk falling edge to cs active edge	–M*P – 1		–M*P + 2.5	ns
Q5	$t_{d(SCLK-CS)}$	Delay time, sclk falling edge to cs inactive edge	N*P – 1		N*P + 2.5	ns
Q6	$t_{d(SCLK-D0)}$	Delay time, sclk falling edge to d[0] transition	–3		5.2	ns
Q7	$t_{ena(CS-D0LZ)}$	Enable time, cs active edge to d[0] driven (lo-z)	–P – 4		–P +3.5	ns
Q8	$t_{dis(CS-D0Z)}$	Disable time, cs active edge to d[0] tri-stated (hi-z)	–P – 4		–P +3.5	ns
Q9	$t_{d(SCLK-D0)}$	Delay time, sclk first falling edge to first d[0] transition (for PHA = 0 only)	–3– P		3.5 – P	ns

(1) P = SCLK period in ns.
(2) M = QSPI_SPI_DC_REG.DDx + 1, N = 2

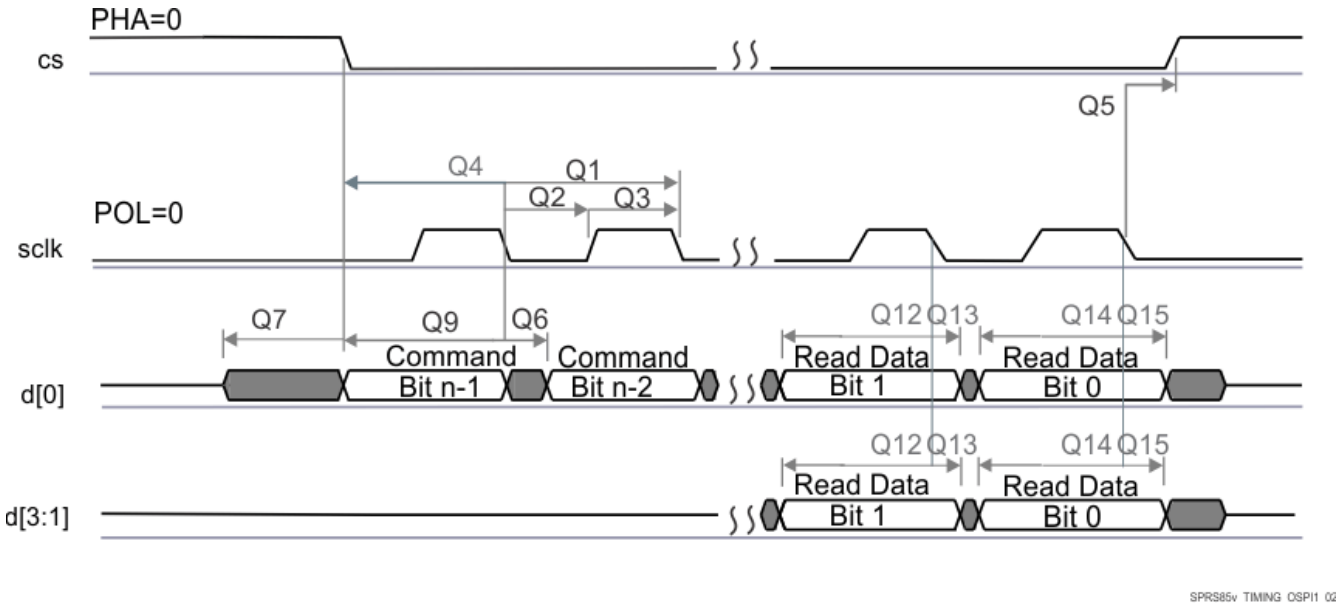


Figure 7-3. QSPI Read (Clock Mode 0)

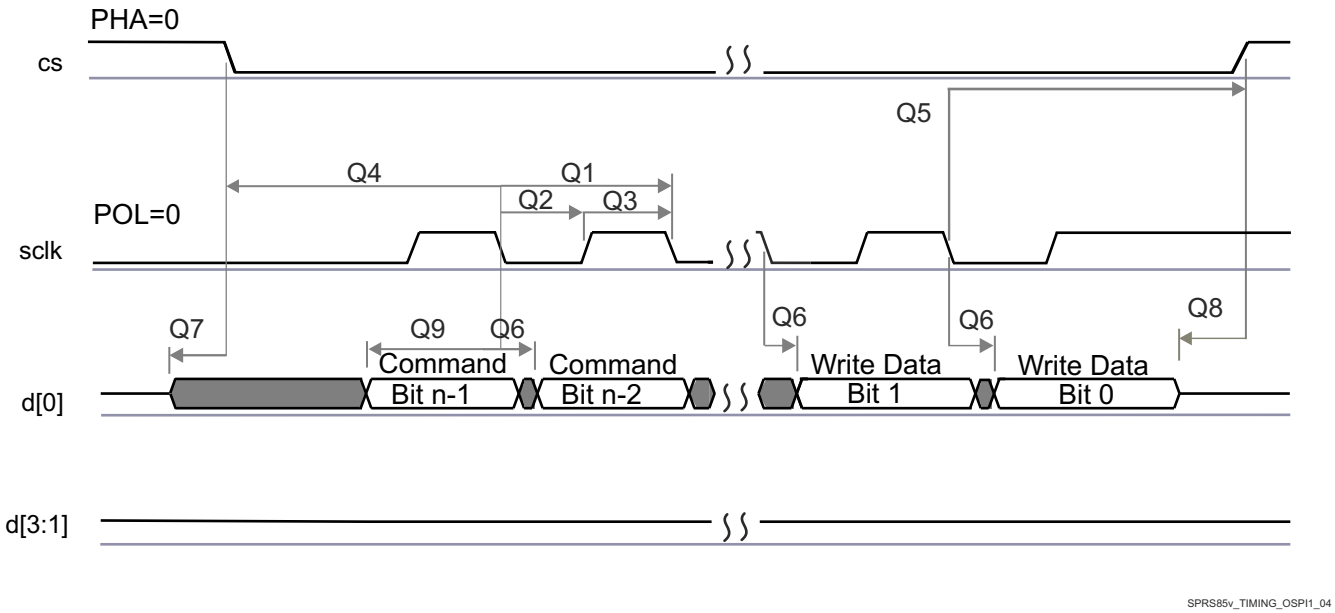


Figure 7-4. QSPI Write (Clock Mode 0)

7.11.3.2 MIBSPI Peripheral

AM273x includes four, Multi-Buffered Serial Peripheral Interface (MIBSPI) master interfaces. Two of these interfaces are intended for external MCU, PMIC, EEPROM, Watchdog, and other system-level communication. The other two interfaces are intended for independently mastering SPI device sensors.

- Maximum clock rate supported over each MIBSPI module is 25 MHz.

7.11.3.2.1 SPI Timing Conditions

NO.	PARAMETER		MIN	TYP	MAX	UNIT
Input Conditions						
1	t_R	Input rise time	1		3	ns
2	t_F	Input fall time	1		3	ns
Output Conditions						
3	C_{LOAD}	Output load capacitance	2		15	pF

7.11.3.2.2 SPI Master Mode Timing and Switching Parameters (CLOCK PHASE = 0, SPICLK = output, SPISIMO = output, and SPISOMI = input)

The following tables and figures present timing requirements and switching characteristics for SPI – Master Mode.

Table 7-12. SPI Master Mode Switching Characteristics (CLOCK PHASE = 0, SPICLK = output, SPISIMO = output, and SPISOMI = input)[(1)(3)]

see Figure 7-5 and Figure 7-6

NO.	PARAMETER		MIN	TYP	MAX	UNIT
1	$t_{c(SPC)M}$	Cycle time, SPICLK[(2)]	40		$256t_{c(VCLK)}$	ns
2	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)M} - 4$		$0.5t_{c(SPC)M} + 4$	ns
	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)M} - 4$		$0.5t_{c(SPC)M} + 4$	
3	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 0)	$0.5t_{c(SPC)M} - 4$		$0.5t_{c(SPC)M} + 4$	ns
	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 1)	$0.5t_{c(SPC)M} - 4$		$0.5t_{c(SPC)M} + 4$	

Table 7-12. SPI Master Mode Switching Characteristics (CLOCK PHASE = 0, SPICLK = output, SPISIMO = output, and SPISOMI = input)[1][3] (continued)

see Figure 7-5 and Figure 7-6

NO.	PARAMETER			MIN	TYP	MAX	UNIT
4	$t_{d(SPCH-SIMO)M}$	Delay time, SPISIMO valid before SPICLK low, (clock polarity = 0)		$0.5t_{c(SPC)M} - 13$			ns
	$t_{d(SPCL-SIMO)M}$	Delay time, SPISIMO valid before SPICLK high, (clock polarity = 1)		$0.5t_{c(SPC)M} - 13$			
5	$t_{v(SPCL-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK low, (clock polarity = 0)		$0.5t_{c(SPC)M} - 10.5$			ns
	$t_{v(SPCH-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK high, (clock polarity = 1)		$0.5t_{c(SPC)M} - 10.5$			
6	$t_{C2TDELAY}$	Setup time CS active until SPICLK high (clock polarity = 0)[5]	CSHOLD = 0	(C2TDELAY+2)* $t_{c(VCLK)} - 7.5$		(C2TDELAY+2) * $t_{c(VCLK)} + 7$	ns
			CSHOLD = 1	(C2TDELAY +3) * $t_{c(VCLK)} - 7.5$		(C2TDELAY+3) * $t_{c(VCLK)} + 7$	
		Setup time CS active until SPICLK low (clock polarity = 1)[5]	CSHOLD = 0	(C2TDELAY+2)* $t_{c(VCLK)} - 7.5$		(C2TDELAY+2) * $t_{c(VCLK)} + 7$	
			CSHOLD = 1	(C2TDELAY +3) * $t_{c(VCLK)} - 7.5$		(C2TDELAY+3) * $t_{c(VCLK)} + 7$	
7	$t_{T2CDELAY}$	Hold time, SPICLK low until CS inactive (clock polarity = 0)[5]		$0.5*t_{c(SPC)M}$ + (T2CDELAY + 1) * $t_{c(VCLK)} - 7$		$0.5*t_{c(SPC)M}$ + (T2CDELAY + 1) * $t_{c(VCLK)}$ + 7.5	ns
		Hold time, SPICLK high until CS inactive (clock polarity = 1)[5]		$0.5*t_{c(SPC)M}$ + (T2CDELAY + 1) * $t_{c(VCLK)} - 7$		$0.5*t_{c(SPC)M}$ + (T2CDELAY + 1) * $t_{c(VCLK)}$ + 7.5	

Table 7-13. SPI Master Mode Timing Requirements (CLOCK PHASE = 0, SPICLK = output, SPISIMO = output, and SPISOMI = input)[1][3]

see Figure 7-5

NO.	PARAMETER		MIN	TYP	MAX	UNIT
8	$t_{su(SOMI-SPCL)M}$	Setup time, SPISOMI before SPICLK low (clock polarity = 0)[4]	5			ns
	$t_{su(SOMI-SPCH)M}$	Setup time, SPISOMI before SPICLK high (clock polarity = 1)[4]	5			
9	$t_{h(SPCL-SOMI)M}$	Hold time, SPISOMI data valid after SPICLK low (clock polarity = 0)[4]	3			ns
	$t_{h(SPCH-SOMI)M}$	Hold time, SPISOMI data valid after SPICLK high (clock polarity = 1)[4]	3			

(1) The MASTER bit (SPIGCRx.0) is set and the CLOCK PHASE bit (SPIFMTx.16) is cleared (where x= 0 or 1).
(2) $t_{c(MSS\_VCLK)}$ = main subsystem clock time = 1 / $f_{(MSS\_VCLK)}$. For more details, see the Technical Reference Manual.
(3) When the SPI is in Master mode, the following must be true: For PS values from 1 to 255: $t_{c(SPC)M} \geq (PS+1)t_{c(MSS\_VCLK)} \geq 25$ ns, where PS is the prescale value set in the SPIFMTx.[15:8] register bits. For PS values of 0: $t_{c(SPC)M} = 2t_{c(MSS\_VCLK)} \geq 25$ ns.
(4) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).
(5) C2TDELAY and T2CDELAY is programmed in the SPIDELAY register.

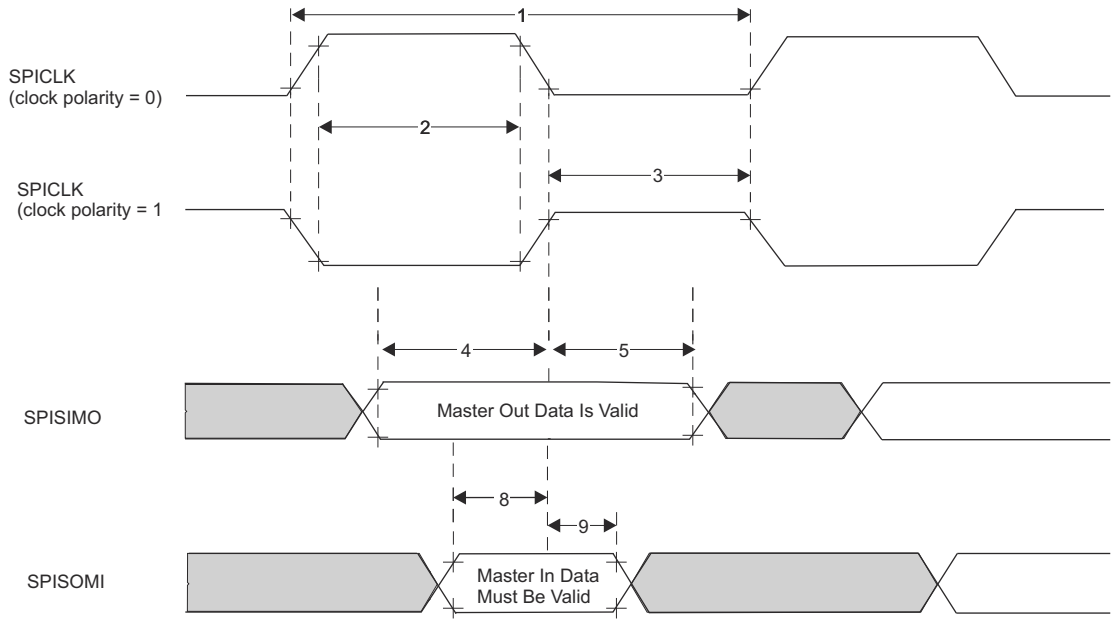


Figure 7-5. SPI Master Mode External Timing (CLOCK PHASE = 0)

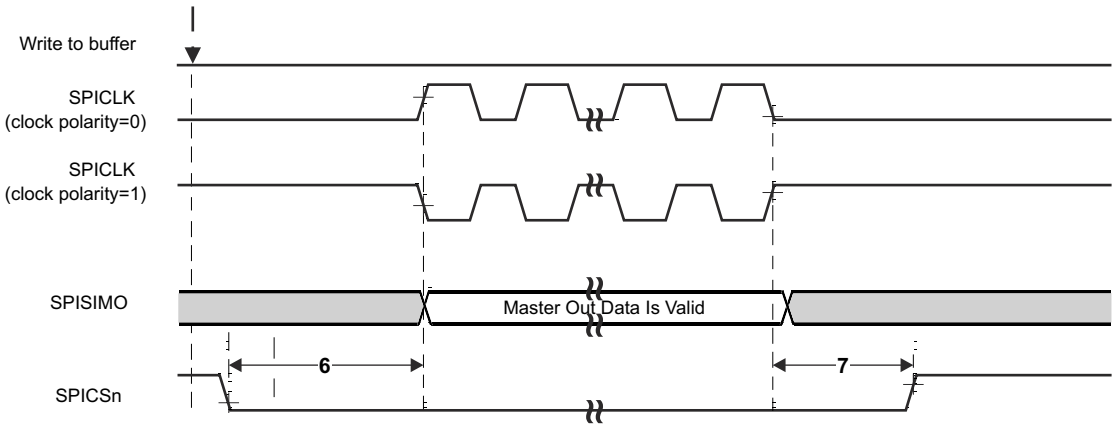


Figure 7-6. SPI Master Mode Chip Select Timing (CLOCK PHASE = 0)

7.11.3.2.3 SPI Master Mode Timing and Switching Parameters (CLOCK PHASE = 1, SPICLK = output, SPISIMO = output, and SPISOMI = input)

Table 7-14. SPI Master Mode Switching Characteristics (CLOCK PHASE = 1, SPICLK = output, SPISIMO = output, and SPISOMI = input)[(1)(3)]

see Figure 7-5 and Figure 7-8

NO.	PARAMETER		MIN	TYP	MAX	UNIT
1	$t_{c(SPC)M}$	Cycle time, SPICLK[(2)]	40		$256t_{c(VCLK)}$	ns
2	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)M} - 4$		$0.5t_{c(SPC)M} + 4$	ns
	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)M} - 4$		$0.5t_{c(SPC)M} + 4$	
3	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 0)	$0.5t_{c(SPC)M} - 4$		$0.5t_{c(SPC)M} + 4$	ns
	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 1)	$0.5t_{c(SPC)M} - 4$		$0.5t_{c(SPC)M} + 4$	
4	$t_{d(SPCH-SIMO)M}$	Delay time, SPISIMO valid before SPICLK low, (clock polarity = 0)	$0.5t_{c(SPC)M} - 13$			ns
	$t_{d(SPCL-SIMO)M}$	Delay time, SPISIMO valid before SPICLK high, (clock polarity = 1)	$0.5t_{c(SPC)M} - 13$			

Table 7-14. SPI Master Mode Switching Characteristics (CLOCK PHASE = 1, SPICLK = output, SPISIMO = output, and SPISOMI = input)[1][3] (continued)

see Figure 7-5 and Figure 7-8

NO.	PARAMETER			MIN	TYP	MAX	UNIT
5	$t_{v(SPCL-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK low, (clock polarity = 0)		$0.5t_{c(SPC)M} - 10.5$			ns
	$t_{v(SPCH-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK high, (clock polarity = 1)		$0.5t_{c(SPC)M} - 10.5$			
6	$t_{C2TDELAY}$	Setup time CS active until SPICLK high (clock polarity = 0)[5]	CSHOLD = 0	$0.5*t_{c(SPC)M} + (C2TDELAY + 2)*t_{c(VCLK)} - 7.5$		$0.5*t_{c(SPC)M} + (C2TDELAY+2) * t_{c(VCLK)} + 7$	ns
			CSHOLD = 1	$0.5*t_{c(SPC)M} + (C2TDELAY + 2)*t_{c(VCLK)} - 7.5$		$0.5*t_{c(SPC)M} + (C2TDELAY+2) * t_{c(VCLK)} + 7$	
		Setup time CS active until SPICLK low (clock polarity = 1)[5]	CSHOLD = 0	$0.5*t_{c(SPC)M} + (C2TDELAY+2)*t_{c(VCLK)} - 7.5$		$0.5*t_{c(SPC)M} + (C2TDELAY+2) * t_{c(VCLK)} + 7$	
			CSHOLD = 1	$0.5*t_{c(SPC)M} + (C2TDELAY+3)*t_{c(VCLK)} - 7.5$		$0.5*t_{c(SPC)M} + (C2TDELAY+3) * t_{c(VCLK)} + 7$	
7	$t_{T2CDELAY}$	Hold time, SPICLK low until CS inactive (clock polarity = 0)[5]		$(T2CDELAY + 1) *t_{c(VCLK)} - 7.5$		$(T2CDELAY + 1) *t_{c(VCLK)} + 7$	ns
		Hold time, SPICLK high until CS inactive (clock polarity = 1)[5]		$(T2CDELAY + 1) *t_{c(VCLK)} - 7.5$		$(T2CDELAY + 1) *t_{c(VCLK)} + 7$	

Table 7-15. SPI Master Mode Timing Requirements (CLOCK PHASE = , SPICLK = output, SPISIMO = output, and SPISOMI = input)[1][3]

see Figure 7-5 and Figure 7-8

NO.	PARAMETER		MIN	TYP	MAX	UNIT
8	$t_{su(SOMI-SPCL)M}$	Setup time, SPISOMI before SPICLK low (clock polarity = 0)[4]	5			ns
	$t_{su(SOMI-SPCH)M}$	Setup time, SPISOMI before SPICLK high (clock polarity = 1)[4]	5			
9	$t_{h(SPCL-SOMI)M}$	Hold time, SPISOMI data valid after SPICLK low (clock polarity = 0)[4]	3			ns
	$t_{h(SPCH-SOMI)M}$	Hold time, SPISOMI data valid after SPICLK high (clock polarity = 1)[4]	3			

(1) The MASTER bit (SPIGCRx.0) is set and the CLOCK PHASE bit (SPIFMTx.16) is set (where x = 0 or 1).
(2) $t_{c(MSS\_VCLK)}$ = main subsystem clock time = 1 / $f_{(MSS\_VCLK)}$. For more details, see the Technical Reference Manual.
(3) When the SPI is in Master mode, the following must be true: For PS values from 1 to 255: $t_{c(SPC)M} \geq (PS +1)t_{c(MSS\_VCLK)} \geq 25$ ns, where PS is the prescale value set in the SPIFMTx.[15:8] register bits. For PS values of 0: $t_{c(SPC)M} = 2t_{c(MSS\_VCLK)} \geq 25$ ns.
(4) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).
(5) C2TDELAY and T2CDELAY is programmed in the SPIDELAY register

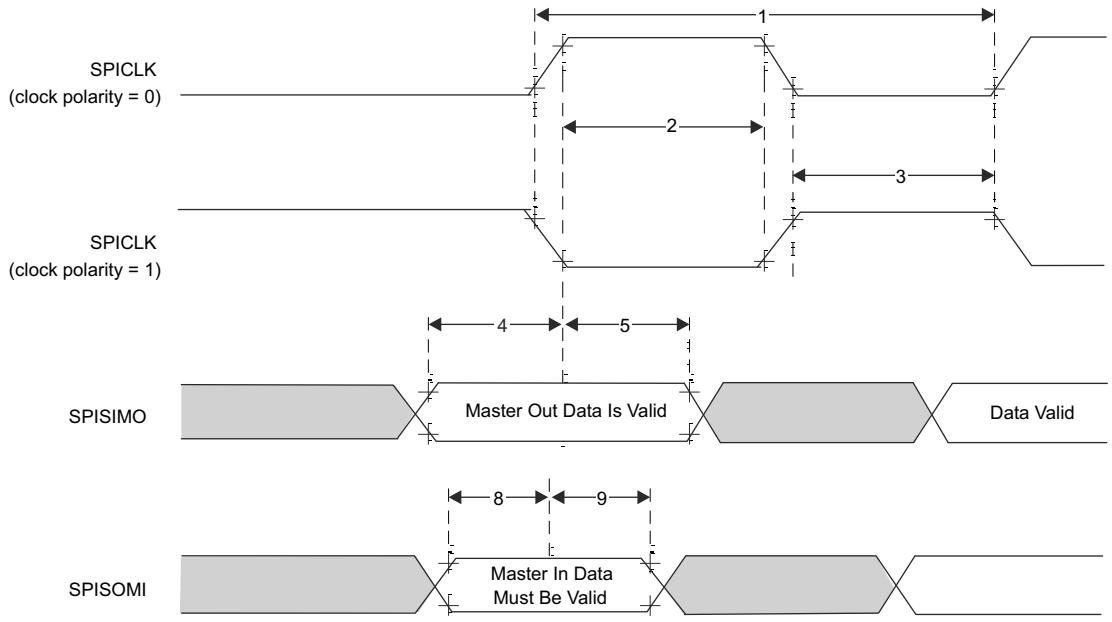


Figure 7-7. SPI Master Mode External Timing (CLOCK PHASE = 1)

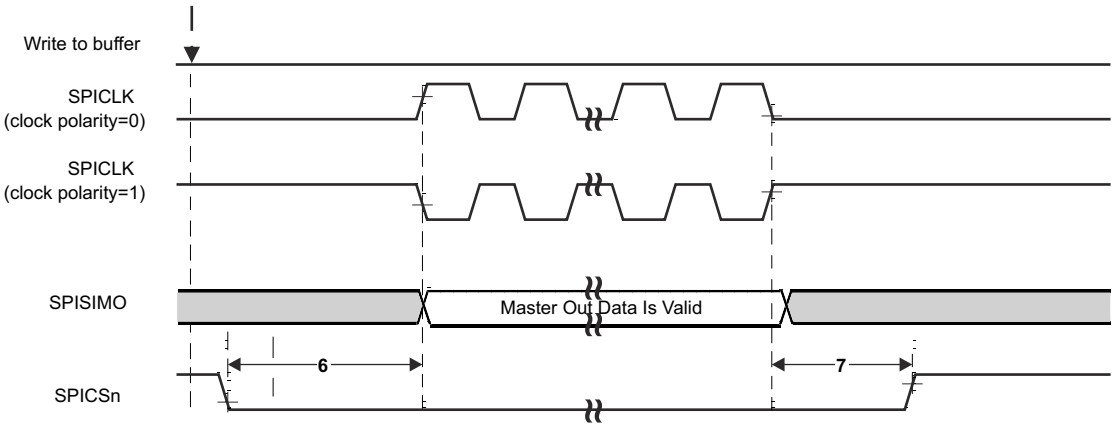


Figure 7-8. SPI Master Mode Chip Select Timing (CLOCK PHASE = 1)

7.11.3.2.4 SPI Slave Mode Timing and Switching Parameters (SPICLK = input, SPISIMO = input, and SPISOMI = output)

Table 7-16. SPI Slave Mode Timing Parameters (SPICLK = input, SPISIMO = input, and SPISOMI = output) (1)(2)

see Figure 7-9 and Figure 7-10

NO.	PARAMETER		MIN	TYP	MAX	UNIT
1	$t_{c(SPC)S}$	Cycle time, SPICLK (2)	25			ns
2	$t_{w(SPCH)S}$	Pulse duration, SPICLK high (clock polarity = 0)	10			ns
	$t_{w(SPCL)S}$	Pulse duration, SPICLK low (clock polarity = 1)	10			
3	$t_{w(SPCL)S}$	Pulse duration, SPICLK low (clock polarity = 0)	10			ns
	$t_{w(SPCH)S}$	Pulse duration, SPICLK high (clock polarity = 1)	10			
4	$t_{d(SPCH-SOMI)S}$	Delay time, SPISOMI valid after SPICLK high (clock polarity = 0; clock phase = 0) OR (clock polarity = 1; clock phase = 1) (3)			11	ns
	$t_{d(SPCL-SOMI)S}$	Delay time, SPISOMI valid after SPICLK low (clock polarity = 1; clock phase = 0) OR (clock polarity = 0; clock phase = 1) (3)			11	

Table 7-16. SPI Slave Mode Timing Parameters (SPICLK = input, SPISIMO = input, and SPISOMI = output) (1)(2) (continued)

see Figure 7-9 and Figure 7-10

NO.	PARAMETER		MIN	TYP	MAX	UNIT
5	$t_{h(SPCH-SOMI)S}$	Hold time, SPISOMI data valid after SPICLK high (clock polarity = 0; clock phase = 0) OR (clock polarity = 1; clock phase = 1)(3)	2			ns
	$t_{h(SPCL-SOMI)S}$	Hold time, SPISOMI data valid after SPICLK low (clock polarity = 1; clock phase = 0) OR (clock polarity = 0; clock phase = 1)(3)	2			

Table 7-17. SPI Slave Mode Switching Characteristics (SPICLK = input, SPISIMO = input, and SPISOMI = output)(1)(2)

see Figure 7-9 and Figure 7-10

NO.	PARAMETER		MIN	TYP	MAX	UNIT
6	$t_{su(SIMO-SPCL)S}$	Setup time, SPISIMO before SPICLK low (clock polarity = 0; clock phase = 0) OR (clock polarity = 1; clock phase = 1)(4)	4.5			ns
	$t_{su(SIMO-SPCH)S}$	Setup time, SPISIMO before SPICLK high (clock polarity = 1; clock phase = 0) OR (clock polarity = 0; clock phase = 1)(4)	4.5			
7	$t_{h(SPCL-SIMO)S}$	Hold time, SPISIMO data valid after SPICLK low (clock polarity = 0; clock phase = 0) OR (clock polarity = 1; clock phase = 1)(4)	1			ns
	$t_{h(SPCL-SIMO)S}$	Hold time, SPISIMO data valid after SPICLK high (clock polarity = 1; clock phase = 0) OR (clock polarity = 0; clock phase = 1)(4)	1			

(1) The MASTER bit (SPIGCRx.0) is cleared (where x = 0 or 1).
(2) If the SPI is in slave mode, the following must be true: $t_{c(SPC)S} \geq (PS + 1)\ t_{c(MSS\_VCLK)}$, where PS = prescale value set in SPIFMTx.[15:8].
(3) When the SPI is in Slave mode, the following must be true: For PS values from 1 to 255: $t_{c(SPC)S} \geq (PS +1)t_{c(MSS\_VCLK)} \geq 25$ ns, where PS is the prescale value set in the SPIFMTx.[15:8] register bits.For PS values of 0: $t_{c(SPC)S} = 2t_{c(MSS\_VCLK)} \geq 25$ ns.
(4) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).

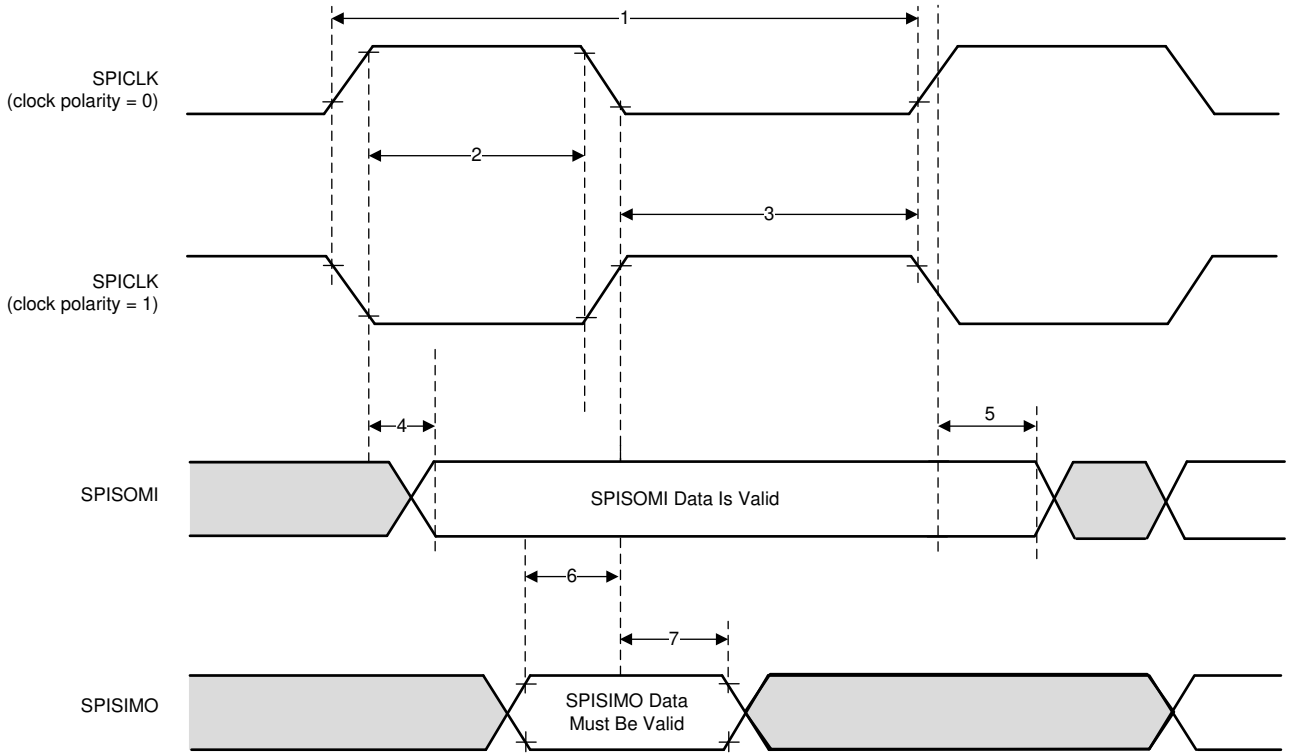


Figure 7-9. SPI Slave Mode External Timing (CLOCK PHASE = 0)

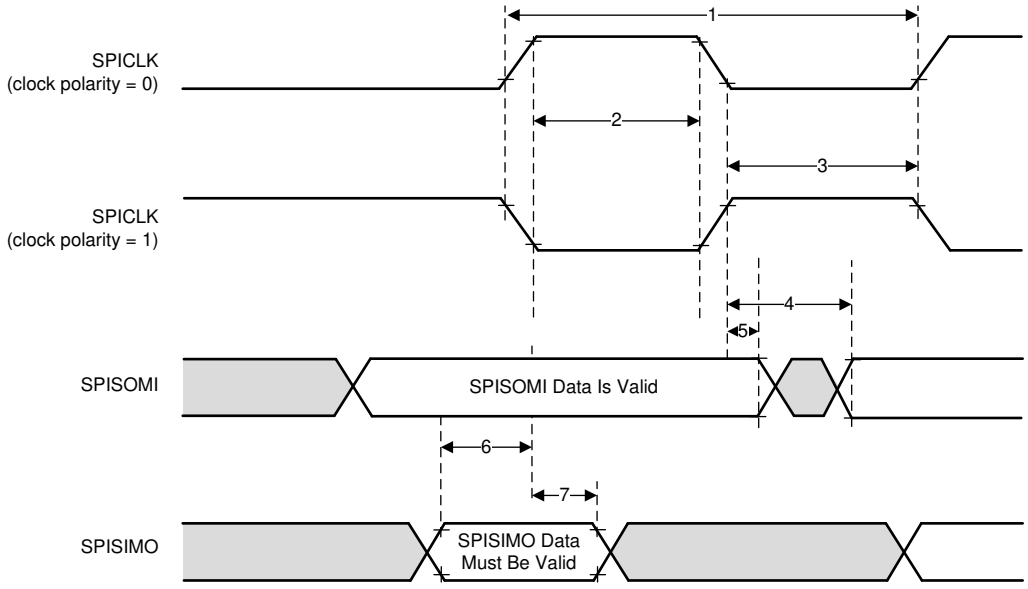


Figure 7-10. SPI Slave Mode External Timing (CLOCK PHASE = 1)

7.11.3.3 Ethernet Switch (RGMII/RMII/MII) Peripheral

AM273x integrates a two port Ethernet switch with one external RGMII/RMII/MII port and another port servicing the Master Sub-System (MSS). This interface is intended to operate primarily as a 100Mbps ECU interface. It can also be used as an instrumentation interface.

- Full Duplex 10/100Mbps wire rate interface to Ethernet PHY over RGMII, RMII, or MII parallel interface
- MDIO Clause 22 and 45 PHY management interface
- IEEE 1588 Synchronous Ethernet support
- Synchronous trigger output allowing Ethernet to trigger CSI data frames

7.11.3.3.1 RGMII/GMII/MII Timing Conditions

SPECIFICATION NUMBER	PARAMETER		MIN	TYP	MAX	UNIT
	Input Conditions					
1	t_R	Input rise time	1		3	ns
2	t_F	Input fall time	1		3	ns
	Output Conditions					
3	C_{LOAD}	Output load capacitance	2		20	pF

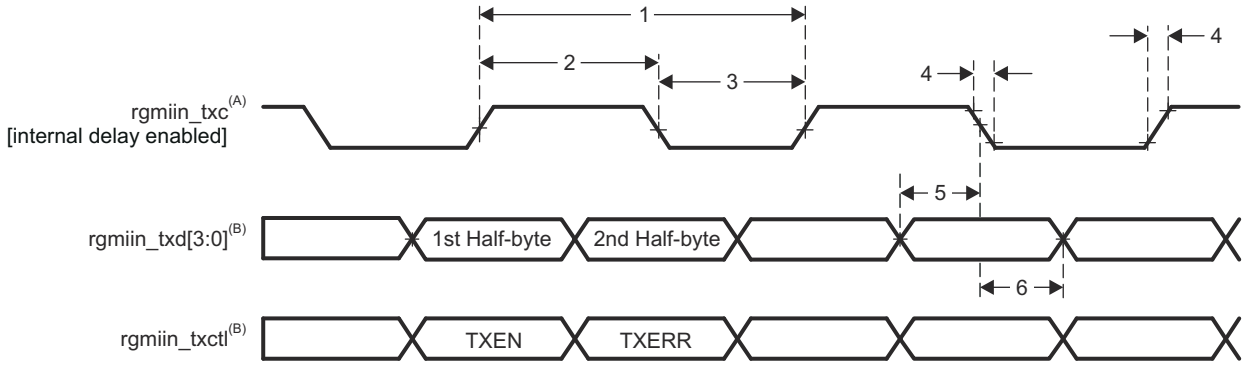
7.11.3.3.2 RGMII Transmit Clock Switching Characteristics

NO.	PARAMETER	DESCRIPTION	SPEED	MIN	MAX	UNIT
1	$t_{c(TXC)}$	Cycle time, rgmiin_txc	10 Mbps	360	440	ns
			100 Mbps	36	44	ns
2	$t_{w(TXCH)}$	Pulse duration, rgmiin_txc high	10 Mbps	160	240	ns
			100 Mbps	16	24	ns
3	$t_{w(TXCL)}$	Pulse duration, rgmiin_txc low	10 Mbps	160	240	ns
			100 Mbps	16	24	ns
4	$t_{t(TXC)}$	Transition time, rgmiin_txc	10 Mbps		0.75	ns
			100 Mbps		0.75	ns

7.11.3.3.3 RGMII Transmit Data and Control Switching Characteristics

NO.(1)	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
5	$t_{osu(TXD-TXC)}$	Output Setup time, transmit selected signals valid to MSS_RGMII_TCLK high/low	RGMII, Internal Delay Enabled, 10/100 Mbps	1.2		ns
6	$t_{oh(TXC-TXD)}$	Output Hold time, transmit selected signals valid after MSS_RGMII_TCLK high/low	RGMII, Internal Delay Enabled, 10/100 Mbps	1.2		ns

(1) For RGMII, transmit selected signals include: MSS_RGMII_TXD[3:0] and MSS_RGMII_TCTL.



A. TXC is delayed internally before being driven to the rgmiin_txc pin. This internal delay is always enabled.

B. Data and control information is transmitted using both edges of the clocks. rgmiin_txd[3:0] carries data bits 3-0 on the rising edge of rgmiin_txc and data bits 7-4 on the falling edge of rgmiin_txc. Similarly, rgmiin_txctl carries TXEN on rising edge of rgmiin_txc and TXERR of falling edge of rgmiin_txc.

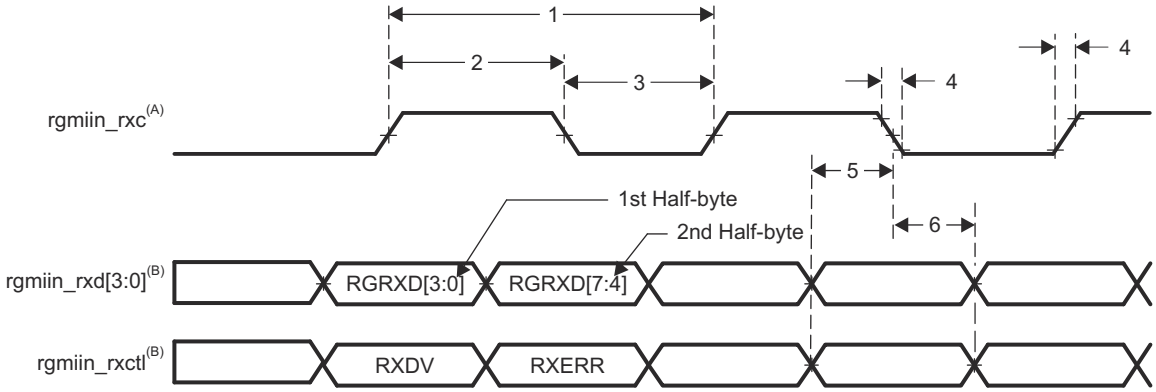
Figure 7-11. RGMII Transmit Interface Switching Characteristics

7.11.3.3.4 RGMII Recieve Clock Timing Requirements

NO.	PARAMETER	DESCRIPTION	SPEED	MIN	MAX	UNIT
1	$t_{c(RXC)}$	Cycle time, rgmiin_rxc	10 Mbps	360	440	ns
			100 Mbps	36	44	ns
2	$t_{w(RXCH)}$	Pulse duration, rgmiin_rxc high	10 Mbps	160	240	ns
			100 Mbps	16	24	ns
3	$t_{w(RXCL)}$	Pulse duration, rgmiin_rxc low	10 Mbps	160	240	ns
			100 Mbps	16	24	ns
4	$t_{t(RXC)}$	Transition time, rgmiin_rxc	10 Mbps		0.75	ns
			100 Mbps		0.75	ns

7.11.3.3.5 RGMII Recieve Data and Control Timing Requirements

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
5	$t_{su(RXD-RXCH)}$	Setup time, receive selected signals valid before MSS_RGMII_RCLK high/low	2		ns
6	$t_{h(RXCH-RXD)}$	Hold time, receive selected signals valid after MSS_RGMII_RCLK high/low	2		ns



A. rgmiin_rxc must be externally delayed relative to the data and control pins.

B. Data and control information is received using both edges of the clocks. MSS_RGMII_RXD[3:0] carries data bits 3-0 on the rising edge of rgmiin_rxc and data bits 7-4 on the falling edge ofrgmiin_rxc. Similarly, rgmiin_rxctl carries RXDV on rising edge of rgmiin_rxc and RXERR on falling edge of rgmiin_rxc.

Figure 7-12. GMAC Receive Interface Timing, RGMIIn operation

7.11.3.3.6 RMII Transmit Clock Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
RMII7	$t_{c(REF\_CLK)}$	Cycle time, REF_CLK	20		ns
RMII8	$t_{w(REF\_CLKH)}$	Pulse duration, REF_CLK high	7	13	ns
RMII9	$t_{w(REF\_CLKL)}$	Pulse duration, REF_CLK low	7	13	ns
RMII10	$t_{t(REF\_CLK)}$	Transistion time, REF_CLK		3	ns

7.11.3.3.7 RMII Transmit Data and Control Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
RMII11	$t_{d(REF\_CLK-TXD)}$	Delay time, REF_CLK high to selected transmit signals valid	2	14.2	ns
	$t_{dd(REF\_CLK-TXEN)}$				

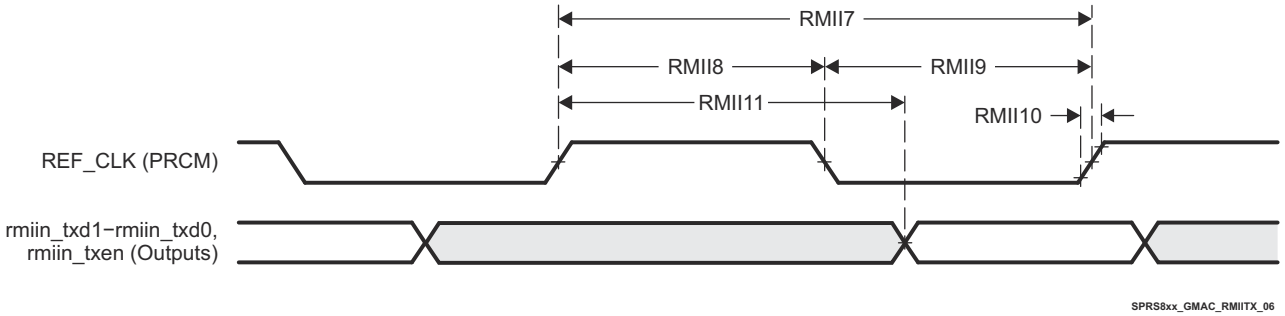


Figure 7-13. GMAC Transmit Interface Timing RMIIn Operation

7.11.3.3.8 RMII Receive Clock Timing Requirements

NO.			MIN	MAX	UNIT
RMII1	$t_{c(REF\_CLK)}$	Cycle time, REF_CLK	20		ns
RMII2	$t_{w(REF\_CLKH)}$	Pulse duration, REF_CLK high	7	13	ns
RMII3	$t_{w(REF\_CLKL)}$	Pulse duration, REF_CLK low	7	13	ns
RMII4	$t_{tt(REF\_CLK)}$	Transistion time, REF_CLK		3	ns

7.11.3.3.9 RMII Receive Data and Control Timing Requirements

NO.			MIN	MAX	UNIT
RMII5	$t_{su(RXD-REF\_CLK)}$	Setup time, receive selected signals valid before REF_CLK	4		ns
	$t_{su(CRS\_DV-REF\_CLK)}$				
	$t_{su(RX\_ER-REF\_CLK)}$				
RMII6	$t_{h(REF\_CLK-RXD)}$	Hold time, receive selected signals valid after REF_CLK	2		ns
	$t_{h(REF\_CLK-CRS\_DV)}$				
	$t_{h(REF\_CLK-RX\_ER)}$				

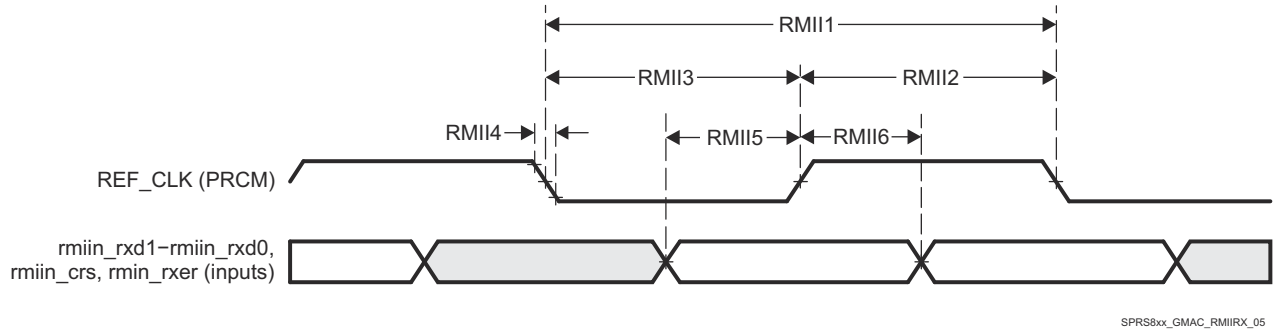


Figure 7-14. GMAC Receive Interface Timing RMIIn operation

7.11.3.3.10 MII Transmit Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
1	$t_{d(TX\_CLK-TXD)}$	Delay time, miin_txclk to transmit selected signals valid	0	25	ns
	$t_{d(TX\_CLK-TX\_EN)}$				
	$t_{d(TX\_CLK-TX\_ER)}$				

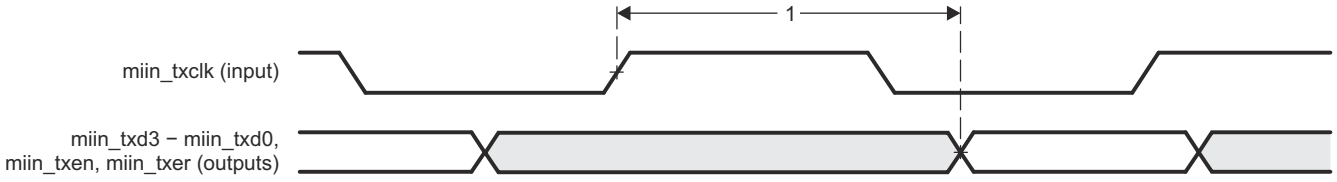


Figure 7-15. GMAC Transmit Interface Timing MIIn operation

7.11.3.3.11 MII Receive Clock Timing Requirements

NO.	PARAMETER	DESCRIPTION	SPEED	MIN	MAX	UNIT
1	$t_{c(RX\_CLK)}$	Cycle time, miin_rxclk	10 Mbps	400		ns
			100 Mbps	40		ns
2	$t_{w(RX\_CLKH)}$	Pulse duration, miin_rxclk high	10 Mbps	140	260	ns
			100 Mbps	14	26	ns
3	$t_{w(RX\_CLKL)}$	Pulse duration, miin_rxclk low	10 Mbps	140	260	ns
			100 Mbps	14	26	ns
4	$t_{t(RX\_CLK)}$	Transition time, miin_rxclk	10 Mbps		3	ns
			100 Mbps		3	ns

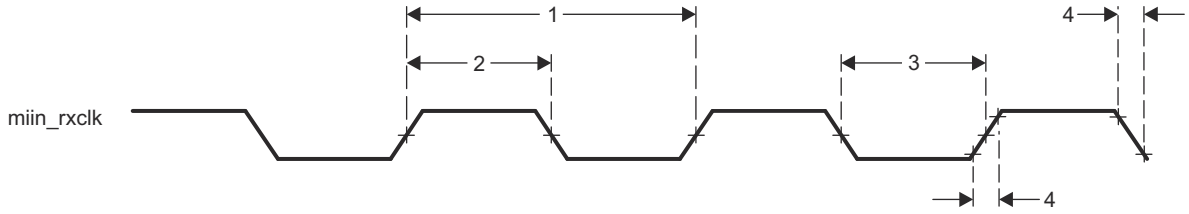


Figure 7-16. Clock Timing (GMAC Receive) - MIIn operation

7.11.3.3.12 MII Receive Timing Requirements

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
1	$t_{su(RXD-RX\_CLK)}$	Setup time, receive selected signals valid before miin_rxclk	8		ns
	$t_{su(RX\_DV-RX\_CLK)}$				
	$t_{su(RX\_ER-RX\_CLK)}$				
2	$t_{h(RX\_CLK-RXD)}$	Hold time, receive selected signals valid after miin_rxclk	8		ns
	$t_{h(RX\_CLK-RX\_DV)}$				
	$t_{h(RX\_CLK-RX\_ER)}$				

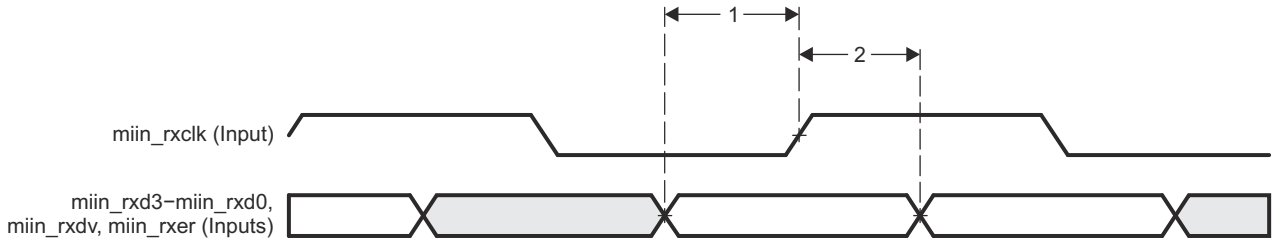


Figure 7-17. GMAC Receive Interface Timing MIIn operation

7.11.3.3.13 MII Transmit Clock Timing Requirements

NO.	PARAMETER	DESCRIPTION	SPEED	MIN	MAX	UNIT
1	$t_{c(TX\_CLK)}$	Cycle time, miin_txclk	10 Mbps	400		ns
			100 Mbps	40		ns
2	$t_{w(TX\_CLKH)}$	Pulse duration, miin_txclk high	10 Mbps	140	260	ns
			100 Mbps	14	26	ns
3	$t_{w(TX\_CLKL)}$	Pulse duration, miin_txclk low	10 Mbps	140	260	ns
			100 Mbps	14	26	ns
4	$t_{t(TX\_CLK)}$	Transition time, miin_txclk	10 Mbps		3	ns
			100 Mbps		3	ns

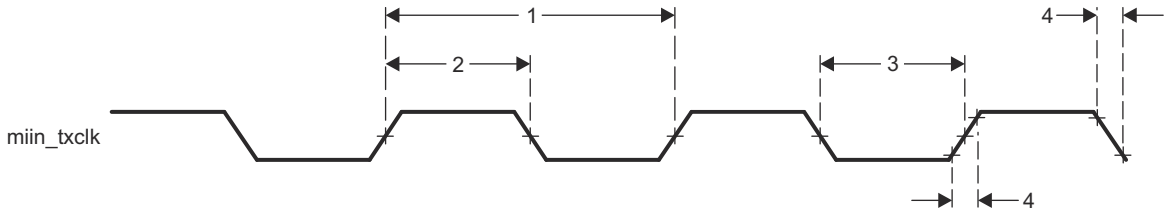


Figure 7-18. Clock Timing (GMAC Transmit) - MIIn operation

7.11.3.3.14 MDIO Interface Timings

CAUTION

The IO Timings provided in this section are only valid for some GMAC usage modes when the corresponding Virtual IO Timings or Manual IO Timings are configured as described in the tables found in this section.

Table 7-18, Table 7-19 and Figure 7-19 present switching characteristics and timing requirements for the MDIO interface.

Table 7-18. Timing Requirements for MDIO Input

No	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
MDIO1	$t_{c(MDC)}$	Cycle time, MDC	400		ns
MDIO2	$t_{w(MDCH)}$	Pulse Duration, MDC High	160		ns
MDIO3	$t_{w(MDCL)}$	Pulse Duration, MDC Low	160		ns
MDIO4	$t_{su(MDIO-MDC)}$	Setup time, MDIO valid before MDC High	90		ns
MDIO5	$t_{h(MDIO\_MDC)}$	Hold time, MDIO valid from MDC High	0		ns

Table 7-19. Switching Characteristics Over Recommended Operating Conditions for MDIO Output

NO	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
MDIO6	$t_{t(MDC)}$	Transition time, MDC		5	ns
MDIO7	$t_{d(MDC-MDIO)}$	Delay time, MDC low to MDIO valid	10	(P * 0.5) - 10	ns

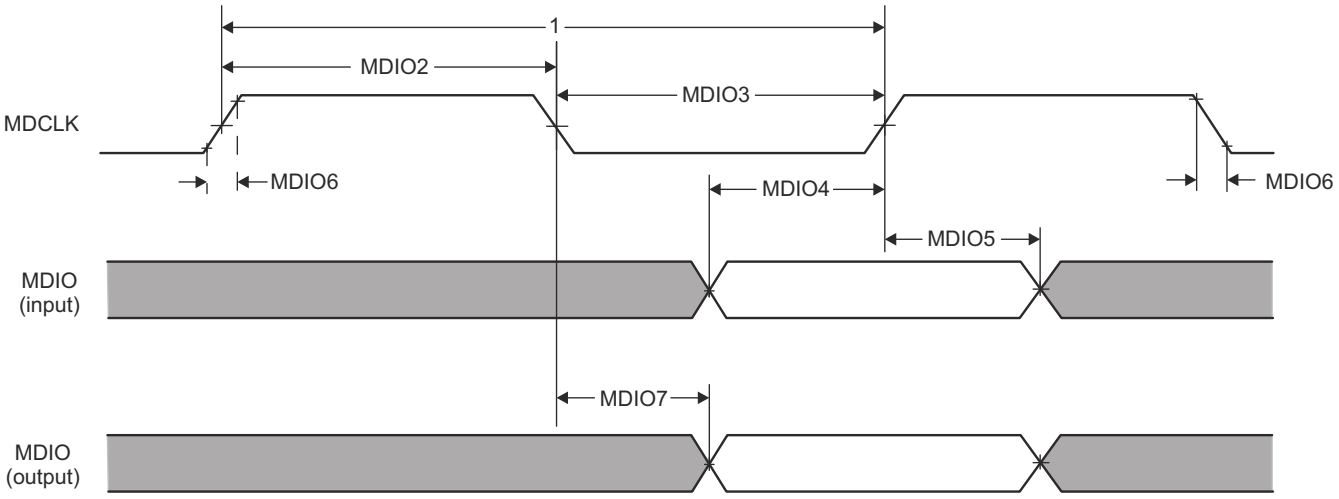


Figure 7-19. GMAC MDIO diagrams

7.11.3.4 LVDS/Aurora Instrumentation and Measurement Peripheral

The AM273x supports a set of LVDS STM-TWP Aurora interface for exporting raw IF ADC sensor data. The LVDS transmitters are shared between the two measurement interface options.

- 4-data lane LVDS interface (two additional lanes for Data Clock and Frame Clock) at 1 Gbps/lane
- 6-lane STM-TWP-Aurora-LVDS interface mode

Please see the AM273x TRM for information regarding programming options for both LVDS interfaces.

7.11.3.4.1 LVDS Interface Configuration

The supported AM273x LVDS lane configuration is four Data lanes (LVDS_TXP/M), one Bit Clock lane (LVDS_CLKP/M) and one Frame clock lane (LVDS_FRCLKP/M). The LVDS interface supports the following data rates:

- 900 Mbps (450 MHz DDR Clock)
- 600 Mbps (300 MHz DDR Clock)
- 450 Mbps (225 MHz DDR Clock)
- 400 Mbps (200 MHz DDR Clock)
- 300 Mbps (150 MHz DDR Clock)
- 225 Mbps (112.5 MHz DDR Clock)
- 150 Mbps (75 MHz DDR Clock)

Note that the bit clock is in DDR format and hence the numbers of toggles in the clock is equivalent to data.

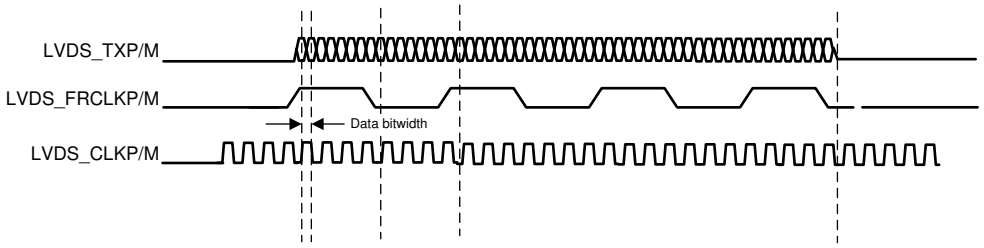


Figure 7-20. LVDS Interface Lane Configuration And Relative Timings

7.11.3.4.2 LVDS Interface Timings

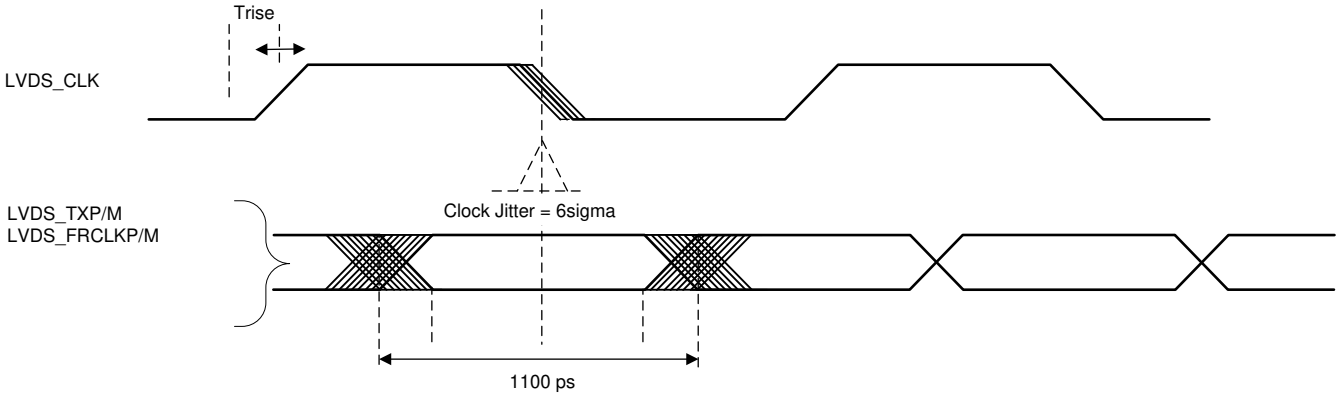


Figure 7-21. Timing Parameters

Table 7-20. LVDS Electrical Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Duty Cycle Requirements	max 1 pF lumped capacitive load on LVDS lanes	48%		52%	
Output Differential Voltage	peak-to-peak single-ended with 100 Ω resistive load between differential pairs	250		450	mV
Output Offset Voltage		1125		1275	mV
Trise and Tfall	20%-80%, 900 Mbps				ps
Jitter (pk-pk)	900 Mbps		80		ps

7.11.3.5 UART Peripheral

AM273x includes four UART interfaces. One UART is intended as a secondary boot loader source, one is intended for use as a register debug interface (with XDS110 class emulator) and two are meant for general UART communication support.

- Maximum baud-rate supported shall be at least 1536Kbaud in all the different clock frequency modes
- UART interfaces multiplexed with other I/O to allow for widest peripheral use flexibility

7.11.3.5.1 UART Timing Requirements

		MIN	TYP	MAX	UNIT
f(baud)	Supported baud rate at 20 pF		921.6		kHz

7.11.3.6 I^2C Protocol Definition

AM273x supports three master or slave Inter-integrated Circuit interfaces (I2C). One I2C interface is intended to be connected to an external PMIC or EEPROM device (alternatively controlled by SPI). The other two I2C are intended as alternative control for sensor devices or other external IC.

- Standard/fast mode I2C interface compliant with Philips I2C specification version 2.1
- Maximum clock rate of 100Kbps in Standard mode and 400Kbps in Fast mode

7.11.3.6.1 I2C Timing Requirements(1)

		STANDARD MODE		FAST MODE		UNIT
		MIN	MAX	MIN	MAX	
$t_{c(SCL)}$	Cycle time, SCL	10		2.5		µs
$t_{su(SCLH-SDAL)}$	Setup time, SCL high before SDA low (for a repeated START condition)	4.7		0.6		µs
$t_{h(SCLL-SDAL)}$	Hold time, SCL low after SDA low (for a START and a repeated START condition)	4		0.6		µs
$t_{w(SCLL)}$	Pulse duration, SCL low	4.7		1.3		µs
$t_{w(SCLH)}$	Pulse duration, SCL high	4		0.6		µs
$t_{su(SDA-SCLH)}$	Setup time, SDA valid before SCL high	250		100		µs
$t_{h(SCLL-SDA)}$(1)	Hold time, SDA valid after SCL low	0	3.45	0	0.9	µs
$t_{w(SDAH)}$	Pulse duration, SDA high between STOP and START conditions	4.7		1.3		µs
$t_{su(SCLH-SDAH)}$	Setup time, SCL high before SDA high (for STOP condition)	4		0.6		µs
$t_{w(SP)}$	Pulse duration, spike (must be suppressed)			0	50	ns
C_b (2) (3)	Capacitive load for each bus line		400		400	pF

(1) The I2C pins SDA and SCL do not feature fail-safe I/O buffers. These pins could potentially draw current when the device is powered down.
(2) The maximum th(SDA-SCLL) for I2C bus devices has only to be met if the device does not stretch the low period (tw(SCLL)) of the SCL signal.
(3) C_b = total capacitance of one bus line in pF. If mixed with fast-mode devices, faster fall-times are allowed.

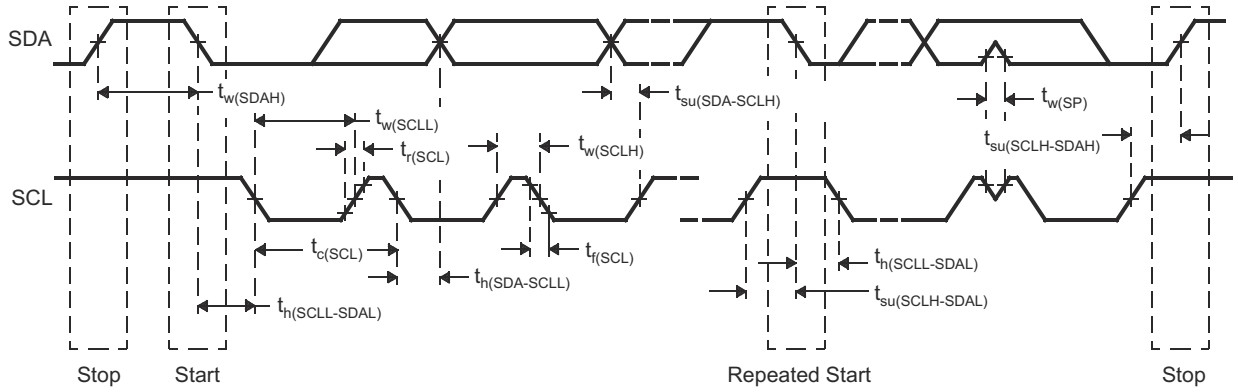


Figure 7-22. I2C Timing Diagram

Note

- A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the VIHmin of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- The maximum th(SDA-SCLL) has only to be met if the device does not stretch the LOW period (tw(SCLL)) of the SCL signal. E.A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement $t_{su(SDA-SCLH)} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line tr max + $t_{su(SDA-SCLH)}$.

7.11.3.7 Controller Area Network - Flexible Data-Rate (CAN-FD)

The AM273x integrates two CAN-FD interfaces, MSS_MCANA and MSS_MCANB. This enables support of a typical use case where one CAN-FD interface is used as ECU network interface while the other interface is used as a local network interface, providing communication with the neighboring sensors.

- Support CAN-FD according to ISO 11898-7 protocol with data rate up to 8Mbps
- Multiplexed GPIO can be used for CAN-FD external driver control
- Synchronous trigger output allows CAN-FD to trigger CSI2 data frames

7.11.3.7.1 Dynamic Characteristics for the CAN-FD TX and RX Pins

PARAMETER[1]		MIN	TYP	MAX	UNIT
$t_{d(MSS\_CANA\_TX)}$	Delay time, transmit shift register to MSS_CANA_TX pin			15	ns
$t_{d(MSS\_CANB\_TX)}$	Delay time, transmit shift register to MSS_CANB_TX pin			15	ns
$t_{d(MSS\_MCANA\_RX)}$	Delay time, MSS_MCANA_RX pin to receive shift register			10	ns
$t_{d(MSS\_MCANB\_RX)}$	Delay time, MSS_MCANB_RX pin to receive shift register			10	ns

(1) These values do not include rise/fall times of the output buffer.

7.11.3.8 CSI-2 Peripheral

AM273x integrates two, 4-lane MIPI CSI-2, D-PHY receiver peripherals: CSI2 receiver 0 (CSI2_RX0) and CSI2 receiver 1 (CSI2_RX1). Each peripheral can be used for capturing sensor data samples. The CSI2 interface is also capable of operating as a hardware-in-the-loop (HIL) interface, allowing for the playback of recorded data for development or diagnostic purposes.

- Interface is compliant with the MIPI CSI-2 D-PHY standard revision 1.2
- 2, 4-lane CSI2 receiver interfaces, working simultaneously at 600 Mbps/lane
- 4-lane, 3-lane, 2-lane, or 1-lane CSI2 configurations
- Support for virtual channels (minimum 4) and data types (minimum 4)
- Support for 8/10/12/14/16-bit RAW data mode with capability of sign extension or zero padding to align with 16-bit memory addressing for RAW 10/12/14 modes
- Support for user defined data types

Please reference the MIPI CSI-2 D-PHY standard revision 1.2 for full receiver timing requirements. Please reference the AM273x TRM for a complete description of all programmable options.

7.11.3.9 General Purpose ADC (GPADC)

AM273x device implements a GPADC module for safety monitoring device and system analog signals such as temperature sensor and voltage regulators.

- Up to 9 external or internal channels supported
- 7.5 ENOB, 625Ksps ADC
- Full-scale range of GPADC input between VSS and 1.8V
- Single or continuous conversion modes
- Data RAM to store the conversion results (1Kbyte results)

7.11.3.10 Enhanced Pulse-Width Modulator (ePWM)

AM273x includes three Enhanced Pulse-Width Modulation (ePWM) modules. These modules can be used to generate duty-cycled controlled waveforms for a power regulator, or a power management systems, or more complex waveforms for motor control applications.

- Dedicated 16-bit time-base counter with period and frequency control for each PWM module
- Each module contains two PWM outputs (EPWMxA and EPWMxB) that shall be usable in the following configurations:
  - Two independent PWM outputs with single-edge operation
  - Two independent PWM outputs with dual-edge symmetric operation
  - One independent PWM output with dual-edge asymmetric operation

7.11.3.11 Enhanced Capture (eCAP)

AM273x device includes one enhanced capture (eCAP) module. The eCAP module is used to capture external timing events. It is a general-purpose module which has a complementary function to ePWM. Uses include speed measurements of rotating machinery (e.g., toothed sprockets sensed via Hall sensors)

- Elapsed time measurements between position sensor pulses
- Period and duty cycle measurements of pulse train signals
- Decoding current or voltage amplitude derviced from duty cycle encoded current/voltage sensor
- eCAP shall be working on operating clock of minimum 100mHz
- 4-event time-stamp registers (each 32 bits)

7.11.3.12 General-Purpose Input/Output

Section 7.11.3.12.1 lists the switching characteristics of output timing relative to load capacitance.

7.11.3.12.1 Switching Characteristics for Output Timing versus Load Capacitance (C_L)(1) (2)

PARAMETER		TEST CONDITIONS		VIOIN = 1.8V	VIOIN = 3.3V	UNIT
t_r	Max rise time	Slew control = 0	C_L = 20 pF	2.8	3.0	ns
			C_L = 50 pF	6.4	6.9	
			C_L = 75 pF	9.4	10.2	
t_f	Max fall time		C_L = 20 pF	2.8	2.8	ns
			C_L = 50 pF	6.4	6.6	
			C_L = 75 pF	9.4	9.8	
t_r	Max rise time	Slew control = 1	C_L = 20 pF	3.3	3.3	ns
			C_L = 50 pF	6.7	7.2	
			C_L = 75 pF	9.6	10.5	
t_f	Max fall time		C_L = 20 pF	3.1	3.1	ns
			C_L = 50 pF	6.6	6.6	
			C_L = 75 pF	9.6	9.6	

(1) Slew control, which is configured by PADxx_CFG_REG, changes behavior of the output driver (faster or slower output slew rate).
(2) The rise/fall time is measured as the time taken by the signal to transition from 10% and 90% of VIOIN voltage.

7.11.4 Emulation and Debug

7.11.4.1 Emulation and Debug Description

7.11.4.2 JTAG Interface

The JTAG interface implements the IEEE1149.1 standard interface for processor debug and boundary scan testing.

Section 7.11.4.2.1 and Section 7.11.4.2.2 assume the operating conditions stated in Figure 7-23.

7.11.4.2.1 Timing Requirements for IEEE 1149.1 JTAG

Table 7-21. JTAG Timing Conditions

		MIN	TYP	MAX	UNIT
Input Conditions					
t_R	Input rise time	1		3	ns
t_F	Input fall time	1		3	ns
Output Conditions					
C_{LOAD}	Output load capacitance	2		15	pF

Table 7-22. JTAG Timing Requirements

NO.			MIN	TYP	MAX	UNIT
1	$t_{c(TCK)}$	Cycle time TCK	66.66			ns
1a	$t_{w(TCKH)}$	Pulse duration TCK high (40% of tc)	26.67			ns
1b	$t_{w(TCKL)}$	Pulse duration TCK low (40% of tc)	26.67			ns
3	$t_{su(TDI-TCK)}$	Input setup time TDI valid to TCK high	2.5			ns

Table 7-22. JTAG Timing Requirements (continued)

NO.			MIN	TYP	MAX	UNIT
3	$t_{su(TMS-TCK)}$	Input setup time TMS valid to TCK high	2.5			ns
4	$t_{h(TCK-TDI)}$	Input hold time TDI valid from TCK high	18			ns
4	$t_{h(TCK-TMS)}$	Input hold time TMS valid from TCK high	18			ns

7.11.4.2.2 Switching Characteristics for IEEE 1149.1 JTAG

NO.	PARAMETER		MIN	TYP	MAX	UNIT
2	$t_{d(TCKL-TDOV)}$	Delay time, TCK low to TDO valid	0		25	ns

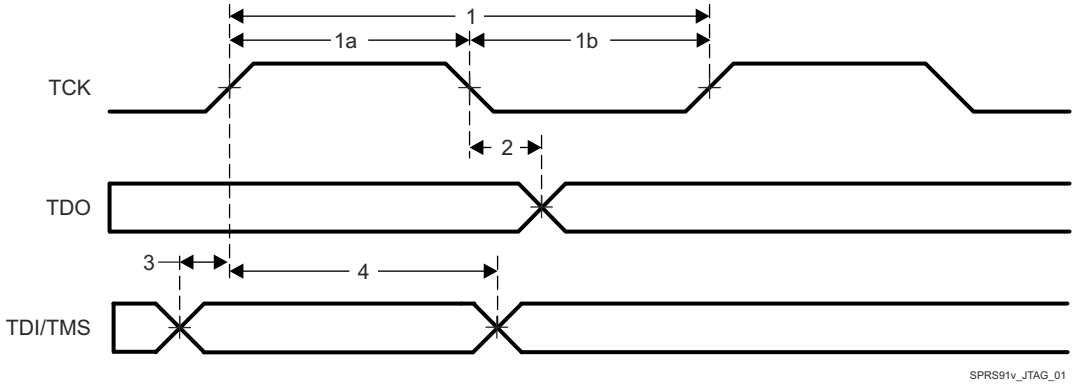


Figure 7-23. JTAG Timing

7.11.4.3 ETM Trace Interface

The ETM Trace interface provides a means of exporting real time processor debug information to a host PC through a compatible emulator toolset.

Section 7.11.4.3.1 and Section 7.11.4.3.2 describe the operating conditions shown in Figure 7-24 and Figure 7-25.

7.11.4.3.1 ETM TRACE Timing Requirements

		MIN	TYP	MAX	UNIT
Output Conditions					
C_{LOAD}	Output load capacitance	2		20	pF

7.11.4.3.2 ETM TRACE Switching Characteristics

NO.	PARAMETER		MIN	TYP	MAX	UNIT
1	$t_{cyc(ETM)}$	Cycle time, TRACECLK period	16			ns
2	$t_{h(ETM)}$	Pulse Duration, TRACECLK High	7			ns
3	$t_{l(ETM)}$	Pulse Duration, TRACECLK Low	7			ns
4	$t_{r(ETM)}$	Clock and data rise time			3.3	ns
5	$t_{f(ETM)}$	Clock and data fall time			3.3	ns
6	$t_{d(ETMTRACECLKH-ETMDATAV)}$	Delay time, ETM trace clock high to ETM data valid	1		7	ns
7	$t_{d(ETMTRACECLKl-ETMDATAV)}$	Delay time, ETM trace clock low to ETM data valid	1		7	ns

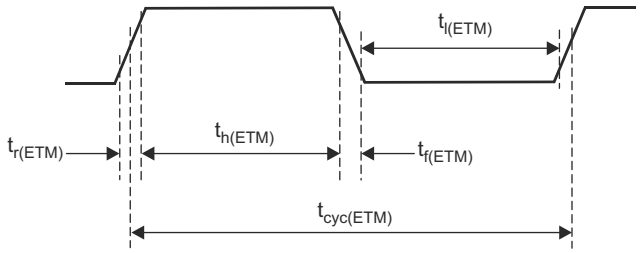


Figure 7-24. ETMTRACECLKOUT Timing

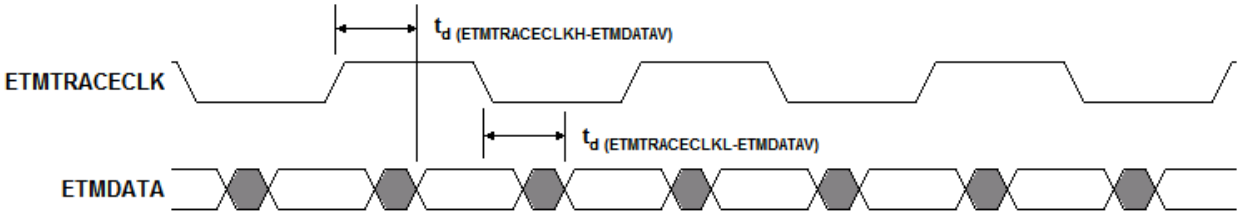


Figure 7-25. ETMDATA Timing

8 Detailed Description

8.1 Overview

The AM273x is a high performance microcontroller with an integrated C66x DSP and is ideally suited for applications needing requiring conditioning and processing functions. Two R5F cores (with optional lockstep capability) running at 400 MHz with 5MB of internal memory coupled along with a broad range of automotive and industrial connectivity peripherals and an easy to use SDK enables our customers to address a wide range of use cases in automotive and industrial markets. Functional safety and security (HSM) features are integrated to address emerging market trends.

One representative use case is for the AM273x to operate as the MCU host in an automotive radar system. In this role AM273x provides data aggregation, FFT, CFAR, range, velocity and angle estimation and tracking processing. The AM273x can operate as a host in single or dual (cascaded) front-end radar application.

As seen in Figure 3-1 the AM273x is divided into a few high level functional subsystems. Each subsystem contains specific control, signal processing, and digital communication peripherals.

- Main Subsystem (MSS): MCU Core, Cryptographic Core, Mailbox, EDMA, RTI, QSPI, SPI, CAN-FD, I2C, UART, Ethernet and GPIO
- DSP Subsystem (DSS): C66x Core, HWA2.0 Accelerator, Mailbox, EDMA, RTI
- Radar Controller Subsystem (RCSS): EDMA, CSI2A/B, SPIA/B, I2C and GPIO

Each primary subsystem is then interconnected through an ECC enabled, switch interconnect bus, allowing for EDMA transfer of data between peripherals and processing cores.

8.2 Main Subsystem

The main subsystem (MSS) is the primary controller of the device and controls all the other device subsystem cores and peripherals. The MSS contains the Cortex-R5F (MSS R5F) processor and associated peripherals and associated EDMA and Mailbox IPC functions. The MSS also controls wider system connectivity and network peripherals such as the I2C, UART, SPI, CAN-FD, EPWM, and Ethernet. The MSS is connected to the primary interconnect through the Main Subsystem (MSS) Interconnect which is ECC enabled.

The MSS contrains its own dedicated functional safety block consisting of DCC, ESM, LBIST/PBIST, CRC Watchdog Timer and GPADC for safety monitoring of critical system signals such as power supply and temperature monitors.

8.3 DSP Subsystem

The DSP subsystem (DSS) contains the TI high performance C66x DSP, HWA 2.0, and a high-bandwidth interconnect for high performance (128-bit, 150MHz), and associated data transfer peripherals: 6x EDMA for data transfer, 2x RTI and Mailbox IPC. The Aurora/LVDS measurement data output interface is also mastered by the C66x DSP. L3 shared memory is available on the DSS interconnect which is also ECC enabled.

For more information on DSP functionality, see the

8.4 Radar Control Subsystem

The radar control subsystem (RCSS) integrates a high-bandwidth interconnect with a pair of 4-lane, CSI 2.0 receivers (CSI2_RX0 and CSI2_RX1), two SPI controllers (RCSS_SPIA and RCSS_SPIB), I2C controllers and a set of GPIO. The SPI, I2C and GPIO peripherals can be utilized for controlling and configuring the attached sensor devices. The CSI 2.0 receivers allow for receiveing high-speed sensor data samples such as samples.

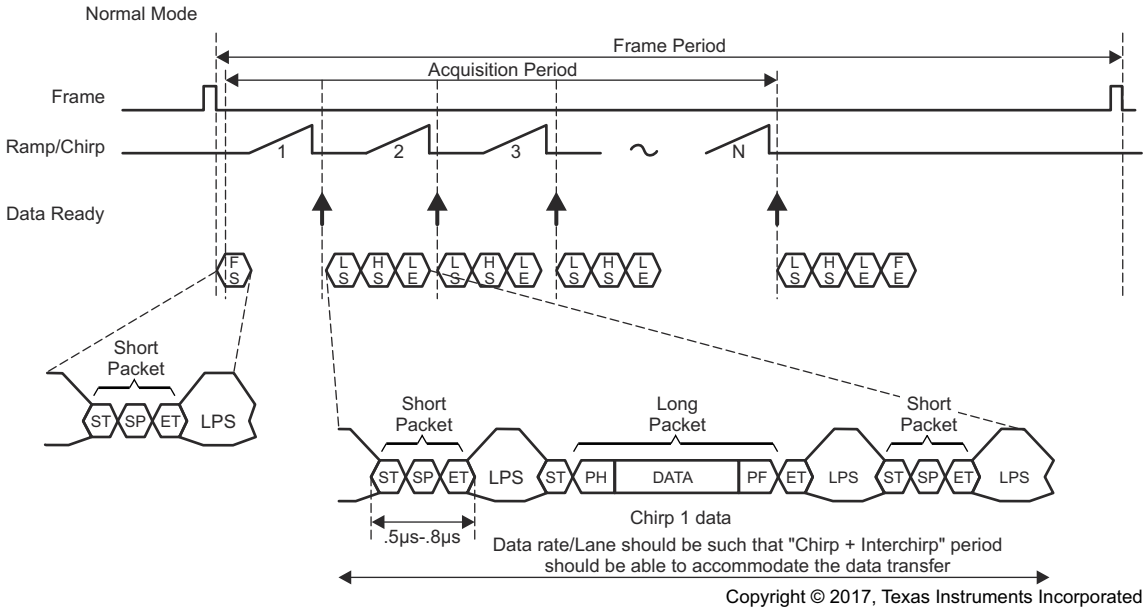
8.5 Other Subsystems

8.5.1 Radar A2D Data Format Over CSI2 Interface

The AM273x device uses MIPI D-PHY / CSI2-based format to receive the raw A2D samples from an external radar transceiver. This is shown in Figure 8-1.

- Supports four data lanes
- CSI-2 data rate scalable from 150 Mbps to 600 Mbps per lane
- Virtual channel based

- CRC generation



Frame **S**tart – CSI2 VSYNC Start Short Packet**L**ine **S**tart – CSI2 HSYNC Start Short Packet**L**ine **E**nd – CSI2 HSYNC End Short Packet**F**rame **E**nd – CSi2 VSYNC End Short Packet

Figure 8-1. CSI-2 Transmission Format

The data payload is constructed with the following three types of information:

- Chirp profile information
- The actual chirp number
- A2D data corresponding to chirps of all four channels
  - Interleaved fashion
- Chirp quality data (configurable)

The payload is then split across the four physical data lanes and transmitted to the receiving D-PHY. The data packet packing format is shown in Figure 8-2.

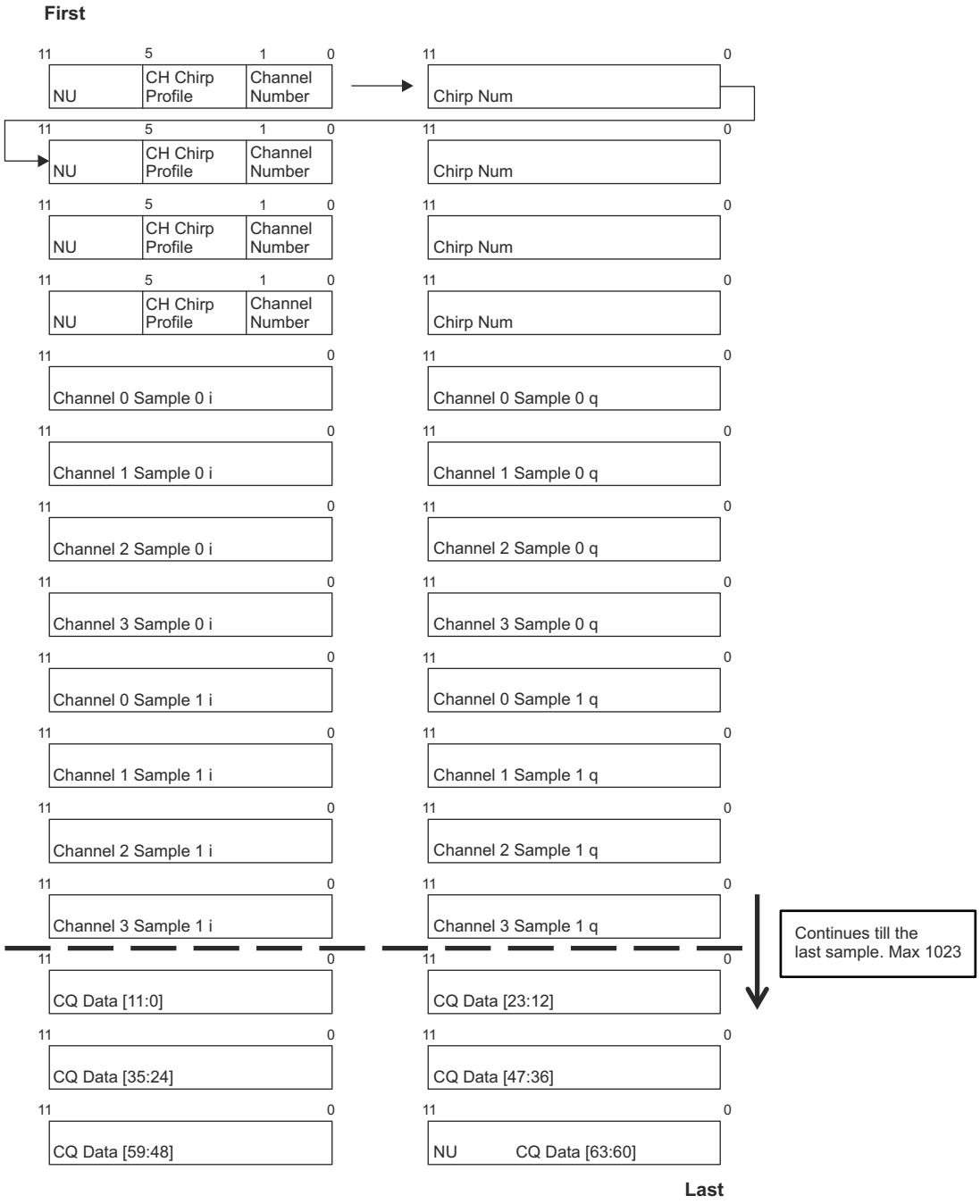


Figure 8-2. Data Packet Packing Format for 12-Bit Complex Configuration

8.5.2 ADC Channels (Service) for User Application

The AM273x device includes provision for an ADC service for user application, where the GPADC engine present inside the device can be used to measure up to nine external and internal voltages. The ADC1, ADC2, ADC3, ADC4, ADC5, ADC6, ADC7, ADC8 and ADC9 pins are used for this purpose.

Note

GPADC structures are used for measuring the output of internal temperature sensors.

GPADC Specifications:

- 625Ksps SAR ADC
- 0 to 1.8-V input range
- 10-bit resolution

Table 8-1. GPADC Parameters

PARAMETER	TYP	UNIT
ADC supply	1.8	V
ADC unbuffered input voltage range	0 – 1.8	V
ADC buffered input voltage range(1)	0.4 – 1.3	V
ADC resolution	10	bits
ADC offset error	±5	LSB
ADC gain error	±5	LSB
ADC DNL	–1/+2.5	LSB
ADC INL	±2.5	LSB
ADC sample rate	625	Ksps
ADC sampling time	400	ns
ADC internal cap	10	pF
ADC buffer input capacitance	2	pF
ADC input leakage current	3	uA

(1) Outside of given range, the buffer output will become nonlinear.

8.6 Boot Modes

AM273x bootloader functionality is controlled by a set of start on power (SOP) pins. These pins states are latched on de-assertion of the NRESET pin after power on of the device. The SOP pins are multiplexed with functional mode signals before and during NRESET de-assertion. After bootloader execution the functional mode operation is then restored. See the power on reset timing sequence for more details. The following tables describe the SOP pin operation.

Host hardware should provide a means for driving these SOP pins to their required states during NRESET de-assertion, but also allow for their functional mode operation if required by the intended application.

Table 8-2. SOP Pins

Pin	SOP Mode Signal Name	Pinlist Signal Name
D6	SOP[0]	TDO
E17	SOP[1]	MSS_MIBSPIB_CS2
F1	SOP[2]	PMIC_CLKOUT
V9	SOP[3]	MSS_UARTB_TX
W2	SOP[4]	MSS_UARTA_TX

Table 8-3. SOP Pin Modes

Boot Options	SOP Mode
Bootmode SOP Modes	• SOP[2:0] = 0b011 selects SOP_MODE2 • SOP[2:0] = 0b001 selects SOP_MODE4 • SOP[2:0] = 0b101 selects SOP_MODE5 • All other states reserved and should not be selected.
Crystal Detect SOP Modes	• SOP[4:3] = 0b00 selects 40 MHz Crystal Mode • SOP[4:3] = 0b01 selects 45.1584 MHz Crystal Mode • SOP[4:3] = 0b10 selects 49.152 MHz Crystal Mode • SOP[4:3] = 0b11 selects 50 MHz Crystal Mode

Table 8-4. Bootmode SOP Descriptions

Bootmode SOP Modes	Function	Description
SOP_MODE2	Development Mode	Development boot mode. The AM273x ROM bootloader will setup the device to wait for a JTAG debugger connection.
SOP_MODE4	Functional Mode	Functional boot mode of the AM273x device. In this mode, the ROM bootloader will attempt to load a valid secondary bootloader image from primarily the QSPI interface and secondarily the SPI host interface.
SOP_MODE5	Device Management Mode	QSPI flash programming boot mode of the AM273x device. In this mode the ROM bootloader will attempt to receive a valid QSPI secondary bootloader image over MSS_UARTA_TX/RX (pins W2, U3) and attempt to flash an attached QSPI memory with this image.

Table 8-5. Crystal Detect SOP Mode Description

Crystal Detect SOP Modes	
40 MHz Crystal Crystal Mode	ROM bootloader image expects a 40 MHz nominal crystal clock source.
45.1584 MHz Crystal Mode	ROM bootloader image expects a 45.1584 MHz nominal crystal clock source.
49.152 MHz Crystal Mode	ROM bootloader image expects a 49.152 MHz nominal crystal clock source.
50 MHz Crystal Mode	ROM bootloader image expects a 50 MHz nominal crystal clock source.

9 Applications, Implementation, and Layout

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Typical Application

9.1.1 Schematic

The below AM273x Example Schematic shows an exerpt the AM273x EVM schematic. The exerpt focuses only on the AM273x device schematic symbols to show the device pin usage.

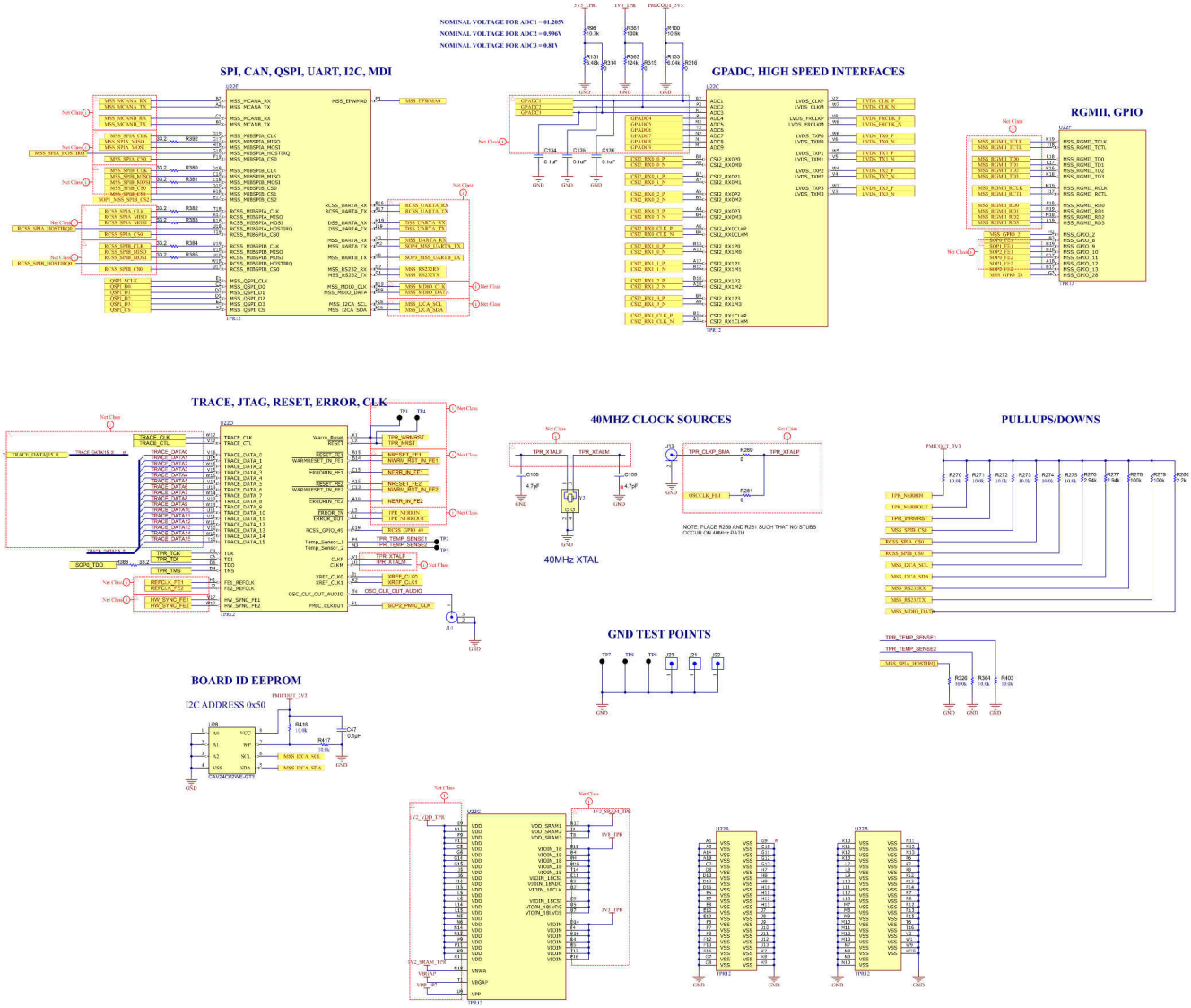


Figure 9-1. AM273x Example Schematic

9.1.2 Layout

9.1.2.1 Layout Example

The following figures are exerpts from the AM273x EVM PCB layout, assembly and layer stack-up.

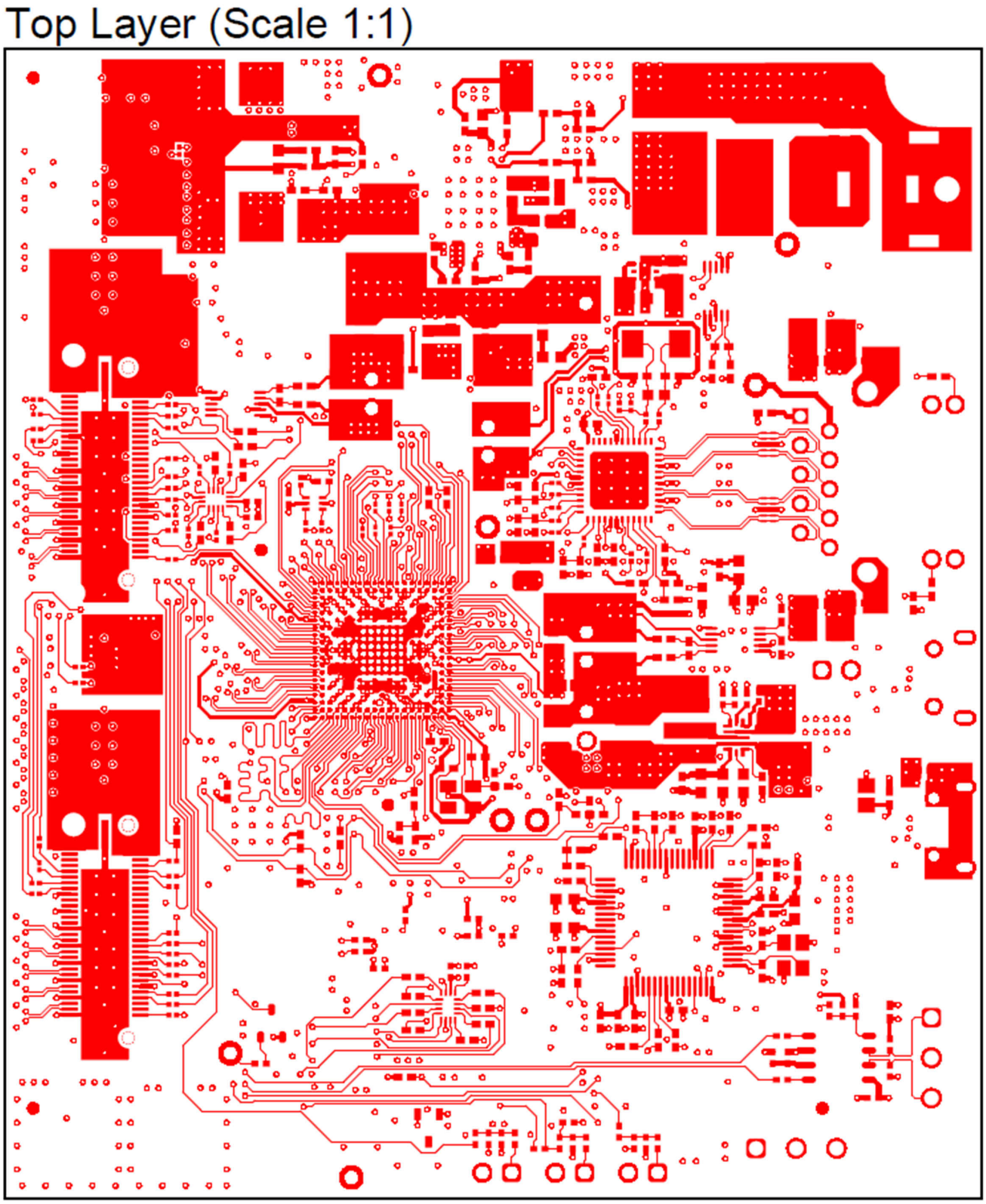


Figure 9-2. AM273x EVM - Layer 1 (Top)

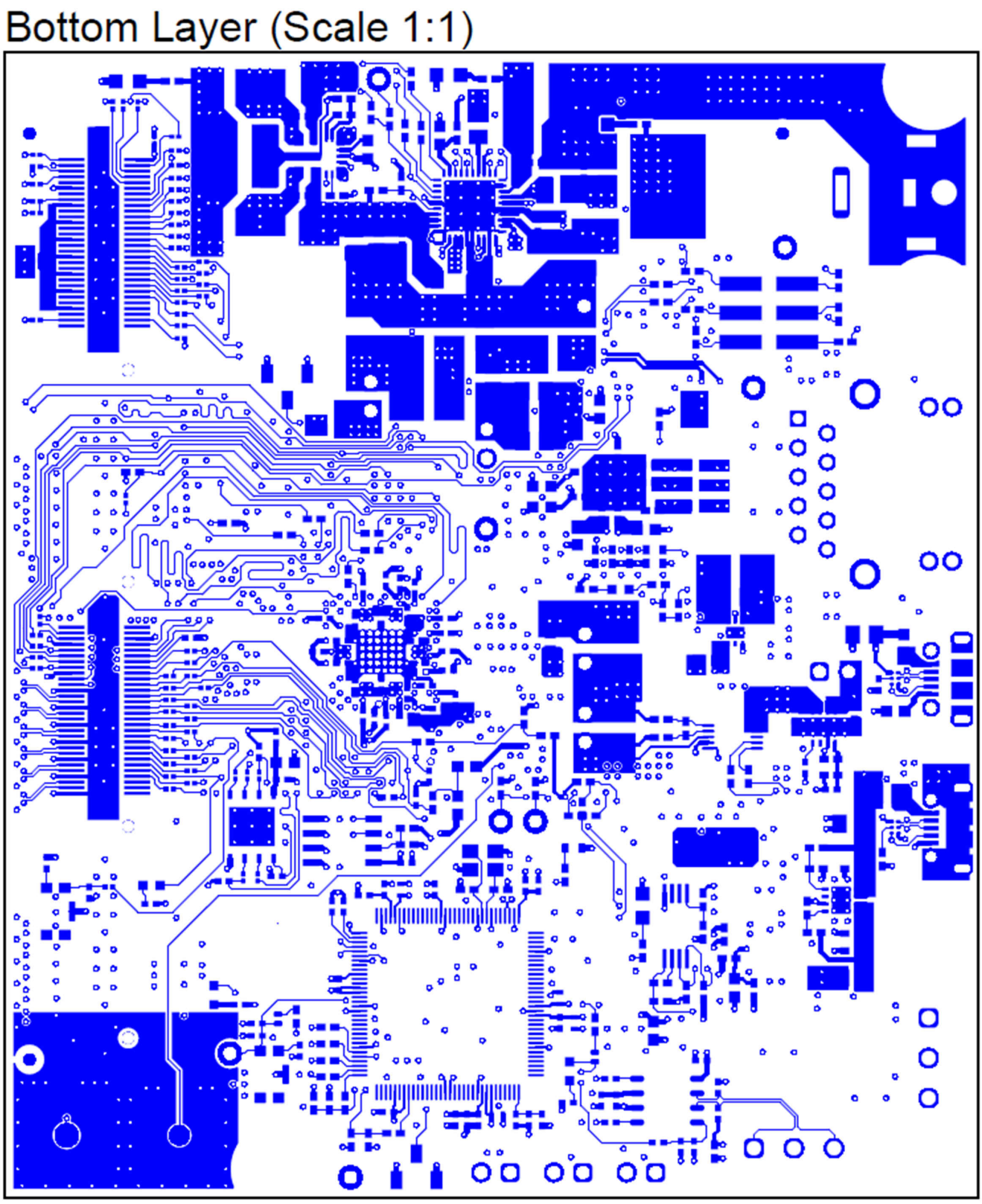


Figure 9-3. AM273x EVM - Layer 10 (Bottom)

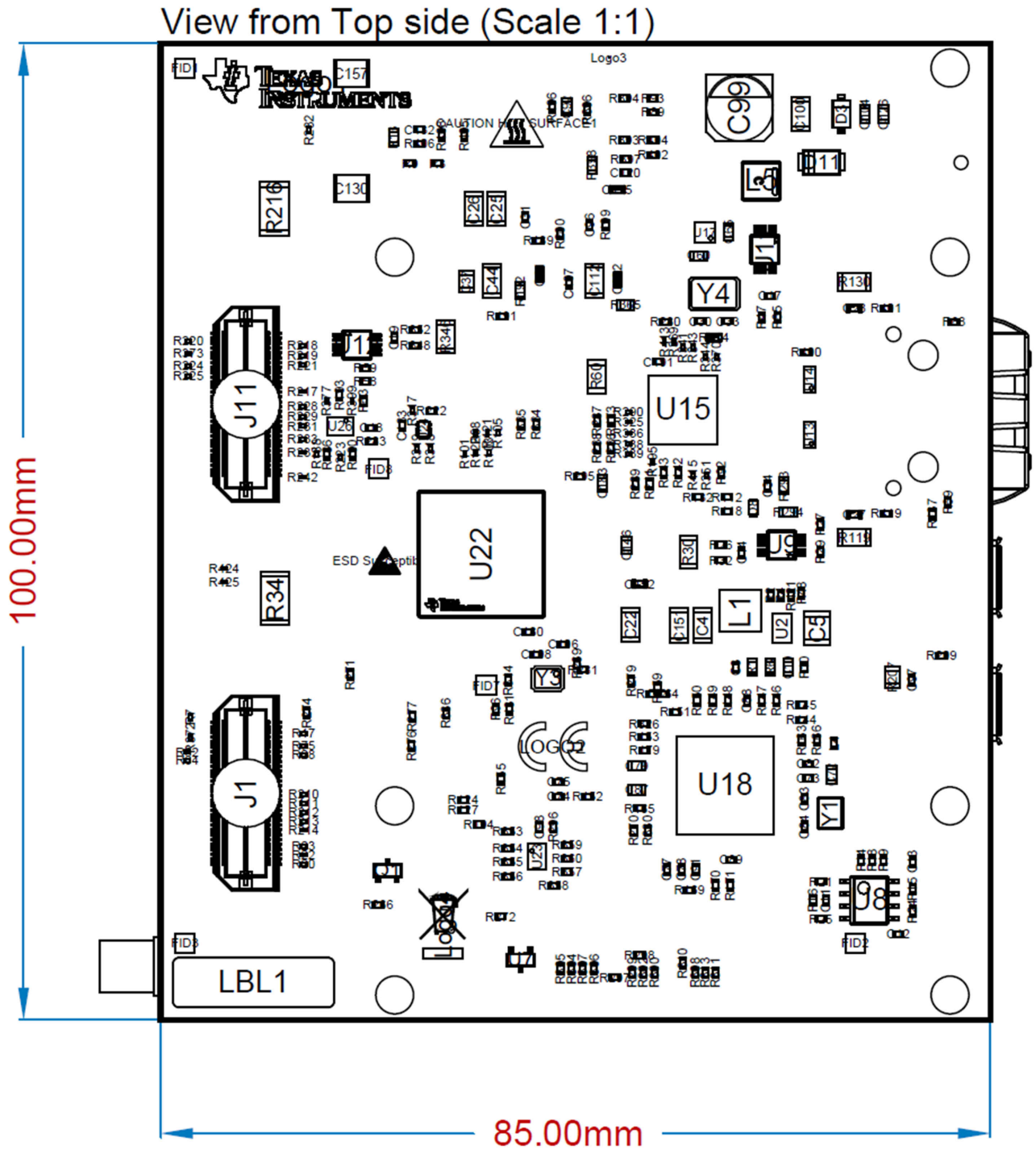


Figure 9-4. AM273x EVM - Top Assembly

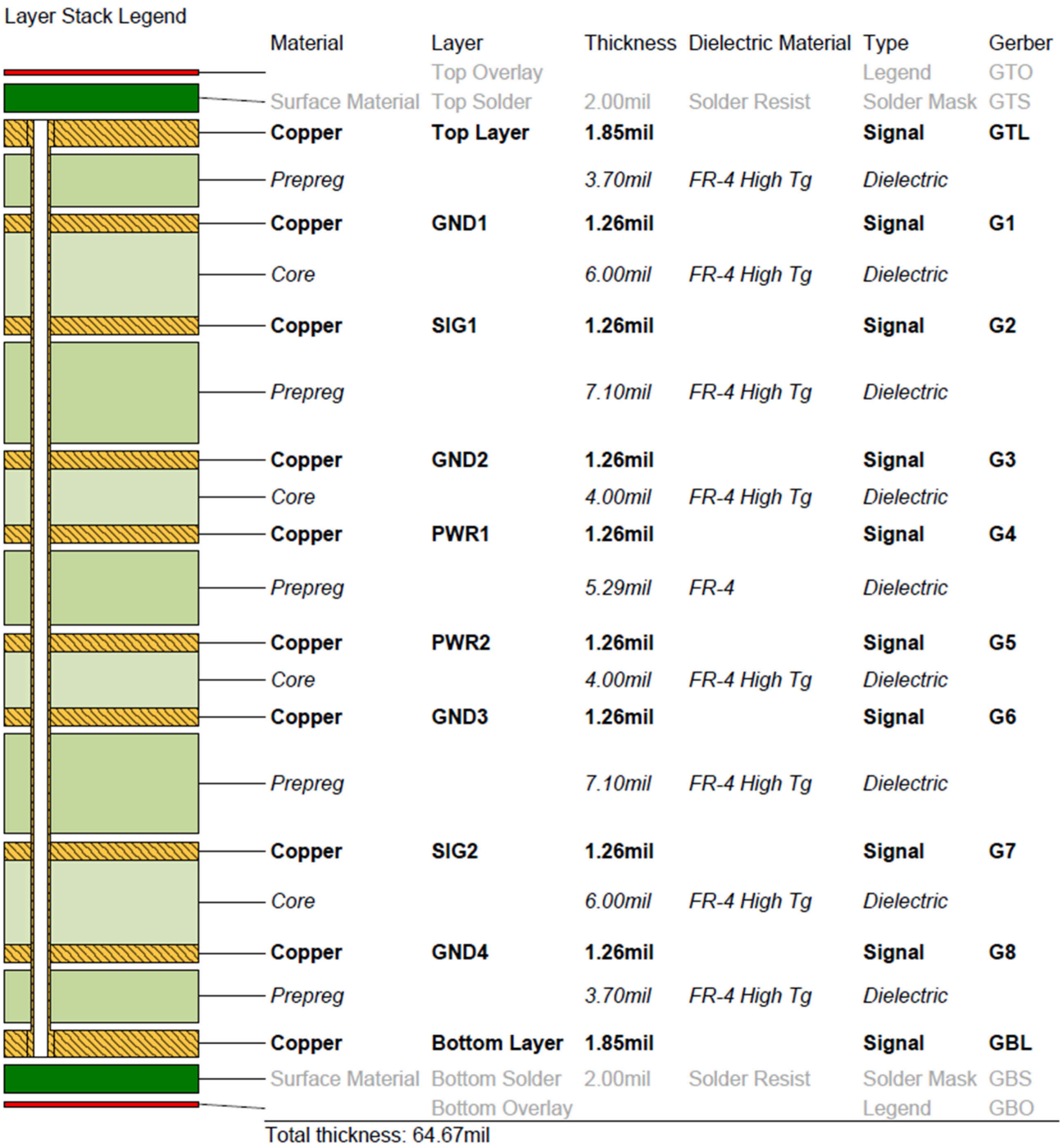


Figure 9-5. AM273x EVM - Layer Stackup

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all microcontrollers (MCU) and support tools. Each device has one of three prefixes: X, P, or null (no prefix) (for example, *AM273x*). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMDX) through fully qualified production devices and tools (TMDS).

Device development evolutionary flow:

X Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

P Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

null Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully-qualified development-support product.

X and P devices and TMDX development-support tools are shipped against the following disclaimer:

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all DSP devices and support tools. Each DSP commercial family member has one of three prefixes: TMX, TMP, or TMS (for example, *AM273x*). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX and TMDX) through fully qualified production devices and tools (TMS and TMDS).

Device development evolutionary flow:

TMX Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

TMP Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

TMS Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully-qualified development-support product.

TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, *ZCE*), the temperature range (for example, blank is the default commercial temperature range),

and the device speed range, in megahertz (for example, *400 MHz*). Table 10-1 and Figure 10-1 provides a legend for reading the complete device name for any *AM273x* device.

For orderable part numbers of *AM273x* devices in the *AM273x* package types, see the Package Option Addendum of this document, ti.com, or contact your TI sales representative.

For additional description of the device nomenclature markings on the die, see the Silicon Errata .

10.1.1 Standard Package Symbolization

Note

Some devices may have a cosmetic circular marking visible on the top of the device package which results from the production test process. In addition, some devices may also show a color variation in the package substrate which results from the substrate manufacturer. These differences are cosmetic only with no reliability impact.

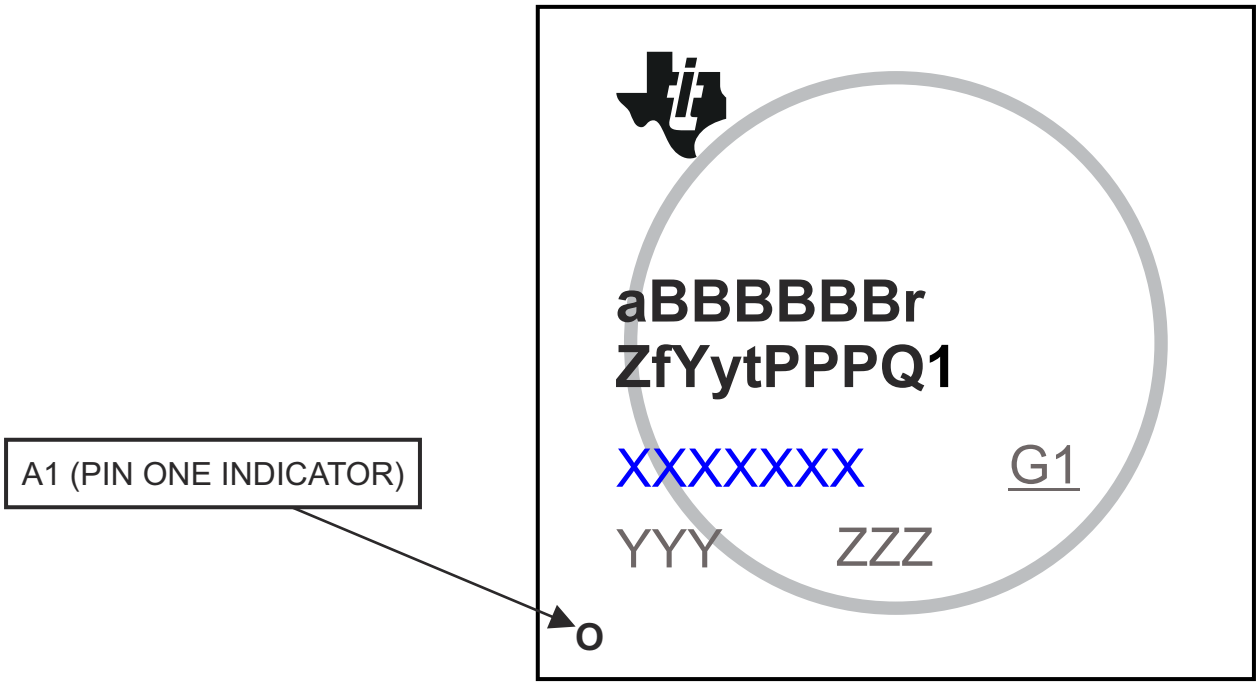


Figure 10-1. Printed Device Reference

10.1.2 Device Naming Convention

Table 10-1. Nomenclature Description

FIELD PARAMETER	FIELD DESCRIPTION	VALUE	DESCRIPTION
a(1)	Device evolution stage	X	Prototype
		P	Preproduction (production test flow, no reliability data)
		BLANK	Production
BBBBBB	Base production part number	AM2732	See Table 5-1, *Device Comparison*
r	Device revision	A	SR 1.0
Z	Device Speed and Memory Grades	D	See Table 7-3, *Speed and Memory Grade*
f	Features (see Table 5-1, *Device Comparison*)	R	General Purpose Device
		S	Programmable DSP (Single Core)
		T	DSP Blackbox
Y	Functional Safety	G	Non-Functional Safety Device
		F	Functional Safety Device
y	Security	G	Non-Secure
		1	Dummy Key Device
		M	Production Key HS Device
t(2)	Temperature (see Section 7.4, *ROC*)	A	–40°C to 105°C - Extended Industrial
		I	–40°C to 125°C - Automotive
		Q	–40°C to 140°C - Extended Automotive
PPP	Package Designator	ZCE	ZCE NFBGA-N285 (13 mm × 13 mm) Package
Q1	Automotive Designator	Q1	Auto Qualified (AEC-Q100)
		EP	Enhanced Product
XXXXXXX			Lot Trace Code (LTC)
YYY			Production Code; For TI use only
ZZZ			Production Code; For TI use only
O			Pin one designator
G1			ECAT—Green package designator

(1) To designate the stages in the product development cycle, TI assigns prefixes to the part numbers. These prefixes represent evolutionary stages of product development from engineering prototypes through fully qualified production devices.
Prototype devices are shipped against the following disclaimer:
"This product is still in development and is intended for internal evaluation purposes."
Notwithstanding any provision to the contrary, TI makes no warranty expressed, implied, or statutory, including any implied warranty of merchantability of fitness for a specific purpose, of this device.

(2) Applies to device max junction temperature.

Note

BLANK in the symbol or part number is collapsed so there are no gaps between characters.

10.2 Tools and Software

The following products support development for AM273x platforms:

Development Tools

Code Composer Studio™ Integrated Development Environment Code Composer Studio (CCS) Integrated Development Environment (IDE) is a development environment that supports TI's Microcontroller and Embedded Processors portfolio. Code Composer Studio comprises a suite of tools used to develop and debug embedded applications. It includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features. The intuitive IDE provides a single user interface taking you through each step of the application development flow. Familiar tools and interfaces allow users to get started faster than ever before. Code Composer Studio combines the advantages of the Eclipse software framework with advanced embedded debug capabilities from TI resulting in a compelling feature-rich development environment for embedded developers.

SYSCONFIG The SYSCONFIG Pin MUX Utility is a software tool which provides a Graphical User Interface for configuring pin multiplexing settings, resolving conflicts and specifying I/O cell characteristics for TI MPUs. Results are output as C header/code files that can be imported into software development kits (SDKs) or used to configure customer's custom software.

AM273x Power Estimation Tool (PET) AM273x Power Estimation Tool (PET) provides users the ability to gain insight in to the power consumption of select TI processors. The tool includes the ability for the user to choose multiple application scenarios and understand the power consumption as well as how advanced power saving techniques can be applied to further reduce overall power consumption.

For a complete listing of development-support tools for the processor platform, visit the Texas Instruments website at ti.com. For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

10.3 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The current documentation that describes the processor, related peripherals, and other technical collateral is listed below.

The following documents describe the AM273x family of devices.

Technical Reference Manual

AM273x Microntrollers Silicon Revision 1.0 Technical Reference Manual Details the integration, the environment, the functional description, and the programming models for each peripheral and subsystem in the AM273x family of devices.

Errata

AM273x Microntrollers Silicon Revision 1.0 Silicon Errata Describes the known exceptions to the functional specifications for the device.

Tip: Search TI.com using literature numbers.

10.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.5 Trademarks

Sitara™, NanoFree™, and TI E2E™ are trademarks of Texas Instruments.
Code Composer Studio™ is a trademark of TI.
Arm® and Cortex® are registered trademarks of Arm Limited.
All trademarks are the property of their respective owners.

10.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

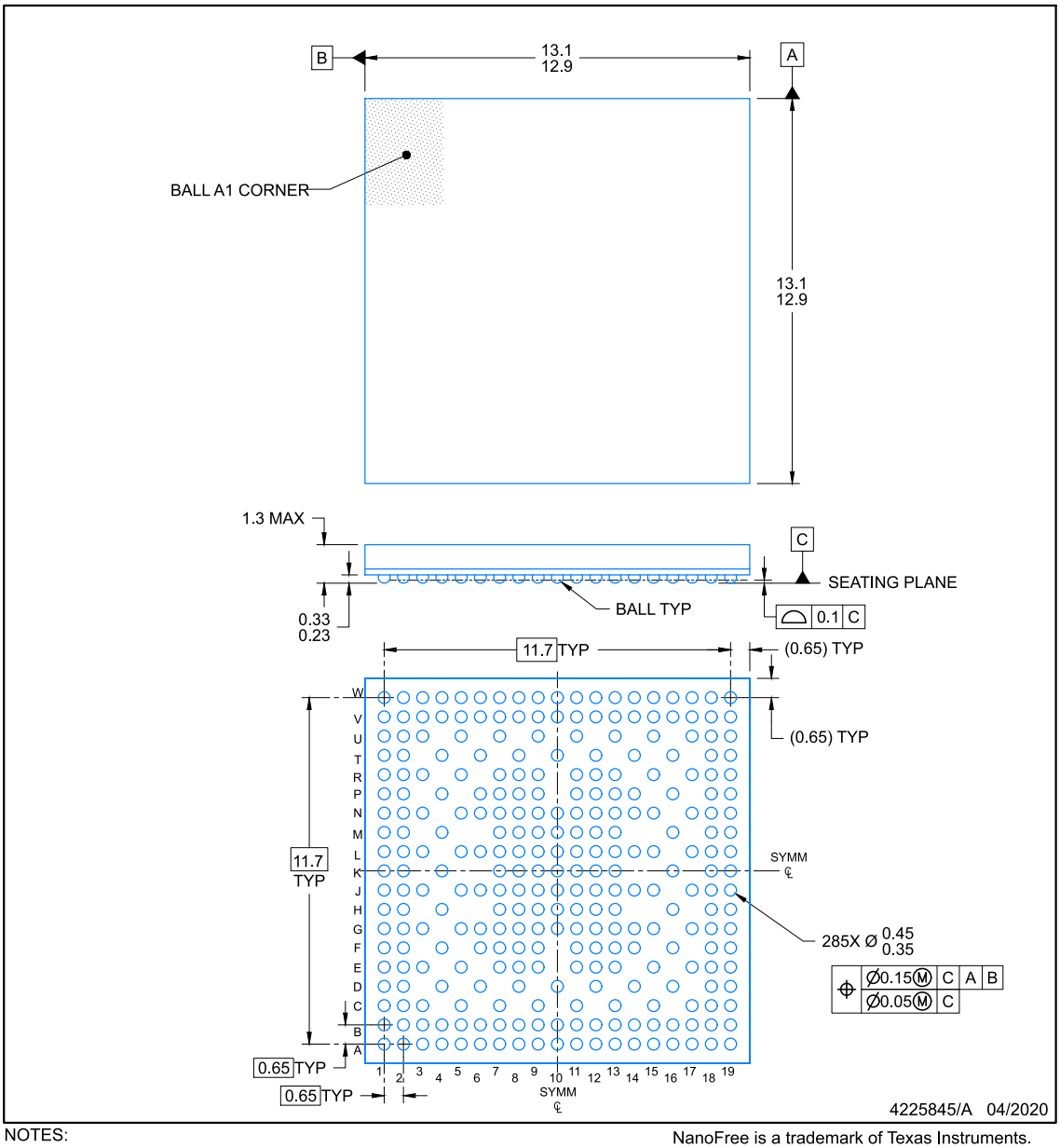
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

ZCE0285A-C01

NFBGA - 1.3 mm max height

PLASTIC BALL GRID ARRAY



NOTES:

NanoFree is a trademark of Texas Instruments.

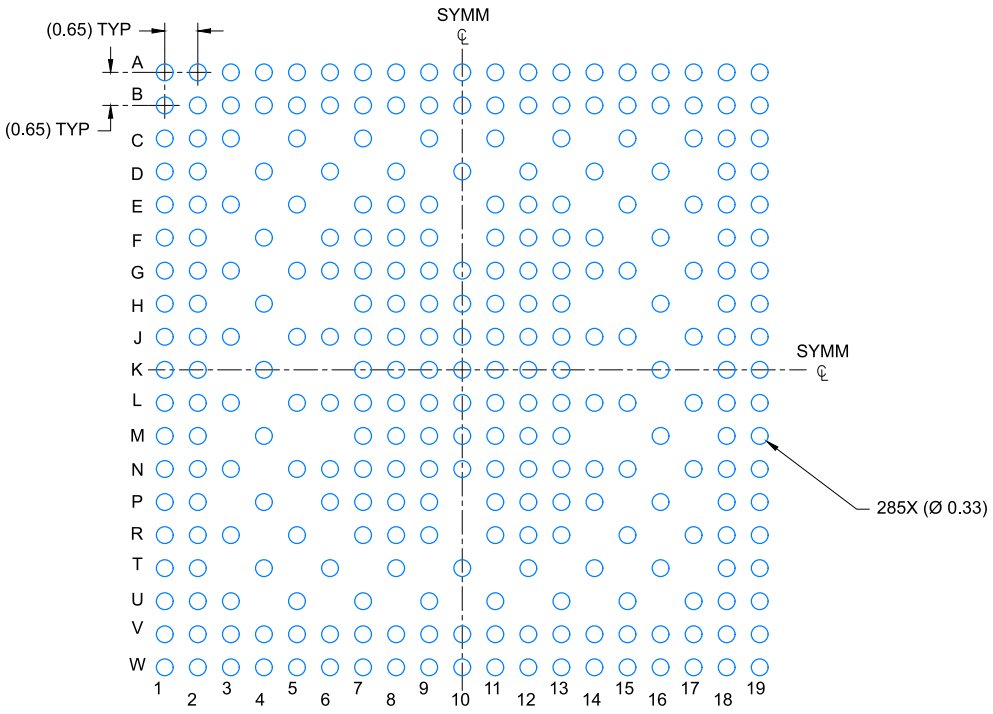
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

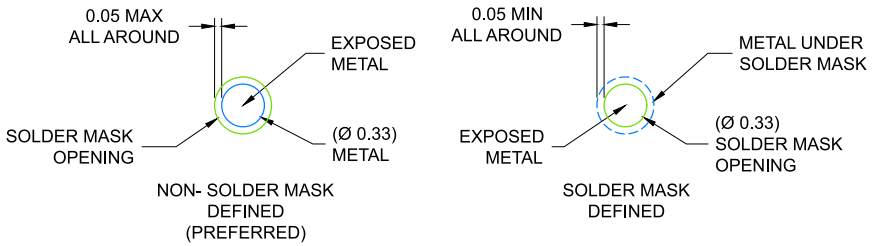
ZCE0285A-C01

NFBGA - 1.3 mm max height

PLASTIC BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE: 8X



SOLDER MASK DETAILS
NOT TO SCALE

4225845/A 04/2020

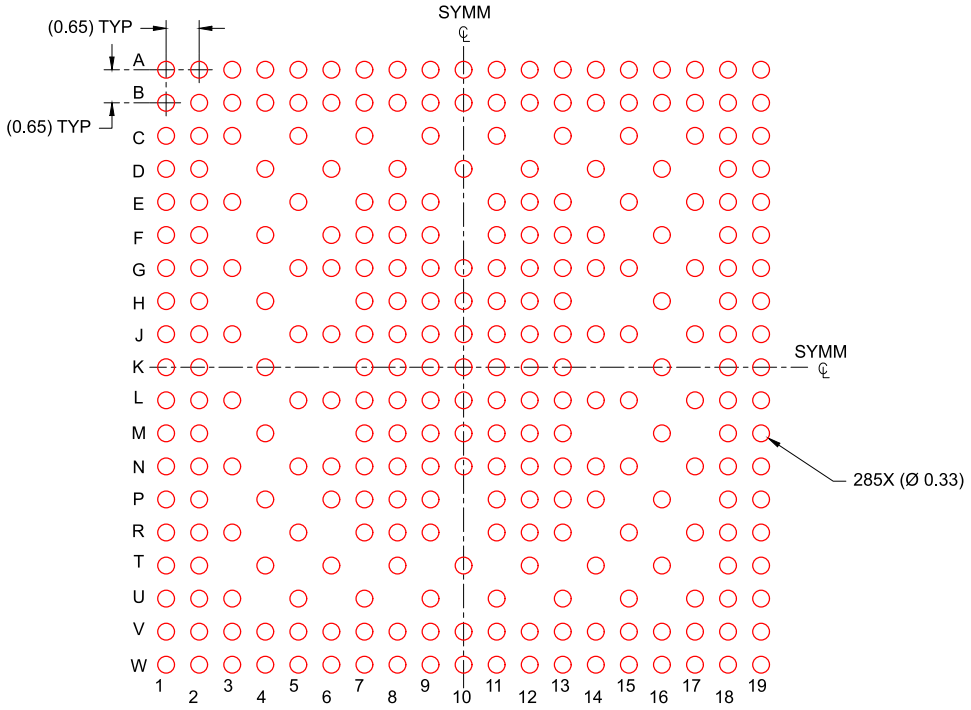
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. Refer to Texas Instruments Literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

ZCE0285A-C01 — **NFBGA - 1.3 mm max height**

PLASTIC BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

4225845/A 04/2020

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AM2732ADRFGAZCER	ACTIVE	NFBGA	ZCE	285	1000	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 105	AM2732A DRFGAZCE 711	Samples
AM2732ADRFGQZCERQ1	ACTIVE	NFBGA	ZCE	285	1000	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 140	AM2732A DRFGQZCEQ1 711	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF AM2732, AM2732-Q1 :

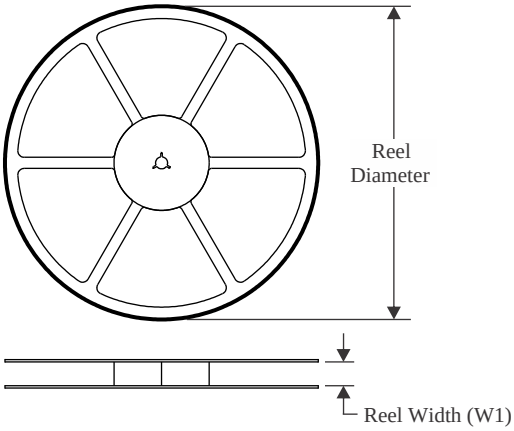
- Catalog : AM2732
- Automotive : AM2732-Q1

NOTE: Qualified Version Definitions:

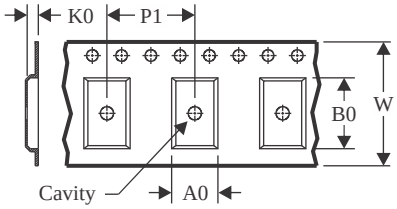
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

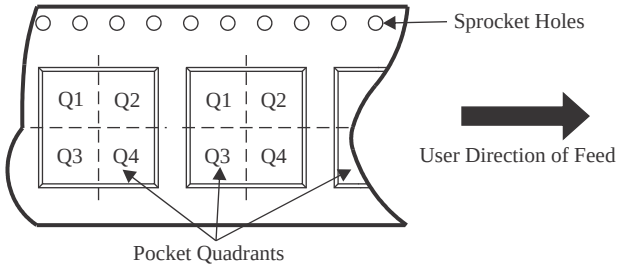


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

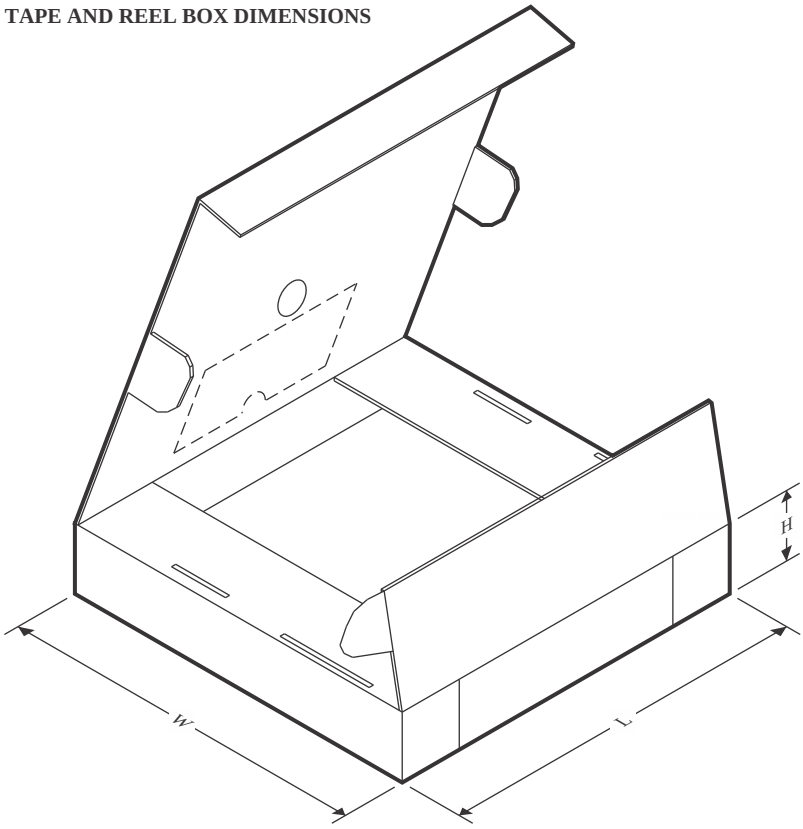
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AM2732ADRFGAZCER	NFBGA	ZCE	285	1000	330.0	24.4	13.3	13.3	2.35	16.0	24.0	Q1
AM2732ADRFGQZCERQ1	NFBGA	ZCE	285	1000	330.0	24.4	13.3	13.3	2.35	16.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AM2732ADRFGAZCER	NFBGA	ZCE	285	1000	336.6	336.6	41.3
AM2732ADRFGQZCERQ1	NFBGA	ZCE	285	1000	336.6	336.6	41.3

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