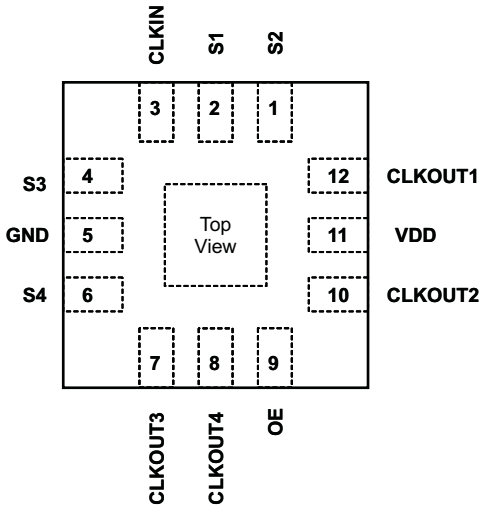
1 to 4 Configurable Clock Buffer for 3D Displays

Check for Samples: CDC1104

FEATURES

- **Input Reference Clock 120Hz–240Hz**
- **Output Clock (Fin/2) 60Hz–120Hz**
- **Output Buffer Drive Strength: 8mA**
- **4 Clock Outputs**
- **4 Control Pins Select Phases of Clock Outputs**
- **Supply Voltage: 3.8V–5.5V**
- **Operating Temperature Range: –40°C to 85°C**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-B)**
  - **500-V Charged-Device Model (C101)**
- **Package Offerings**
  - **12-pin QFN (3mm x 3mm)**

RVK PACKAGE
(TOP VIEW)



DESCRIPTION

The CDC1104 is a 1 to 4 configurable clock buffer. The device accepts an input reference clock and creates 4 buffered output clocks with an output frequency equal to one half the input clock frequency. Four control inputs, S1, S2, S3, S4 configurable phases of the clock outputs.

ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	RVK	Tape and reel	CDC1104RVKR	ZT

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

PIN FUNCTIONS

NO.	NAME	TYPE(1)	DESCRIPTION
1	S2	I	Output clock select. Refer to Output Clock Selection Table
2	S1	I	Output clock select. Refer to Output Clock Selection Table
3	CLKIN	I	Clock Input
4	S3	I	Output clock select. Refer to Output Clock Selection Table
5	GND	P	Ground
6	S4	I	Not internally connected
7	CLKOUT3	O	Buffered CLK Output. Refer to Output Clock Selection Table
8	CLKOUT4	O	Buffered CLK Output. Refer to Output Clock Selection Table
9	OE	I	Chip Enable
10	CLKOUT2	O	Buffered CLK Output. Refer to Output Clock Selection Table
11	VDD	P	Inverted output. No counter delay
12	CLKOUT1	O	Buffered CLK Output. Refer to Output Clock Selection Table

(1) G = Ground, I = Input, O = Output, P = Power

TRUTH TABLE

INPUTS						OUTPUTS			
OE	CLKIN	S4	S3	S2	S1	CLKOUT4	CLKOUT3	CLKOUT2	CLKOUT1
0	CLK	X	X	X	X	L	L	L	L
1	CLK	0	0	0	0	L	L	L	L
1	CLK	0	0	0	1	CLK\	CLK\	CLK\	CLK
1	CLK	0	0	1	0	CLK\	CLK\	CLK	CLK\
1	CLK	0	0	1	1	CLK\	CLK\	CLK	CLK
1	CLK	0	1	0	0	CLK\	CLK	CLK\	CLK\
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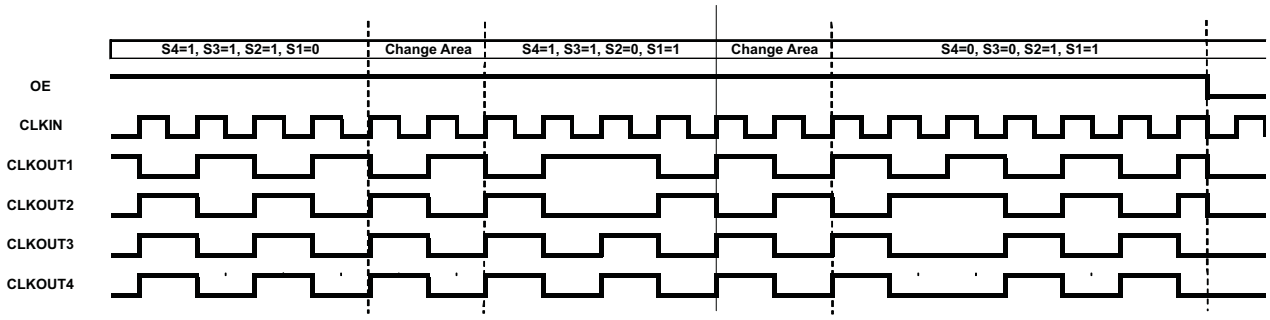
1	CLK	1	0	1	0	CLK	CLK\	CLK	CLK\
1	CLK	1	0	1	1	CLK	CLK\	CLK	CLK
1	CLK	1	1	0	0	CLK	CLK	CLK\	CLK\
1	CLK	1	1	0	1	CLK	CLK	CLK\	CLK
1	CLK	1	1	1	0	CLK	CLK	CLK	CLK\
1	CLK	1	1	1	1	CLK	CLK	CLK	CLK

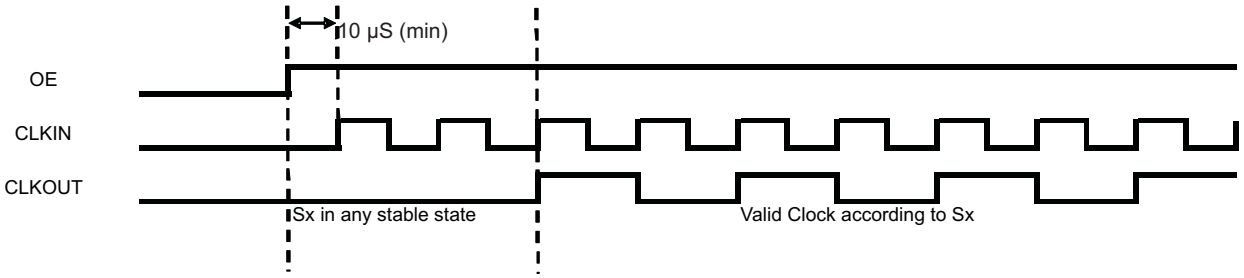
Timing Diagram For Glitch Free Operation

Transition of outputs from any state to any other state



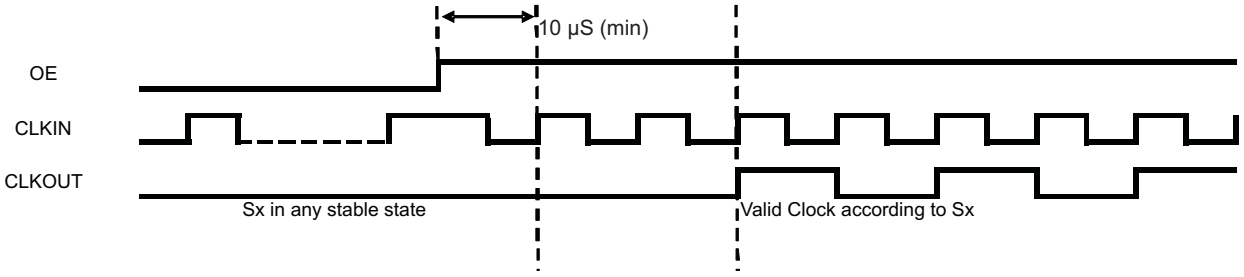
NOTE: Transition to new state will happen after a latency of one output clock cycle after completing the present output clock cycle. Transition to new state will happen after a latency of up to 3 input clock cycles excluding the input cycle where the transition has occurred.

Power Up



NOTE: Transition to new state will happen after a latency of 2 input clock cycles excluding the input cycle where the transition has occurred.

OE Operation



NOTE: Transition to new state will happen after a latency of 2 input clock cycles excluding the input cycle where the transition has occurred.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.3	6	V
V_I	Input voltage range(2)		–0.3	6	V
V_O	Output voltage range in the high or low state(2)		–0.3	6	V
I_{IK}	Input clamp current	$V_I < 0$		±20	mA
I_{OK}	Output clamp current	$V_O < 0$		±20	mA
I_{OL}	Continuous output Low current	$V_O = 0$ to V_{CC}		±20	mA
I_{OH}	Continuous output High current	$V_O = 0$ to V_{CC}		±20	mA
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

			VALUE	UNIT
θ_{JA}	Package thermal impedance(1)	RVK Package	72.2	°C/W

(1) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	3.8	5.5	V
V_{IH}	High-Level Input Voltage	1.6	5.5	V
V_{IL}	Low-Level Input Voltage	0	0.8	V
I_{IH}	High-level input current		1	µA
I_{IL}	Low-level input current		1	µA
V_I		0	5.5	V
V_O		0	VCC	V
I_{OH}	High-level output current		-8	mA
I_{OL}	Low-level output current		8	mA
T_A	Operating free-air temperature	–40	85	°C

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = –40°C to 85°C			UNIT
			MIN	TYP	MAX	
V_{OH}	I_{OH} = –8 mA	3.8 V	Vcc-0.6			V
		5 V	Vcc-0.4			V
V_{OL}	I_{OL} = 8 mA	3.8 V			0.40	V
		5 V			0.40	V
I_i (CLKIN, OE, Sx)	V_I = GND to 4 V	5.5 V			1	µA
I_{CC} (Disabled)	V_{IO} = 0 V or 5.5V, OE = Low	3.8 V to 5.5 V		0.5	2	µA
$I_{DD\_}$ (Dynamic)	OE = 5.5 V; Sx = 0 V, 5.5 V; CLKIN = 0 V, 5.5 V	5.5 V		20	50	µA
	OE = 3.0 V; Sx = 0 V, 3.0 V; CLKIN = 0 V, 3.0 V	5.5 V		20	50	µA
	OE = 1.6 V; Sx = 0 V, 1.6 V; CLKIN = 0 V, 1.6 V	5.5 V		20	50	µA
C_I (CLKIN, OE, Sx)	V_I = V_{CC} or GND			7		pF

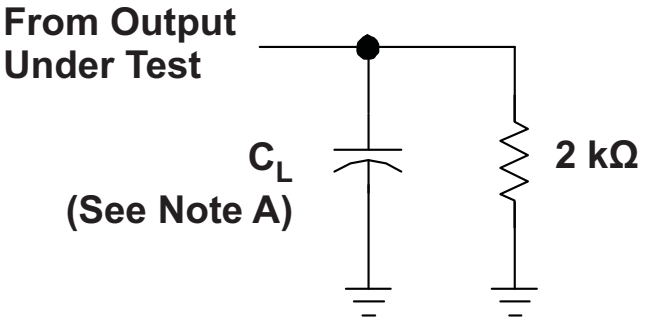
SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

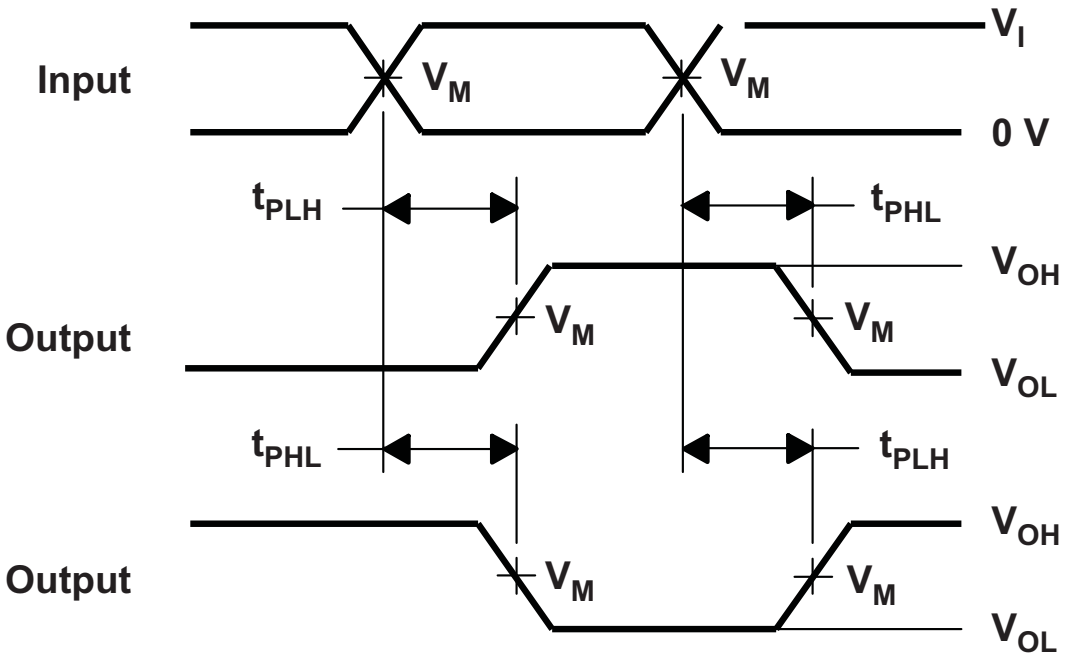
PARAMETER	FROM (INPUT) TO(OUTPUT) V_{CC}	T_A = –40°C to 85°C			UNIT
		MIN	TYP	MAX	
F_{CLKIN}	Input clock frequency	120		240	Hz
F_{CLKOUT}	Output clock frequency	F_{CLKIN} /2		F_{CLKIN} /2	Hz
t_{RISE} / t_{FALL}	Output rise/fall time			10	µs
t_{RISE} / t_{FALL}	Input rise/fall time			50	µs
Input Duty Cycle	Input duty cycle	49%	50%	51%	
Output Duty Cycle	Output duty cycle	49%	50%	5%1	
t_{SU}	Setup time on Sx	60			µs
t_H	Hold time on Sx	60			µs
t_{SKEW}	CLKOUTx skew			10	µs

PARAMETER MEASUREMENT INFORMATION

Propagation Delays



	VCC = 3.3 V ± 0.3 V
C_L	15 pF
V_M	$V_{CC}/2$
V_I	V_{CC}



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NON INVERTING OUTPUTS

A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, for propagation delays t_r/t_f = 3 ns, for setup and hold times and pulse width t_r/t_f = 1.2 ns.

D. The outputs are measured on at a time, with on transition per measurement.

E. t_{PLH} and $_{tPHL}$ are the same a t_{pd}.

F. All parameters and waveforms are no applicable to all devices.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CDC1104RVKR	ACTIVE	WQFN	RVK	12	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZTH	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

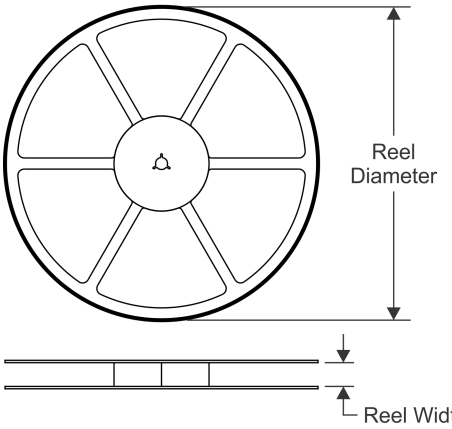
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

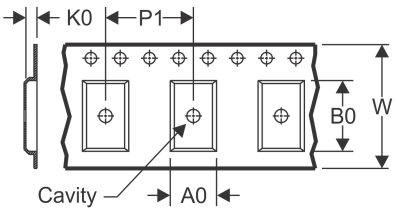
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

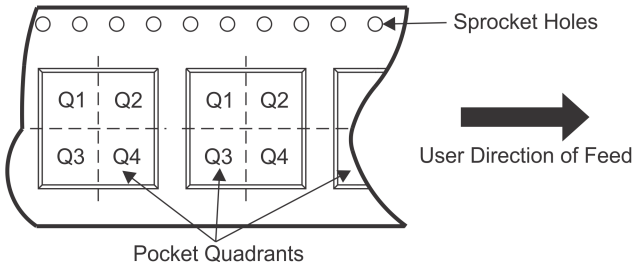


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

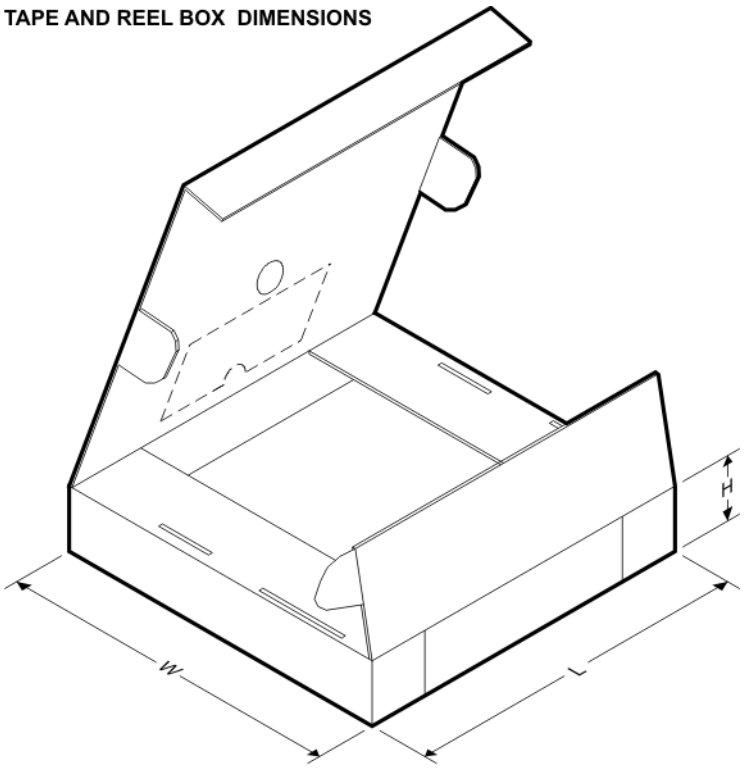
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDC1104RVKR	WQFN	RVK	12	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

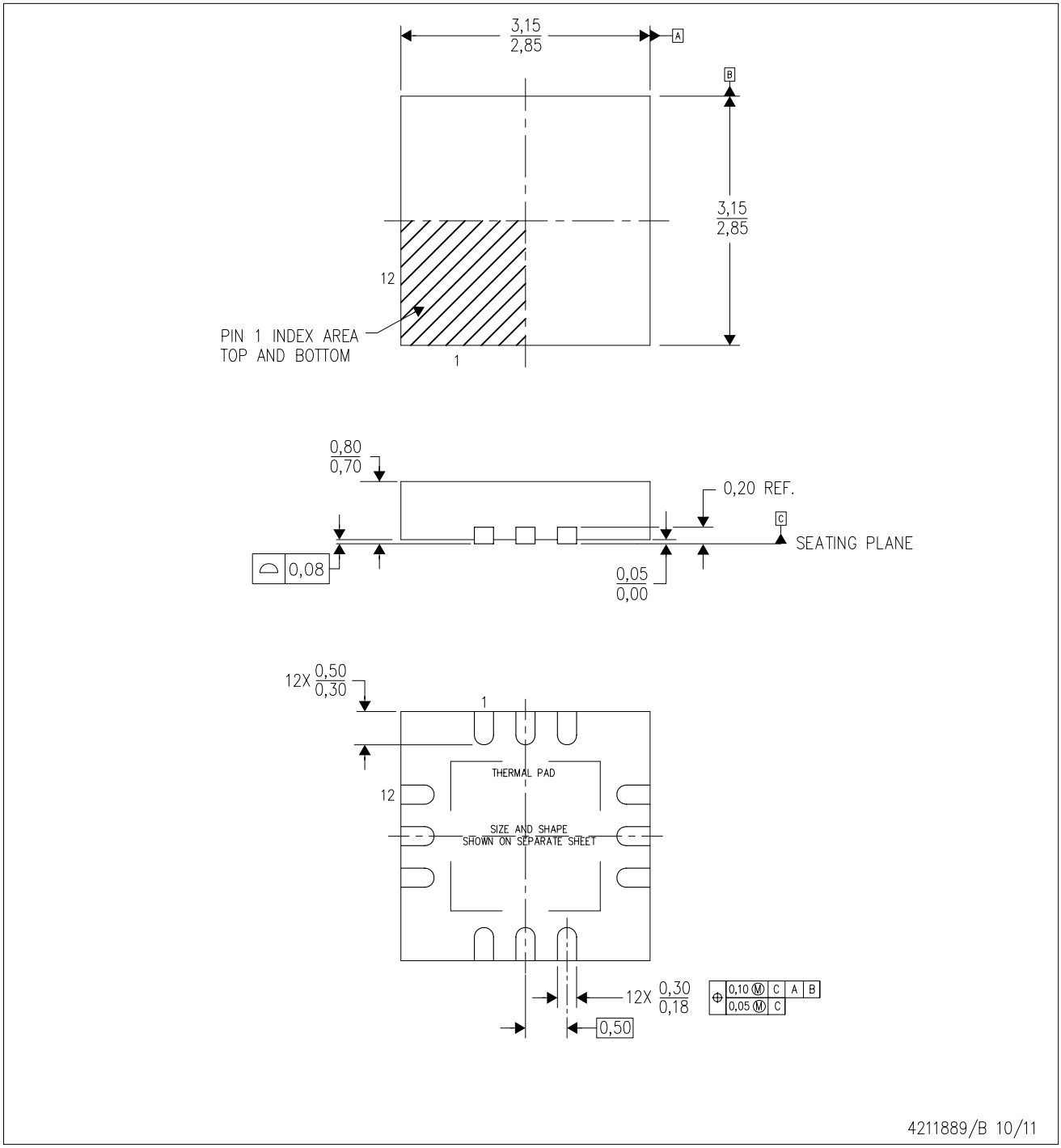
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDC1104RVKR	WQFN	RVK	12	3000	367.0	367.0	35.0

RVK (S–PWQFN–N12) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

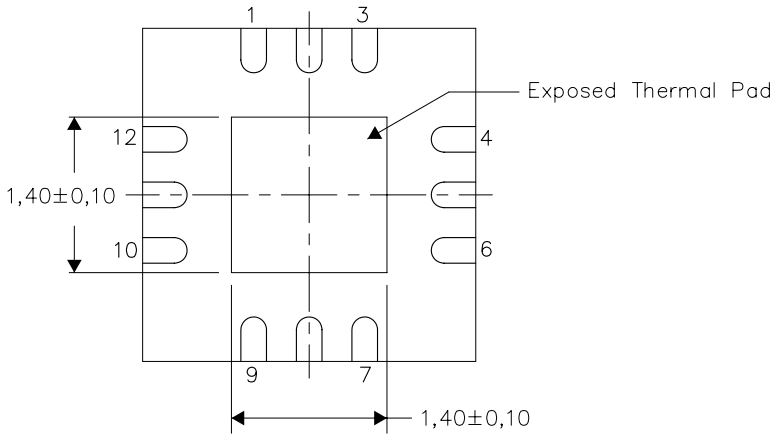
RVK (S–PWQFN–N12) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4211891/A 06/11

NOTE: All linear dimensions are in millimeters

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