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NAME OF PRODUCT DC-AC Inverter Control IC

TYPE

## BD9886F

FUNCTION • 2ch control with Push-Pull

- ·Lamp current and voltage sense feed back control
- · Sequencing easily achieved with Soft Start Control
- Short circuit protection with Timer Latch
- Under Voltage Lock Out
- · Short circuit protection with over voltage
- ·Mode-selectable the operating or stand-by mode by stand-by pin
- ·Synchronous operating the other BD9886F IC's
- BURST mode controlled by PWM and DC input

## ○Absolute Maximum Ratings (Ta = 25℃)

Parameter	Symbol	Limits	Unit
Supply Voltage	Vcc	15	V
Operating Temperature Range	Topr	-40~+90	C
Storage Temperature Range	Tstg	-55~+125	C
Power Dissipation	Pd	600*	mW
Maximum Junction Temperature	Tjmax	+125	Ĉ

\*Pd derated at 6.0mW/°C for temperature above Ta = 25°C (When mounted on a PCB 70.0mm×70.0mm×1.6mm)

ORecommended operating condition

Parameter	Symbol	Limits	Unit
Supply voltage	Vcc	5.0~14.0	V
CT oscillation frequency	fст	20~150	kHz
BCT oscillation frequency	fbCT	0.05~0.50	kHz

Status of this document

The Japanese version of this document is the official specification.

Please use the translation version of this document as a reference to expedite understanding of the official version. If these are any uncertainty in translation version of this document, official version takes priority.

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## OElectric Characteristics (Ta=25°C, VCC=7V)

			Limits		1	
Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Conditions
((WHOLE DEVICE))						
Operating current	Icc1	-	11.0	17.0	mA	T CT=0.5V
Stand-by current	1001	_	2	10	μA	01-01-01-01
((OVER VOLTAGE DETECT))	1. 1002		<u> </u>	10	<u>μη</u>	
FB over voltage detect voltage	Vovf	2.20	2.40	2.60	v	
	0001	2.20	2.40	2.00		
((STAND BY CONTROL))			<u> </u>		<u> </u>	
Stand-by voltage H	VstH	1.6	_	VCC	V	System ON
Stand-by voltage L	VstL	-0.3	-	0.8	V	System OFF
Stand-by hysteresis	⊿Vst	0.08	0.18	0.28	<u> </u>	
((TIMER LATCH))						
Timer Latch voltage	Vcp	1.9	2.0	2.1	V	
Timer Latch current	lcp	0.5	1.0	1.5	μA	
((BURST MODE))						
BOSC Max voltage	VburH	1.94	2.0	2.06	V	fBCT=0.2kHz
BOSC Min Voltage	VburL	0.4	0.5	0.6	V	fBCT=0.2kHz
BOSC constant current	IBCT	1.35/BRT	1.5/BRT	1.65/BRT	A	
BOSC frequency	fBCT	266	280	294	Hz	BRT=33k Ω 、BCT=0.050 μ
((OSC BLOCK))	···		•			····.
OSC constant current	Іст	1.35/RT	1.5/RT	1.65/RT	A	
OSC Max voltage	VoscH	1.8	2.0	2.2	v	fct=60kHz
	VoscL	0.3	0.5	0.7	v v	fct=60kHz
OSC Min voltage						
MAX DUTY	MAXDUTY	44	46.5	49	%	fct=60kHz
Soft start current	lss	1.0	2.0	3.0	μA	
IS COMP detect Voltage	Visc	0.45	0.50	0.55	V	
SS COMP detect voltage	Vss	2.0	2.2	2.4	V	
SRT ON resistance	RSRT	-	200	400	Ω	
((UVLO BLOCK))						
Operating voltage	Vuv I oH	4.100	4.300	4.500	V	
Shut down voltage	VuvioL	3.900	4.100	4.300	V	
Operating voltage (External UVLO)	Vuvlo1	2.160	2.220	2.280	v	
Lock out voltage (External UVLO)	Vuvio2	2.242	2.315	2.388	V	
Hysteresis width	⊿Vuvlo	0.068	0.095	0.122	V	
((REG BLOCK))	•	•				• · · · · · · · · · · · · · · · · · · ·
REG output voltage	VREG	3.038	3.100	3.162	V	
REG source current	IREG	5.0		_	mA	
VREF voltage	Vref	1.225	1.250	1.275	۷ I	VREF=0pen
((FEED BACK BLOCK))	•			•		
IS threshold voltage	Vis	1.225	1.250	1.275	l v	VREF=0pen
	Vvs	1.220	1.250	1.280	v	
VS threshold voltage		-	-			
IS source current 1	lis1			1.5	μΑ	DUTY=2.0V
IS source current 2	lis2	13.0	20.0	27.0	μΑ	DUTY=0V、IS=0.5V
VS source current	lvs	_		1.0	μA	
((OUTPUT BLOCK))		1 1/00 0 0	1/00 C C	1		
NAch output voltage H	VoutNAH	VCC-0.3	VCC-0.1		V	
NBch output voltage H	VoutNBH	VCC-0.3	VCC-0.1		V	
NAch output voltage L	VoutNAL		0.1	0.3	V	
NBch output voltage L	VoutNBL		0.1	0.3	V	
NAch output sink resistance	RsinkNA		5	10	Ω	lsink = 10mA
NAch output source resistance	RsourceNA		8	16	Ω	Isource = 10mA
NBch output sink resistance	RsinkNB	-	5	10	Ω	lsink = 10mA
NBch output source resistance	RsourceNB		8	16	Ω	lsource = 10mA
Drive output frequency	four	58.5	60.0	61.5	KHz	RT=18kΩ、CT=400pF
((COMP BLOCK))						
Under voltage detect	VCOMPL	0.620	0.640	0.660	V	
((PROTECT CLOCK))						
Normal output voltage	VPH	2.9	3.1	3.3	l v	1
Protect output voltage	VPL			0.5	v v	
	1 "		I	0.5	1	

(This product is not designed for normal operation with in a radio active environment.)



OPackage Dimensions



OBlock Diagram

#### REG VREF ст REG BLOCI osc BOSC SYSTEM ON/OFF STB BLOCK STB UVLO BLOCK - vcc J UVLO ss FB1 +vcc ISI LOGIC BLOCK F/B BLOCK① OUTPUT BLOCK① NA1 PWM BLOCK① ss · -VSI 5 NB1 ст・ FB2 +vcc ŧ IS2 F/B BLOCK② LOGIC BLOCK ଅ NA2 PWM BLOCK② OUTPUT BLOCK2 ss VS2 NB2 ст PGND PROTECT BLOCK 🗘 FAIL COMP1 COMP2 SCP SRT

#### **OPin Description**

<b></b>			
Pin No.	Pin	Function	
	Name		
1	DUTY	Control PWM mode and BURST mode	
2	BRT	External resistor from BRT to GND for	
	Uni	adjusting the BURST triangle oscillator	
3	ВСТ	External capacitor from BCT to GND for	
		adjusting the BURST triangle oscillator	
4	RT	External resistor from SRT to RT for	
		adjusting the triangle oscillator	
5	SRT	External resistor from SRT to RT for	
		adjusting the triangle oscillator	
6	Ст	External capacitor from CT to GND for	
		adjusting the triangle oscillator	
7	GND	GROUND	
8	FB1	Error amplifier output(1)	
9	IS1	Error amplifier input①	
10	VS1	Error amplifier input②	
11	FB2	Error amplifier output②	
12	IS2	Error amplifier input③	
13	VS2	Error amplifier input④	
14	VREF	Reference voltage	
15	FAIL	Protect clock output	
16	STB	Stand-by switch	
17	COMP1	Under voltage detect for 1ch	
18	COMP2	Under voltage detect for 2ch	
19	UVLO	External Under Voltage Lock OUT	
20	REG	Internal regulator output	
21	SS	External capacitor from SS to GND for	
21		Soft Start Control	
22	90B	External capacitor from SCP to GND for	
22	SCP	Timer Latch	
23	NA2	FET driver for 2ch	
24	NB2	FET driver for 2ch	
25	PGND	Ground for FET drivers	
26	NB1	FET driver for 1ch	
27	NA1	FET driver for 1ch	
28	Vcc	Supply voltage input	



#### ONOTE FOR USE

- 1. When designing the external circuit, including adequate margins for variation between external devices and the IC.Use adequate margins for steady state and transient characteristics.
- 2. Recommended Operating Range

The circuit functionality is guaranteed within of ambient temperature operation range as long as it is within recommended operating range. The standard electrical characteristic values cannot be guaranteed at other voltages in the operating ranges, however, the variation will be small.

3. Mounting Failures

Mounting failures, such as misdirection or miscounts, may harm the device.

4. Electromagnetic Fields

A strong electromagnetic field may cause the IC to malfunction.

- 5. The GND pin should be the location within  $\pm$ 0.3V compared with the PGND pin
- 6. BD9886FV has the short circuit protection with Thermal Shut Down System. When STB or Vcc pin re-supplied, They enables to cancel the latch. If It rise the temperature of the chip more than 170°C (TYP), It make the external FET OFF
- 7. Absolute maximum ratings are those values that, if exceeded, may cause the life of a device to become significantly shortened. Moreover, the exact failure mode caused by short or open is not defined. Physical countermeasures, such as a fuse, need to be considered when using a device beyond its maximum ratings.
- About the external FET, the parasitic Capacitor may cause the gate voltage to change, when the drain voltage is switching. Make sure to leave adequate margin for this IC variation.
- 9. On operating Slow Start Control (SS is less than 2.2V), It does not operate Timer Latch.
- 10. By STB voltage, BD9886F is changed to 2 states. Therefore, do not input STB pin voltage between one state and the other state (0.8~1.6).
- 1 1. The pin connected a connector need to connect to the resistor for electrical surge destruction.
- 1 2. This IC is a monolithic IC which (as shown is Fig-1)has P<sup>+</sup> substrate and between the various pins. A P-N junction is formed from this P layer of each pin. For example, the relation between each potential is as follows,

 $\bigcirc$  (When GND > PinB and GND > PinA, the P-N junction operates as a parasitic diode.)

 $\bigcirc$  (When PinB > GND > PinA, the P-N junction operates as a parasitic transistor.)

Parasitic diodes can occur inevitably in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits as well as operation faults and physical damage. Accordingly you must not use methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND(P substrate)voltage to an input pin. Resistance Transistor (NPN)



Fig-1 Simplified structure of a Bipolar IC

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As of 18th. April 2005