LDMOS 2-stage power MMIC Rev. 2 — 22 April 2022

Product profile 1.

1.1 General description

The BLM9H0610S-60PG is a dual section, 2-stage power MMIC using Ampleon's state of the art GEN9 HV LDMMIC technology. This multiband device is perfectly suited as general purpose driver or small cell final in the frequency range from 600 MHz to 1000 MHz. Available in gull wing outline.

Performance Table 1.

Typical RF performance at $T_{case} = 25$ °C. Test signal: 3GPP test model 1; 64 DPCH; PAR = 9.9 dB at 0.01 % probability on CCDF; specified in a quadrature combined class-AB demo circuit.

Test signal	f	V _{DS}	P _{L(AV)}	G _p	η _D	ACPR _{5M}
	(MHz)	(V)	(W)	(dB)	(%)	(dBc)
single carrier W-CDMA	853	48	2.5	35.5	12	-45

1.2 Features and benefits

- Designed for broadband operation (frequency 600 MHz to 1000 MHz)
- High section-to-section isolation enabling multiple combinations
- Biasing of individual stages is externally accessible
- Integrated ESD protection
- Excellent thermal stability
- High power gain
- On-chip matching for ease of use
- For RoHS compliance see the product details on the Ampleon website

1.3 Applications

- RF power MMIC for W-CDMA base stations in the 600 MHz to 1000 MHz frequency range. Possible circuit topologies are the following as also depicted in Section 8.1:
 - Dual section or single ended
 - Doherty
 - Quadrature combined
 - Push-pull

2. Pinning information

2.1 Pinning



2.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
V _{DS(A1)}	1	drain-source voltage of section A, driver stage (A1)
V _{GS(A2)}	2	gate-source voltage of section A, final stage (A2)
V _{GS(A1)}	3	gate-source voltage of section A, driver stage (A1)
RF_IN_A	4	RF input section A
n.c.	5	not connected
n.c.	6	not connected
n.c.	7	not connected
n.c.	8	not connected
n.c.	9	not connected
n.c.	10	not connected
RF_IN_B	11	RF input section B
V _{GS(B1)}	12	gate-source voltage of section B, driver stage (B1)
V _{GS(B2)}	13	gate-source voltage of section B, final stage (B2)
V _{DS(B1)}	14	drain-source voltage of section B, driver stage (B1)

Table 2. Pin descriptioncontinued								
Symbol	Pin	Description						
RF_OUT_B/V _{DS(B2)}	15	RF output section B / drain-source voltage of section B, final stage (B2)						
RF_OUT_A/V _{DS(A2)}	16	RF output section A / drain-source voltage of section A, final stage (A2)						
GND	flange	RF ground						

3. Ordering information

Table 3. Ordering			information
	Type num	ber	Package

Type number	Раска	аскаде						
	Name	Description	Version					
BLM9H0610S-60PG		plastic, heatsink small outline package; 16 leads	OMP-780-16G-1					

4. Block diagram



5. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	drain-source voltage		-	108	V
V _{GS}	gate-source voltage		-6	+13	V
T _{stg}	storage temperature		-65	+150	°C
Tj	junction temperature	<u>[1]</u>	-	225	°C
T _{case}	case temperature		-	125	°C

[1] Continuous use at maximum temperature will affect the reliability. For details refer to the online MTF calculator.

6. Thermal characteristics

Table 5. Thermal characteristics

Measured per section of device.

Symbol	Parameter	Conditions	Value	Unit
11(10)	thermal resistance from junction to case	final stage; $T_{case} = 80 \text{ °C}$; $P_L = 1.25 \text{ W}$ [1]	3.50	K/W

[1] When operated with a CW signal.

7. Characteristics

Table 6. DC characteristics

 $T_{case} = 25 \ ^{\circ}C$; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Final sta	ge	1				
V _{(BR)DSS}	drain-source breakdown voltage	$V_{GS} = 0 V; I_D = 256 \mu A$	108	-	-	V
V _{GSq}	gate-source quiescent voltage	V _{DS} = 48 V; I _D = 125 mA	1.55	2.16	2.55	V
I _{DSS}	drain leakage current	$V_{GS} = 0 V; V_{DS} = 48 V$	-	-	1.4	μA
I _{DSX}	drain cut-off current	$V_{GS} = 5.8 \text{ V}; V_{DS} = 10 \text{ V}$	-	4.1	-	А
I _{GSS}	gate leakage current	V_{GS} = 1.0 V; V_{DS} = 0 V	-	-	140	nA
Driver st	age					
V _{(BR)DSS}	drain-source breakdown voltage	$V_{GS} = 0 V; I_D = 51 \mu A$	108	-	-	V
V _{GSq}	gate-source quiescent voltage	V _{DS} = 48 V; I _D = 25 mA	1.55	2.16	2.55	V
I _{DSS}	drain leakage current	$V_{GS} = 0 V; V_{DS} = 48 V$	-	-	1.4	μΑ
I _{GSS}	gate leakage current	V_{GS} = 1.0 V; V_{DS} = 0 V	-	-	140	nA

Table 7. RF Characteristics

Test signal: pulsed CW: $t_p = 455 \ \mu$ s; $\delta = 8.65 \ \%$; RF performance at $V_{DS} = 48 \ V$; $I_{Dq1} = 25 \ mA$ (driver stage); $I_{Dq2} = 125 \ mA$ (final stage); $T_{case} = 25 \ ^{\circ}C$; $P_{L(AV)} = 1.25 \ W$; per section unless otherwise specified in a production circuit.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
G _p	power gain	f = 957.5 MHz	34	35.5	-	dB
η _D	drain efficiency	f = 957.5 MHz	8	11	-	%
RL _{in}	input return loss	f = 957.5 MHz	-	-18	-11	dB
P _{L(1dB)}	output power at 1 dB gain compression		44.6	45.3	-	dBm

8. Application information

Table 8. Typical performance

Test signal: 1-tone pulsed CW; RF performance at $T_{case} = 25 \text{ °C}$; $V_{DS} = 48 \text{ V}$; $I_{Dq1} = 25 \text{ mA}$ (driver); $I_{Dq2} = 125 \text{ mA}$ (final); per section; measured in a quadrature combined application circuit operating in the 758 MHz to 960 MHz band.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
P _{L(1dB)}	output power at 1 dB gain compression	f = 800 MHz	-	61.4	-	W
η_D	drain efficiency	at P _{L(1dB)} ; f = 800 MHz	-	69.1	-	%
Gp	power gain	P _{L(AV)} = 2.5 W; f = 800 MHz	-	38.1	-	dB
B _{video}	video bandwidth	2-tone CW; $P_{L(AV)} = 2.5$ W; f = 853 MHz	-	150.0	-	MHz
G _{flat}	gain flatness	$P_{L(AV)} = 2.5 \text{ W}; f = 758 \text{ MHz to } 960 \text{ MHz}$	-	1.6	-	dB
s12 ²	isolation	between section A and section B; f = 800 MHz	-	29.0	-	dB
К	Rollett stability factor	T_{case} = 25 °C; f = 0.6 GHz to 1.0 GHz	-	>1.6	-	

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Table 9.List of componentsSee Figure 3 for component layout.

Component	Description	Value	Remarks
C1, C8, C10, C18	multilayer ceramic chip capacitor	4.7 μF, 50 V	Murata: GRM32ER71H475KA88L, SMD 1210
C2, C3, C4, C5, C6, C7, C9, C17	multilayer ceramic chip capacitor	100 nF, 50 V	SMD 0805
C11, C13, C14, C16	multilayer ceramic chip capacitor	82 pF	Murata: HiQ, GQM21 series, SMD 805
C12, C15	multilayer ceramic chip capacitor	2.4 pF	Murata: HiQ, GQM21 series, SMD 805
R1, R8	resistor	1 kΩ, 1 %	SMD 805
R2, R9	resistor	1 kΩ, 1 %	SMD 805
R3, R7	resistor	56 kΩ, 1 % [<u>1]</u>	SMD 805
R4, R6	resistor	56 kΩ, 1 % [<u>1]</u>	SMD 805
R5, R10	resistor	50 Ω, 25 W	Anaren: C16A50Z4
L1, L2	RF choke	$5 \times 3 \text{ mm}$	
CLP1, CLP2	hybrid coupler	3 dB, 90°	Anaren: X3C09P1-03S

[1] Tune for I_{Dq} driver.

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8.1 Possible circuit topologies







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8.2 Ruggedness in a Doherty operation

The BLM9H0610S-60PG is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 55 V; I_{Dq1} = 25 mA (driver); I_{Dq2} = 125 mA (final); at CW P_L = 25 W under Z_S = 50 Ω ; f = 925 MHz.

8.3 Impedance information

Table 10. Typical impedance tuned for maximum output power

Measured load-pull data per section; test signal: pulsed CW; $T_{case} = 25 \ ^{\circ}C$; $V_{DS} = 48 \ V$; $I_{Dq1} = 25 \ mA$ (driver); $I_{Dq2} = 125 \ mA$ (final); $t_p = 100 \ \mu$ s; $\delta = 10 \ ^{\circ}$; $Z_S = 50 \ ^{\circ}\Omega$. Typical values unless otherwise specified.

	tuned for maximum output power				tuned for maximum power added efficiency					
f	ZL	G _{p(max)}	PL	໗ _{add}	AM-PM conversion	ZL	G _{p(max)}	PL	η_{add}	AM-PM conversion
(MHz)	(Ω)	(dB)	(W)	(%)	(deg)	(Ω)	(dB)	(W)	(%)	(deg)
652.0	6.9 + j 7.5	38.0	49.3	57.2	-3.0	4.7 + j 15.3	41.2	21.7	65.0	-12.5
698.0	9.7 + j 6.4	37.7	52.9	60.9	-5.2	7.8 + j 12.4	39.4	37.1	68.0	-5.4
720.0	10.6 + j 4.2	36.7	54.0	57.1	1.8	7.8 + j 12.3	39.1	35.7	66.9	-3.5
746.0	10.7 + j 4.3	36.4	56.3	58.6	-1.2	7.8 + j 12.4	39.1	35.3	67.8	-4.4
769.0	10.9 + j 5.9	36.7	58.1	63.6	-1.2	7.8 + j 12.3	38.4	38.2	70.6	-5.9
798.0	13.1 + j 4.7	36.4	56.7	60.5	-2.7	6.1 + j 12.1	38.5	33.1	69.2	-10.0
820.0	12.5 + j 5.2	36.5	56.0	63.7	-0.2	6.7 + j 11.2	38.4	36.4	71.3	-12.6
869.0	13.2 + j 2.2	35.8	54.4	56.9	-6.2	6.6 + j 9.8	38.0	40.5	70.7	-6.0
880.0	12.6 + j 5.2	36.0	54.4	62.1	-1.5	6.7 + j 11.2	38.6	33.8	69.9	-12.6
894.0	12.5 + j 5.2	35.9	54.1	61.8	-6.4	6.5 + j 9.7	37.8	40.1	70.0	-5.6
920.0	13.0 + j 2.3	35.4	51.8	55.4	-2.1	6.5 + j 9.8	38.2	37.3	69.7	-6.0
940.0	10.0 + j 4.6	35.7	54.9	62.6	2.1	5.0 + j 10.0	37.9	33.4	71.9	-4.9
960.0	8.5 + j 5.4	36.1	54.6	66.0	-4.1	4.9 + j 8.6	37.8	38.0	71.9	-4.1
1000.0	7.8 + j 4.1	35.3	58.5	66.0	-0.3	4.4 + j 7.4	36.8	41.3	73.5	-8.7

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8.4 Graphs



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9. Package outline



Fig 17. Package outline OMP-780-16G-1 (sheet 1 of 2)

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OMP-780-16G-1

			—			
Items	Description					
	Dimensions are exc	Dimensions are excluding mold protrusion. Areas located adjacent to the leads have a maximum mold protrusion of 0.25				
(1)	mm (per side) and 0.62 mm max. in length. In between the 14 leads the protrusion is 0.25 mm max. At all other areas the					
	mold protrusion is maximum 0.15 mm per side. See also detail B.					
(2)	The metal protrusion (tie bars) in the corner will not stick out of the molding compound protrusions (detail A).					
(3)	The lead dambar (metal) protrusions are not included. Add 0.14 mm max to the total lead dimension at the dambar location.					
(4)	The hatched area in	ed area indicated the exposed heatsink.				
(5)	The leads and exposed heatsink are plated with matte Tin (Sn).					
(6)	Dimension is measured with respect to the bottom of the heatsink Datum H. Positive value means that the bottom of the heatsink is higher than the bottom of the lead.					
(7)	-		ured from the seating plane.			
(
(B	DETAIL A SCALE 25:1			
		B	Lead dambar location DETAIL A SCALE 25:1			
(utline drawing:	B D D D D D D D D D D D D D D D D D D D	SCALE 25:1	3/1/2		

Fig 18. Package outline OMP-780-16G-1 (sheet 2 of 2)

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10. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A or equivalent standards.

Table 11.ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2A [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	1C [2]

[1] CDM classification C2A is granted to any part that passes after exposure to an ESD pulse of 500 V.

[2] HBM classification 1C is granted to any part that passes after exposure to an ESD pulse of 1000 V.

11. Abbreviations

Table 12. Abbreviations			
Acronym	Description		
3GPP	3rd Generation Partnership Project		
CCDF	Complementary Cumulative Distribution Function		
CW	Continuous Wave		
DPCH	Dedicated Physical CHannel		
ESD	ElectroStatic Discharge		
GEN9	Ninth Generation		
HV	High Voltage		
LDMMIC	Laterally Diffused Monolithic Microwave Integrated Circuit		
LDMOS	Laterally Diffused Metal Oxide Semiconductor		
MMIC	Monolithic Microwave Integrated Circuit		
MTF	Median Time to Failure		
PAR	Peak-to-Average Ratio		
RoHS	Restriction of Hazardous Substances		
SMD	Surface Mounted Device		
VBW	Video BandWidth		
W-CDMA	Wideband Code Division Multiple Access		

12. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLM9H0610S-60PG v.2	20220422	Product data sheet	-	BLM9H0610S-60PG v.1
Modifications:	Section 5 on	page 3: changed case te	emperature value from	m 110 °C to 125 °C
	Section 13.2	on page 18: updated sec	ction	
	Section 13.3	on page 18: updated sec	ction	
BLM9H0610S-60PG v.1	20200306	Product data sheet	-	-

13. Legal information

13.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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Date of release: 22 April 2022 Document identifier: BLM9H0610S-60PG