

PRODUCT/PROCESS CHANGE NOTIFICATION

PCN APG-ABD/14/8491 Dated 26 May 2014

Bipolar Technology : Wafer Diameter Change from 5 to 6 (Ang Mo Kio - Singapore)

Table 1. Change Implementation Schedule

Forecasted implementation date for change	31-Jul-2014
Forecasted availability date of samples for customer	30-Jun-2014
Forecasted date for STMicroelectronics change Qualification Plan results availability	26-Jul-2014
Estimated date of changed product first shipment	31-Jul-2014

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	see list
Type of change	Waferfab material change
Reason for change	Company Road Map
Description of the change	We are going to change the wafer diameter of some Bipolar technology products from 5 inchs to 6 inchs in Ang Mo Kio - Singapore.
Change Product Identification	Dedicated Finished-Good codes
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	

Customer Acknowledgement of Receipt	PCN APG-ABD/14/8491
Please sign and return to STMicroelectronics Sales Office	Dated 26 May 2014
Qualification Plan Denied	Name:
Qualification Plan Approved	Title:
	Company:
🗖 Change Denied	Date:
Change Approved	Signature:
Remark	

Name	Function
Celant, Luca	Marketing Manager
Nicoloso, Riccardo	Product Manager
Pintus, Alberto	Q.A. Manager

DOCUMENT APPROVAL



Bipolar Technology - Wafer Diameter Change from 5" to 6" (Ang Mo Kio – Singapore)

WHAT:

We are going to change the wafer diameter of some Bipolar technology products from 5 inchs to 6 inchs in Ang Mo Kio - Singapore.

WHY:

Company Road Map

HOW:

See enclosed qualification plan QP0034 14 CS2039 (Completion scheduled on July 2014)

Sample availability on demand through Sales Offices

WHEN:

We are ready to implement the change, upon Customer agreemnt, from July 2014

See below list of products involved

Line	-	Product 🗾
L00903		E-TDA7391PD
L00903		E-TDA7391PDTR
L00903		TDA7391
L00903		TDA7391LV
L00903		TDA7391LVPD
L00903		TDA7391LVPDTR
L00903		TDA7391LVPDU
L00903		TDA7391LVPDUTR
L00903		TDA7391PDU
L00903		TDA7391PDUTR
L24903		TDA2004R
L35003		TDA2005R
L35003		XL350CAX-GCP

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Q100 QUALIFICATION TEST PLAN

 Automotive Grade Level:
 3
 -40 +85°C
 MSL
 3

Supplier Name:	STM	General Specification:	AEC Q100 Rev. G
Supplier Part number:	TDA2003/TDA2004/TDA2005/TDA7391	Supplier Wafer Fabrication:	AMK
Line code:	L540/L249/L350/L009	Supplier Assembly site:	Muar (PSO), BSK (MW)
Device Description:	Power Amp	Package:	PSO20 & MW
Process:	BIPOLAR	Date:	9 May 2014
Reason of Qualification:	Wafer Diameter change (5" \rightarrow 6")		

Test	#	Reference	Test Conditions	Lots	SS	Total	Comments
							(NA=Not Applicable)

TEST GROUP A ACCELERATED ENVIRONMENT STRESS TESTS

PC	A1	JESD22 A113 J-STD-020	Preconditioning: (Test @ Rm) SMD only; Moisture Preconditioning for THB/ HAST , AC/ UHST , TC, & PTC; Peak Reflow Temp = 245°C	3	231	693	MSL3 Planned for PSO20
THB 1	A2	JESD22 A101	Temperature Humidity Bias: (Test @ Rm/Hot) 85C/85%, 1000h	3	77	231	NA; Planned on three lots for FE.BE compatibility
AC ¹	A3	JESD22 A102	Autoclave: (Test @ Rm) 96h, 121C, 2atm	3	77	231	NA; Planned on three lots for FE.BE compatibility
тс	A4	JESD22 A104	Temperature Cycle: (Test @ Hot) Range 1: 1000c, -50/+150C Range 2: 500c, -65/+150°C	3	77	231	Planned
PTC	A5	JESD22 A105	Power Temperature Cycle: (Test @ Rm/Hot)	1	45	45	Failure mode covered by TC and HTOL stress tests
HTSL	A6	JESD22 A103	High Temperature Storage Life: (Test @ Rm/Hot) 500h, 150C	1	45	45	NA; Planned on three lots for FE.BE compatibility

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Test	#	Reference	Test Conditions	Lots	SS	Total	Comments
							(NA= Not Applicable)

TEST GROUP B ACCELERATED LIFETIME SIMULATION TESTS

HTOL	B1	JESD22 A108	High Temp Operating Life: (Test @ Rm/Hot/Cold) Tj=150C, 1000h, Vs= 16V	3	77	231	Planned on three diffusion lots (TDA2003, TDA7391 and one lot covered by Family data ²)
ELFR	B2	AEC-Q100-008	Early Life Failure Rate: (Test @ Rm/Hot) Tj=125°C, 24h, Vs=16V	3	800	2400	Planned on TDA2003
EDR	B3	AEC-Q100-005	NVM Endurance & Data Retention Test: (Test @ Rm/Hot)	-	-	-	NA

Test	#	Reference	Test Conditions	Lots	SS	Total	Comments
							(NA=Not Applicable)

TEST GROUP C PACKAGE ASSEMBLY INTEGRITY TESTS

WBS	C1	AEC-Q100-001	Wire Bond Shear Test: (Ppk > 1.67 and Cpk > 1.33)	30 bonds	5 parts	30	Assy data
WBP	C2	Mil-STD-883 Method 2011	Wire Bond Pull: (Ppk > 1.67 and Cpk > 1.33);	30 bonds	5 parts	30	Planned after TC and HTSL
SD	С3	JESD22 B102	Solderability: (>95% coverage)	3	15	45	NA
PD	C4	JESD22 B100, JESD22 B108	Physical Dimensions: (Ppk > 1.67 and Cpk > 1.33)	3	10	30	NA
SBS	С5	AEC-Q100-010	Solder Ball Shear: (Ppk > 1.67 and Cpk > 1.33)	50 balls	1	50	NA
LI	С6	JESD22 B105	Lead Integrity: (No lead cracking or breaking); Through-hole only	50 leads	1	50	NA

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Test	#	Reference	Test Conditions	Lots	SS	Total	Comments
							(NA=Not Applicable)

TEST GROUP D DIE FABBRICATION RELIABILITY TESTS

EM	D1	JESD61	Electromigration:	-	-	-	Process Data
TDDB	D2	JESD35	Time Dependant Dielectric Breakdown:	-	-	-	Process Data
HCI	D3	JESD60 & 28	Hot Carrier Injection:	-	-	-	Process Data
NBTI	D4	JESD90	Negative Bias Temperature Instability	-	-	-	Process Data
SM	D5	JESD61, 87 & 202	Stress Migration	-	-	-	Process Data

Test	#	Reference	Test Conditions	Lots	SS	Total	Comments
							(NA=not applicable)

TEST GROUP E DIE FABBRICATION RELIABILITY TESTS

TST	E1	User/Supplier Specification	Pre and Post Stress Electrical Test:	All	All	All	In accordance to product spec
HBM- MM	E2	AEC-Q100-002 AEC-Q100-003	Electrostatic Discharge, Human Body Model / Machine Model: (Test @ Rm/Hot); (2kV HBM / 200V MM) HBM+ MM	1	3	6	Planned
CDM	E3	AEC-Q100-011	Electrostatic Discharge, Charged Device Model: (Test @ Rm/Hot); (750V corner leads, 500V all other leads)	1	3	3	Planned
LU	E4	AEC-Q100-004	Latch-Up: (Test @ Rm/Hot)	1	6	6	Planned
ED	E5	AEC-Q100-009	Electrical Distributions: (Test @ Rm/Hot/Cold) (Cpk > 1.33, Ppk > 1.67)	3	30	90	Planned
FG	E6	AEC-Q100-007	Fault Grading	-	-	-	NA
CHAR	E7	AEC-Q003	Characterization: (Test @ Rm/Hot/Cold)	-	-	-	Planned
GL	E8	AEC-Q100-006	Electro-Thermally Induced Gate Leakage: (Test @ Rm)	1	6	6	NA
EMC	E9	SAE J1752/3	IEC62132-2: Integrated circuits - Measurement of electromagnetic immunity, 150 kHz to 1 GHz	1	1	1	NA

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SC	E10	AEC-Q100 012	Short circuit Characterization	3	10	30	Performed according to ST internal specification
		JESD89-1					
SER	E11	JESD89-2	Soft Error Rate	1	3	3	NA
		JESD89-3					

Test	#	Reference	Test Conditions	Lots	SS	Total	Comments
							(NA=Not Applicable)

TEST GROUP F DEFECT SCREENING TESTS

PAT	F1	AEC-Q001	See AEC-Q001- This is highly recommended by Automotive Electronic	All	All	All	NA
SBL	F2	AEC-Q002	See AEC-Q001- This is highly recommended by Automotive Electronic Council	All	All	All	NA

Test	#	Reference	Test Conditions	Lots	SS	Total	Comments
							(NA=Not Applicable)

TEST GROUP G CAVITY PACKAGE INTEGRITY TESTS

MS	ESD22 B104 Test after CA	Mechanical Shock: (Test @ Rm)	-	-	-	NA
VFV	JESD22 B103 Test after CA	Variable Frequency Vibration: (Test @ Rm)	-	-	-	NA
CA	Mil-STD-883 Method 2001	Constant Acceleration: (Test @ Rm)	-	-	-	NA
GFL	Mil-STD-883 Method 1014	Gross and Fine Leak:	-	-	-	NA
DROP	-	Drop Test: (Test @ Rm) MEMS cavity parts only. Drop part on each of 6 axes once from a height of 1.2m onto a concrete surface.	-	-	-	NA
LT	Mil-STD-883	Lid Torque:	-	-	-	NA

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	Method 2	004				
DS	Mil-STD-	383 Die Shear:			-	NA
05	Method 2	Die Shedra	-	-		
IWV	Mil-STD-	383 Teternel Water Veneri				N4
TAAA	Method 1	118 Internal Water Vapor:	-	-	-	NA

NOTES

- 1. Test preceded by 100 thermal cycling for robust evaluation.
- 2. PTV: L4949

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