

2.5V Drive Nch MOSFET

RJU002N06

Structure

Silicon N-channel MOS FET

Features

1) Low On-resistance.

2) Low voltage drive (2.5V drive).

Applications

Switching

Packaging specifications

	Package	Taping
Туре	Code	T106
	Basic ordering unit (pieces)	3000
RJU002N06	0	

•Dimensions (Unit : mm)



Inner circuit



•Absolute maximum ratings (Ta=25°C)

Parameter		Symbol	Limits	Unit	
Drain-source voltage		VDSS	60	V	
Gate-source voltage		V _{GSS}	±12	V	
Droin ourront	Continuous	ID	±200	mA	
Drain current	Pulsed	I _{DP} *1	±800	mA	
Total power dissipation		P _D *2	200	mW	
Channel temperature		Tch	150	°C	
Range of storage temperature		Tstg	-55 to +150	۵°	
*1 Pws10us Duty cyclos1%					

*1 Pw≤10μs, Duty cycle≤1% *2 Each terminal mounted on a recommended land

Thermal resistance

Parameter	Symbol	Limits	Unit
Channel to ambient	Rth(ch-a)*	625	°C/W
	Kiii(Cii-a)	025	0/11

* Each terminal mounted on a recommended land

•Electrical characteristics (Ta=25°C)

Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions
Gate-source leakage	Igss	-	-	±10	μΑ	Vgs=±12V, Vds=0V
Drain-source breakdown voltage	$V_{(BR)DSS}$	60	-	_	V	I _D = 1mA, V _{GS} =0V
Zero gate voltage drain current	IDSS	_	-	1	μΑ	V _{DS} = 60V, V _{GS} =0V
Gate threshold voltage	V _{GS (th)}	0.5	_	1.5	V	V _{DS} = 10V, I _D = 1mA
Static drain-source on-state resistance	$R_{DS}(on)^*$	-	1.6	2.3	Ω	ID= 200mA, VGs= 4.5V
		-	1.7	2.4	Ω	I _D = 200mA, V _{GS} = 4V
		-	2.2	3.1	Ω	I _D = 200mA, V _{GS} = 2.5V
Forward transfer admittance	Y _{fs} *	0.1	-	_	S	V _{DS} = 10V, I _D = 200mA
Input capacitance	Ciss	-	18	_	pF	VDS= 10V
Output capacitance	Coss	-	7	_	pF	V _{GS} =0V
Reverse transfer capacitance	Crss	-	5	_	pF	f=1MHz
Turn-on delay time	td (on) *	_	7	_	ns	Vdd≒ 30V
Rise time	tr *	_	7	_	ns	$I_{D}=100mA$
Turn-off delay time	td (off) *	-	12	-	ns	Vgs= 4V RL=300Ω
Fall time	t _f *	-	90	_	ns	$R_{G}=10\Omega$

•Body diode characteristics (Source-drain) (Ta=25°C)

Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions
Forward voltage	Vsd	-	-	1.2	V	Is= 0.16A, V _{GS} =0V

•Electrical characteristics curves







Fig.12 Normalized Transient Thermal Resistance vs. Pulse Width

Notes

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Appendix-Rev4.1