

DUAL P-CHANNEL ENHANCEMENT MODE MOSFET
Product Summary

$V_{(BR)DSS}$	$R_{DS(on) max}$	I_D $T_A = +25^\circ C$
-30V	65m Ω @ $V_{GS} = -10V$	-4.4A
	115m Ω @ $V_{GS} = -4.5V$	-3.2A

Description

This new generation MOSFET has been designed to minimize the on-state resistance ($R_{DS(ON)}$) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

Applications

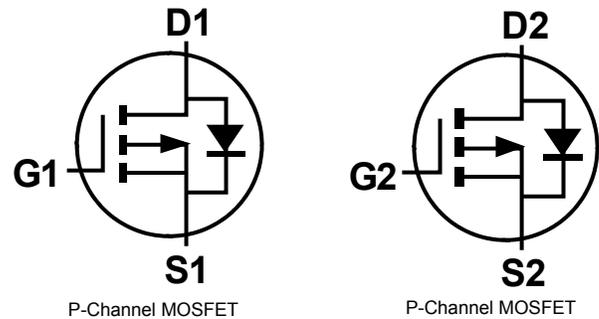
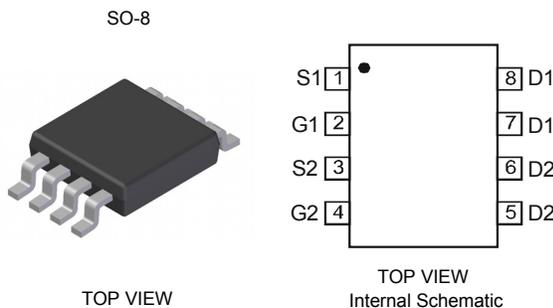
- Power Management Functions
- Analog Switch
- Load Switch
- Boost Switch

Features

- Dual P-Channel MOSFET
- Low On-Resistance
- Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

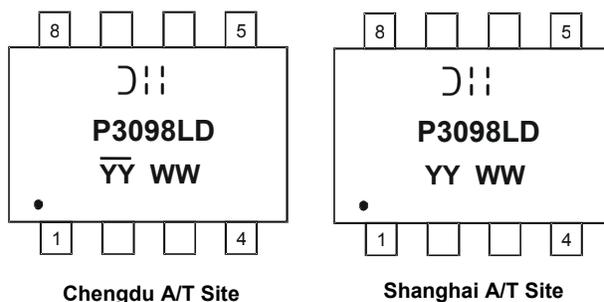
Mechanical Data

- Case: SO-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections Indicator: See Diagram
- Terminals: Finish - Matte Tin annealed over Copper lead frame. Solderable per MIL-STD-202, Method 208 $\text{\textcircled{3}}$
- Weight: 0.072g (approximate)


Ordering Information (Note 4)

Part Number	Case	Packaging
DMP3098LSD-13	SO-8	2,500/Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
 2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 4. For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

Marking Information


- $\text{\textcircled{D}}$::= Manufacturer's Marking
 P3098LD = Product Type Marking Code
 YYWW = Date Code Marking
 YY or YY = Year (ex: 14 = 2014)
 WW = Week (01 - 53)
 \overline{YY} = Date Code Marking for SAT (Shanghai Assembly/ Test site)
 \overline{YY} = Date Code Marking for CAT (Chengdu Assembly/ Test site)

Maximum Ratings (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic			Symbol	Value	Units
Drain-Source Voltage			V_{DSS}	-30	V
Gate-Source Voltage			V_{GSS}	± 20	V
Drain Current (Note 5)	Steady State	$T_A = +25^\circ\text{C}$	I_D	-4.4	A
		$T_A = +70^\circ\text{C}$		-3.3	
Pulsed Drain Current (Note 6)			I_{DM}	-15	A

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Total Power Dissipation (Note 5)	P_D	1.8	W
Thermal Resistance, Junction to Ambient (Note 5)	$R_{\theta JA}$	70	$^\circ\text{C/W}$
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ\text{C}$

Electrical Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	-30	—	—	V	$V_{GS} = 0V, I_D = -250\mu\text{A}$
Zero Gate Voltage Drain Current	I_{DSS}	—	—	-1	μA	$V_{DS} = -30V, V_{GS} = 0V$
Gate-Source Leakage	I_{GSS}	—	—	± 100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(th)}$	-1	1.7	-2.1	V	$V_{DS} = V_{GS}, I_D = -250\mu\text{A}$
Static Drain-Source On-Resistance	$R_{DS(on)}$	—	56	65	m Ω	$V_{GS} = -10V, I_D = -5.0A$
		—	98	115		$V_{GS} = -4.5V, I_D = -4.0A$
Forward Transconductance	g_{fs}	—	5.2	—	S	$V_{DS} = -10V, I_D = -5.0A$
Diode Forward Voltage (Note 7)	V_{SD}	-0.5	—	-1.2	V	$V_{GS} = 0V, I_S = -2.6A$
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{iss}	—	336	—	pF	$V_{DS} = -25V, V_{GS} = 0V$ $f = 1.0\text{MHz}$
Output Capacitance	C_{oss}	—	70	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	49	—	pF	
Gate Resistance	R_G	—	4.6	—	Ω	$V_{DS} = 0V, V_{GS} = 0V, f = 1.0\text{MHz}$
SWITCHING CHARACTERISTICS						
Total Gate Charge	Q_g	—	4.0	—	nC	$V_{DS} = -15V, V_{GS} = -4.5V, I_D = -5.0A$
			7.8			$V_{DS} = -15V, V_{GS} = -10V, I_D = -5.0A$
Gate-Source Charge	Q_{gs}	—	1.0	—		$V_{DS} = -15V, V_{GS} = -4.5V, I_D = -5.0A$
Gate-Drain Charge	Q_{gd}	—	2.5	—		$V_{DS} = -15V, V_{GS} = -4.5V, I_D = -5.0A$
Turn-On Delay Time	$t_{d(on)}$	—	6.0	—	ns	$V_{DS} = -15V, V_{GS} = -10V,$ $I_D = -1A, R_G = 6.0\Omega$
Rise Time	t_r	—	5.0	—		
Turn-Off Delay Time	$t_{d(off)}$	—	17.6	—		
Fall Time	t_f	—	9.5	—		

- Notes:
- Device mounted on 2 oz. 1" x 1" Copper pads on 2" x 2" FR-4 PCB.
 - Pulse width $\leq 10\mu\text{s}$, Duty Cycle $\leq 1\%$.
 - Short duration pulse test used to minimize self-heating effect.

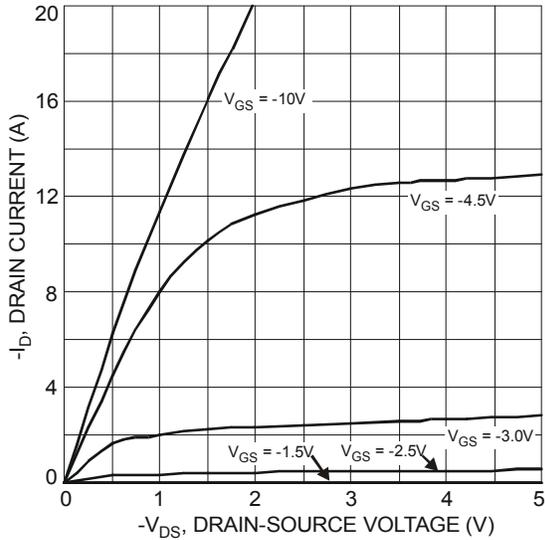


Fig. 1 Typical Output Characteristics

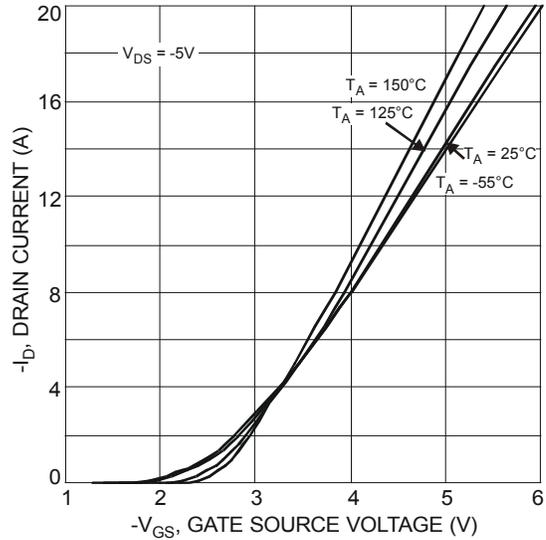


Fig. 2 Typical Transfer Characteristics

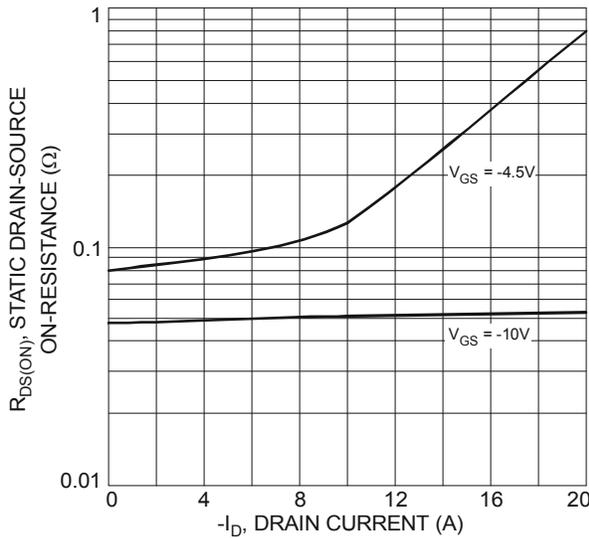


Fig. 3 Typical On-Resistance vs. Drain Current and Gate Voltage

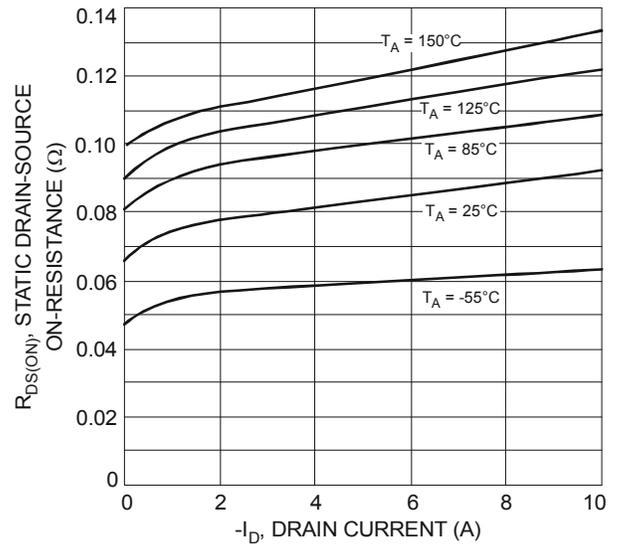


Fig. 4 Typical On-Resistance vs. Drain Current and Temperature

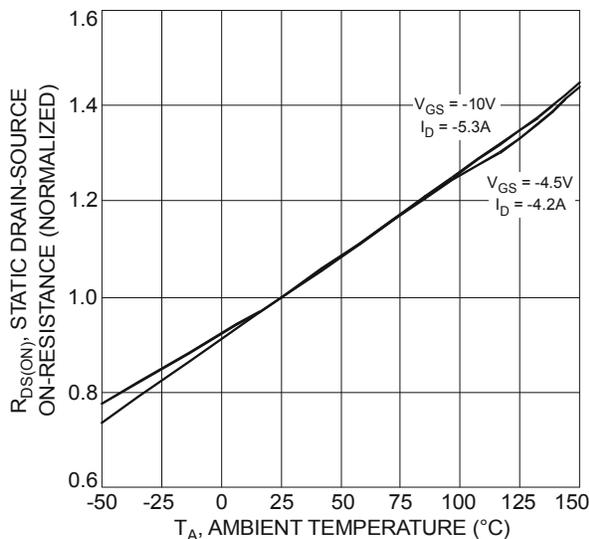


Fig. 5 On-Resistance Variation with Temperature

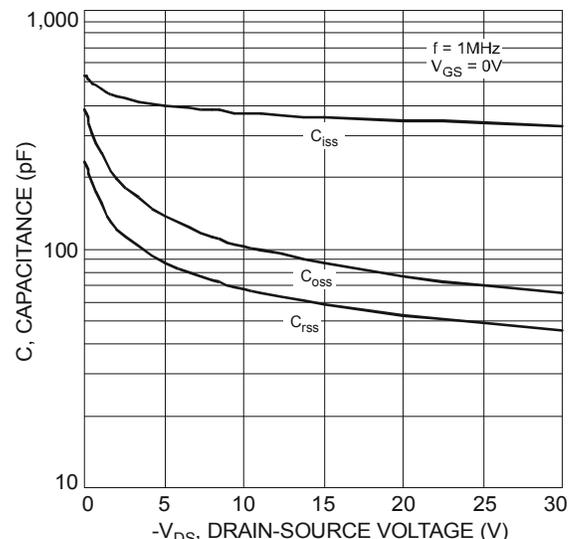


Fig. 6 Typical Capacitance

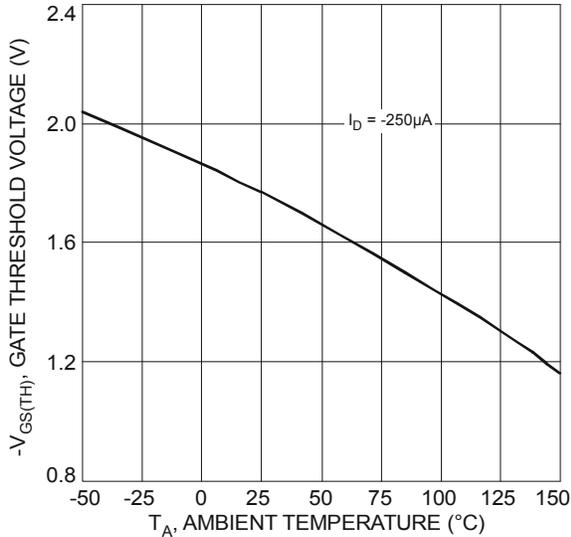


Fig. 7 Gate Threshold Variation vs. Ambient Temperature

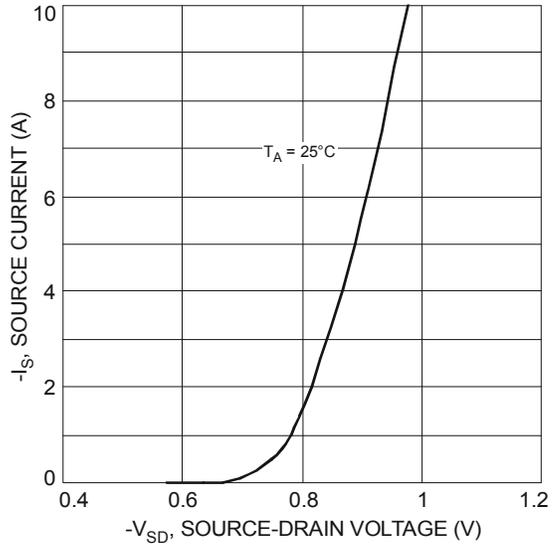
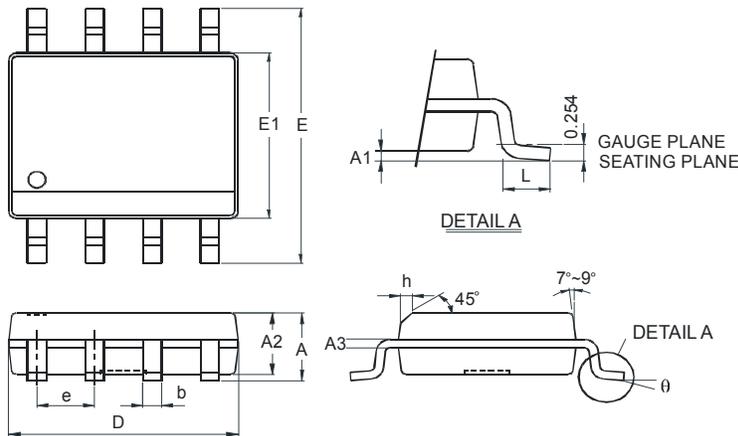


Fig. 8 Diode Forward Voltage vs. Current

Package Outline Dimensions

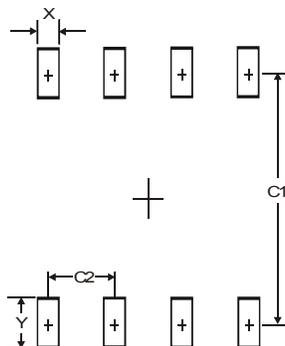
Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for latest version.



SO-8		
Dim	Min	Max
A	-	1.75
A1	0.10	0.20
A2	1.30	1.50
A3	0.15	0.25
b	0.3	0.5
D	4.85	4.95
E	5.90	6.10
E1	3.85	3.95
e	1.27 Typ	
h	-	0.35
L	0.62	0.82
θ	0°	8°
All Dimensions in mm		

Suggested Pad Layout

Please see AP02001 at <http://www.diodes.com/datasheets/ap02001.pdf> for the latest version.



Dimensions	Value (in mm)
X	0.60
Y	1.55
C1	5.4
C2	1.27

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