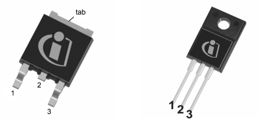
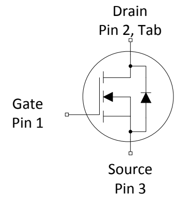
MOSFET

600V CoolMOS™ CE Power Transistor

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. CoolMOS™ CE is a price-performance optimized platform enabling to target cost sensitive applications in Consumer and Lighting markets by still meeting highest efficiency standards. The new series provides all benefits of a fast switching Superjunction MOSFET while not sacrificing ease of use and offering the best cost down performance ratio available on the market.

DPAK PG-TO 220 FP





Features

- Extremely low losses due to very low FOM Rdson*Qg and Eoss
- Very high commutation ruggedness
- Easy to use/drive
- Pb-free plating, Halogen free mold compound
- Qualified for standard grade applications

Applications

PFC stages, hard switching PWM stages and resonant switching stages for e.g. PC Silverbox, Adapter, LCD & PDP TV and indoor lighting.

Please note: Note1: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.
*Note2: *6R800CE is Full PAK marking only*

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS} @ $T_{j,max}$	650	V
$R_{DS(on),max}$	800	mΩ
Id.	8.4	A
$Q_{g.typ}$	17.2	nC
$I_{D,pulse}$	15.7	A
E_{oss}@400V	1.6	µJ

Type / Ordering Code	Package	Marking	Related Links
IPD60R800CE	PG-TO 252	60S800CE / 6R800CE*	see Appendix A
IPA60R800CE	PG-TO 220 FullPAK		

Table of Contents

1 Maximum ratings

at T_j = 25°C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1]	I_D	- -	- -	8.4 5.3	A	T_C=25°C T_C=100°C
Pulsed drain current[2]	$I_{D,pulse}$	-	-	15.7	A	T_C=25°C
Avalanche energy, single pulse	E_{AS}	-	-	72	mJ	I_D=1A; V_{DD}=50V; see table 11
Avalanche energy, repetitive	E_{AR}	-	-	0.17	mJ	I_D=1A; V_{DD}=50V; see table 11
Avalanche current, repetitive	I_{AR}	-	-	1.0	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	50	V/ns	V_{DS}=0...480V
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC (f>1 Hz)
Power dissipation (Non FullPAK) TO-252	P_{tot}	-	-	74	W	T_C=25°C
Storage temperature	T_{stg}	-40	-	150	°C	-
Operating junction temperature	T_j	-40	-	150	°C	-
Continuous diode forward current	I_S	-	-	5.9	A	T_C=25°C
Diode pulse current[2]	$I_{S,pulse}$	-	-	15.7	A	T_C=25°C
Reverse diode dv/dt[3]	dv/dt	-	-	15	V/ns	V_{DS}=0...400V, I_{SD}<=I_S, T_j=25°C see table 9
Maximum diode commutation speed	di_f/dt	-	-	500	A/µs	V_{DS}=0...400V, I_{SD}<=I_S, T_j=25°C see table 9
Power dissipation (FullPAK) TO-220FP	P_{tot}	-	-	27	W	T_C=25°C
Mounting torque (FullPAK) TO-220FP	-	-	-	50	Ncm	M2.5 screws
Insulation withstand voltage for TO-220FP	V_{ISO}	-	-	2500	V	V_{rms}, T_C=25°C, t=1min

2 Thermal characteristics

Table 3 Thermal characteristics (FullPAK) TO-220FP

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	4.6	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	80	°C/W	leaded
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	-	-	260	°C	1.6mm (0.063 in.) from case for 10s

[1] Limited by $T_{j\,max}$. TO252 equivalent,Maximum duty cycle D=0.50
[2] Pulse width t_p limited by $T_{j,max}$
[3] Identical low side and high side switch with identical R_G

Table 4 Thermal characteristics TO-252

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	1.70	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	62	°C/W	device on PCB, minimal footprint
Thermal resistance, junction - ambient for SMD version	R_{thJA}	-	35	45	°C/W	Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm² (one layer, 70µm thickness) copper area for drain connection and cooling. PCB is vertical without air stream cooling.
Soldering temperature, wave & reflow soldering allowed	T_{sold}	-	-	260	°C	reflow MSL3

3 Electrical characteristics

at T_j=25°C, unless otherwise specified

Table 5 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	600	-	-	V	V_{GS}=0V, I_D=0.25mA
Gate threshold voltage	$V_{(GS)th}$	2.5	3.0	3.5	V	V_{DS}=V_{GS}, I_D=0.17mA
Zero gate voltage drain current	I_{DSS}	- -	- 10	1 -	µA	V_{DS}=600, V_{GS}=0V, T_j=25°C V_{DS}=600, V_{GS}=0V, T_j=150°C
Gate-source leakage current	I_{GSS}	-	-	100	nA	V_{GS}=20V, V_{DS}=0V
Drain-source on-state resistance	$R_{DS(on)}$	- -	0.68 1.76	0.80 -	Ω	V_{GS}=10V, I_D=2A, T_j=25°C V_{GS}=10V, I_D=2A, T_j=150°C
Gate resistance	R_G	-	11	-	Ω	f=1MHz, open drain

Table 6 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	373	-	pF	V_{GS}=0V, V_{DS}=100V, f=1MHz
Output capacitance	C_{oss}	-	27	-	pF	V_{GS}=0V, V_{DS}=100V, f=1MHz
Effective output capacitance, energy related[1]	$C_{o(er)}$	-	18	-	pF	V_{GS}=0V, V_{DS}=0...480V
Effective output capacitance, time related[2]	$C_{o(tr)}$	-	74	-	pF	I_D=constant, V_{GS}=0V, V_{DS}=0...480V
Turn-on delay time	$t_{d(on)}$	-	9	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=2.5A, R_G=6.8Ω; see table 10
Rise time	t_r	-	7	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=2.5A, R_G=6.8Ω; see table 10
Turn-off delay time	$t_{d(off)}$	-	50	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=2.5A, R_G=6.8Ω; see table 10
Fall time	t_f	-	12	-	ns	V_{DD}=400V, V_{GS}=13 V, I_D=2.5A, R_G=6.8Ω; see table 10

Table 7 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	2	-	nC	V_{DD}=480V, I_D=2.5A, V_{GS}=0 to 10V
Gate to drain charge	Q_{gd}	-	8.9	-	nC	V_{DD}=480V, I_D=2.5A, V_{GS}=0 to 10V
Gate charge total	Q_g	-	17.2	-	nC	V_{DD}=480V, I_D=2.5A, V_{GS}=0 to 10V
Gate plateau voltage	$V_{plateau}$	-	5.4	-	V	V_{DD}=480V, I_D=2.5A, V_{GS}=0 to 10V

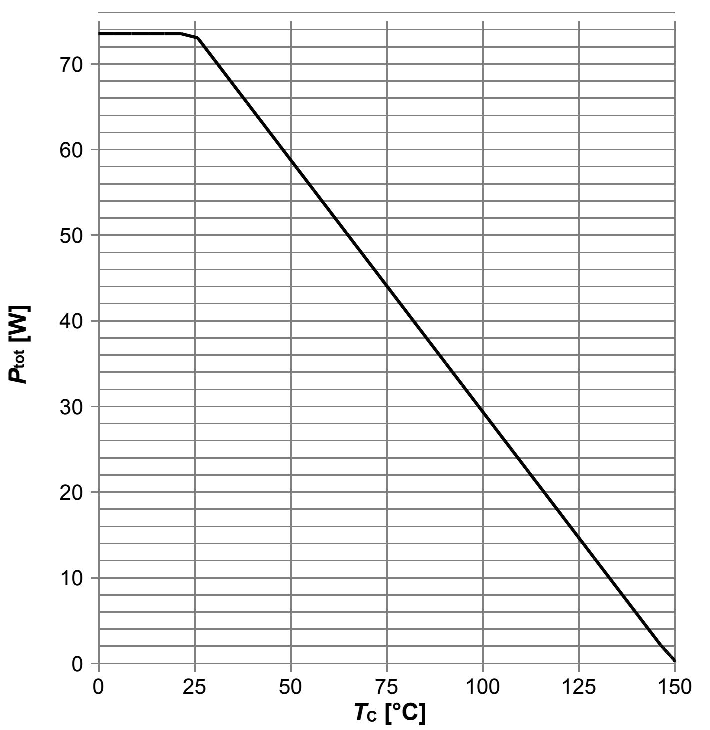
[1] $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% $V_{o(BR)DSS}$
[2] $C_{o(tr)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% $V_{o(BR)DSS}$

Table 8 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.9	-	V	V_{GS}=0V, I_F=2.5A, T_j=25°C
Reverse recovery time	t_{rr}	-	250	-	ns	V_R=400V, I_F=2.5A, di_F/dt=100A/µs; see table 9
Reverse recovery charge	Q_{rr}	-	1.8	-	µC	V_R=400V, I_F=2.5A, di_F/dt=100A/µs; see table 9
Peak reverse recovery current	I_{rrm}	-	16	-	A	V_R=400V, I_F=2.5A, di_F/dt=100A/µs; see table 9

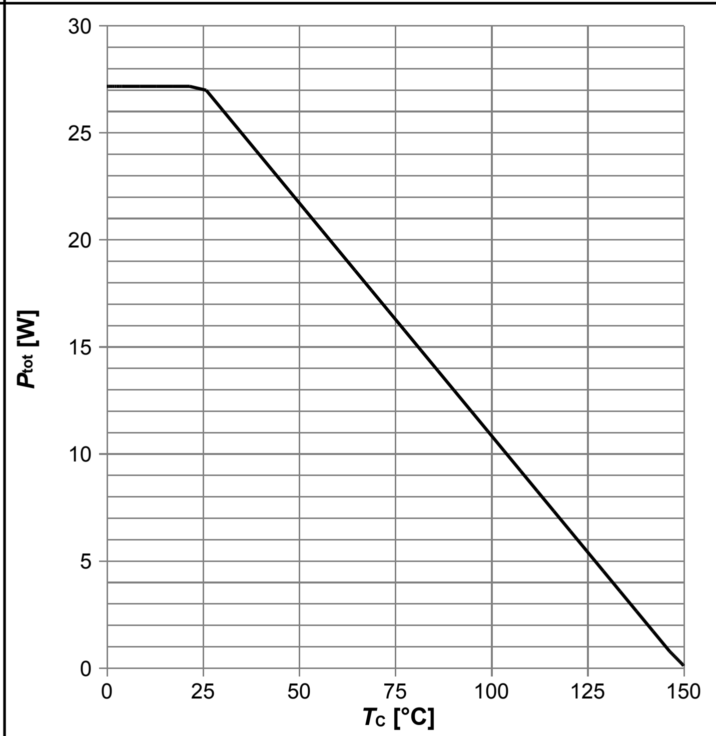
4 Electrical characteristics diagrams

Diagram 1: Power dissipation (Non FullPAK)



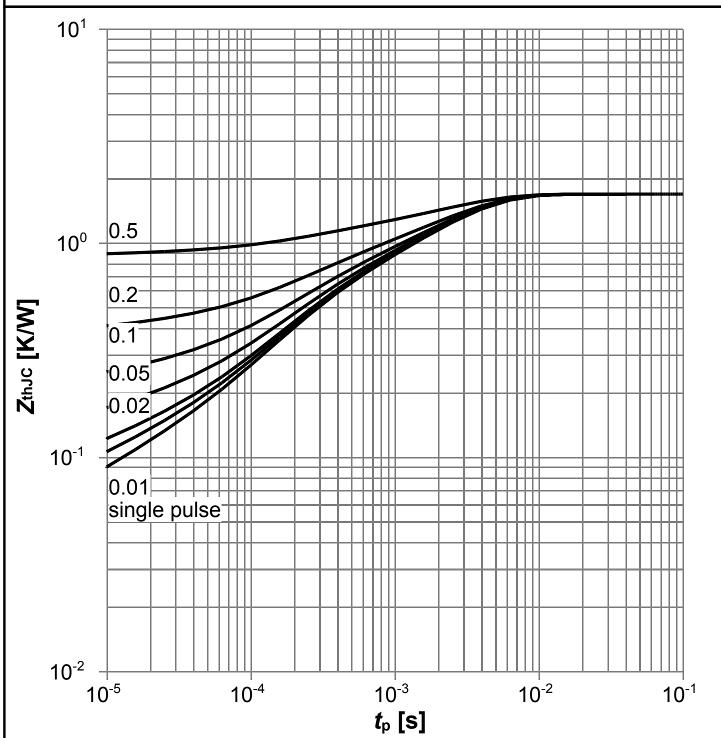
P_{tot}=f(T_C)

Diagram 2: Power dissipation (FullPAK)



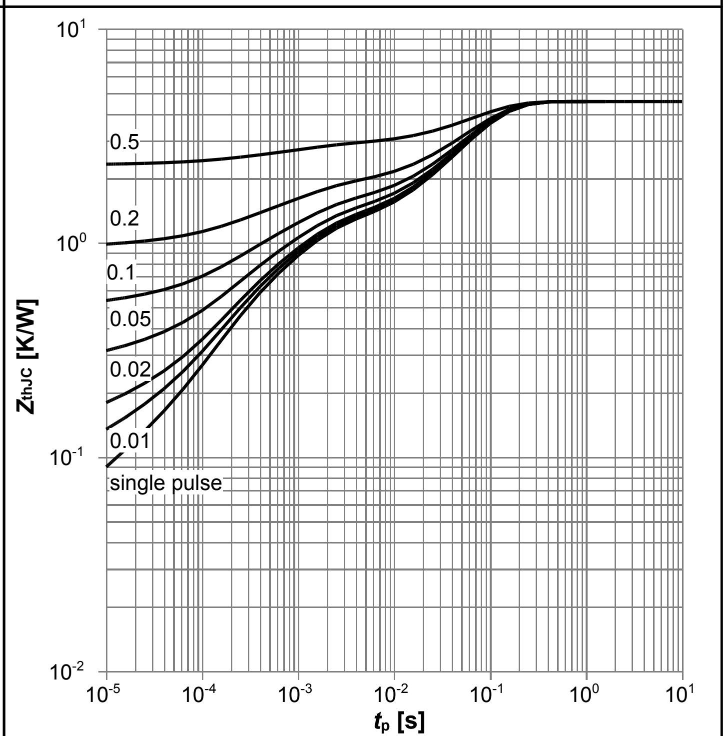
P_{tot}=f(T_C)

Diagram 3: Max. transient thermal impedance (Non FullPAK)



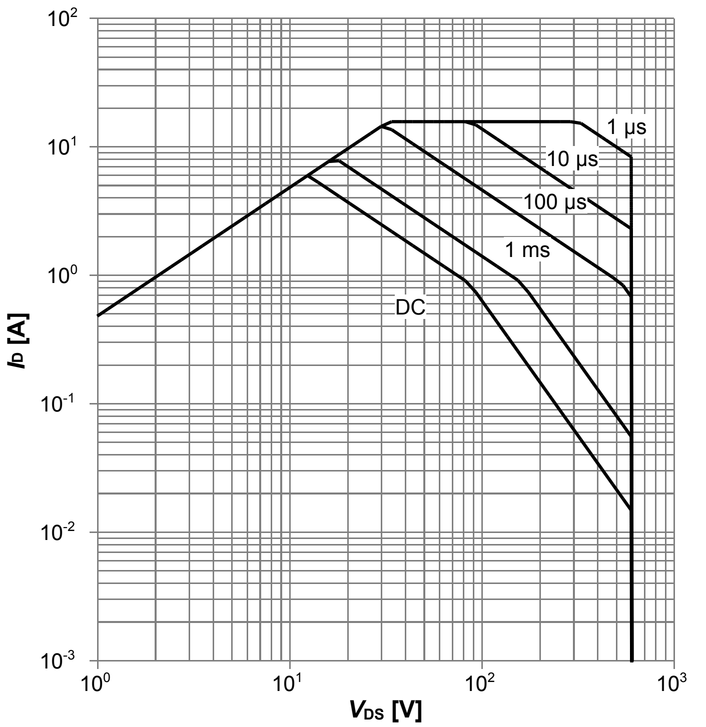
Z_{thJC} =f(t_P); parameter: D=t_p/T

Diagram 4: Max. transient thermal impedance (FullPAK)



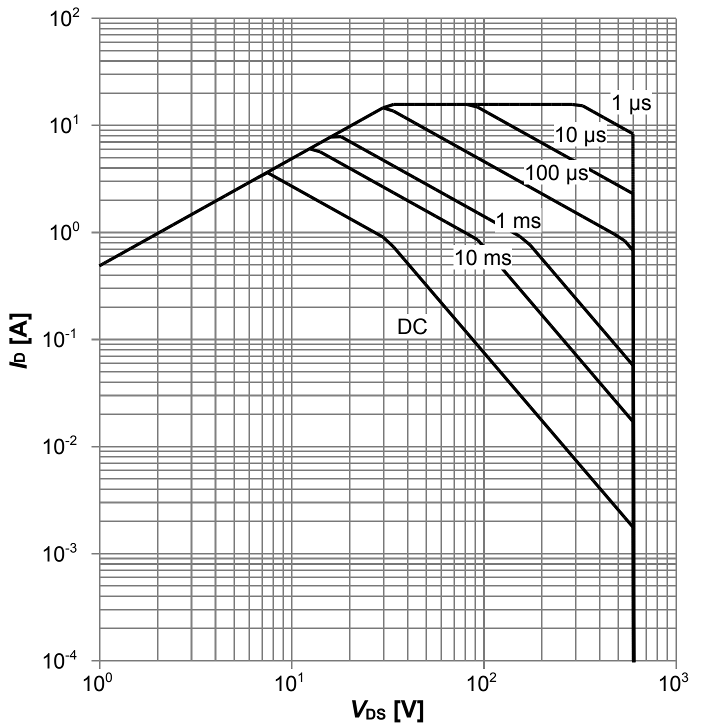
Z_{thJC} =f(t_P); parameter: D=t_p/T

Diagram 5: Safe operating area (Non FullPAK)



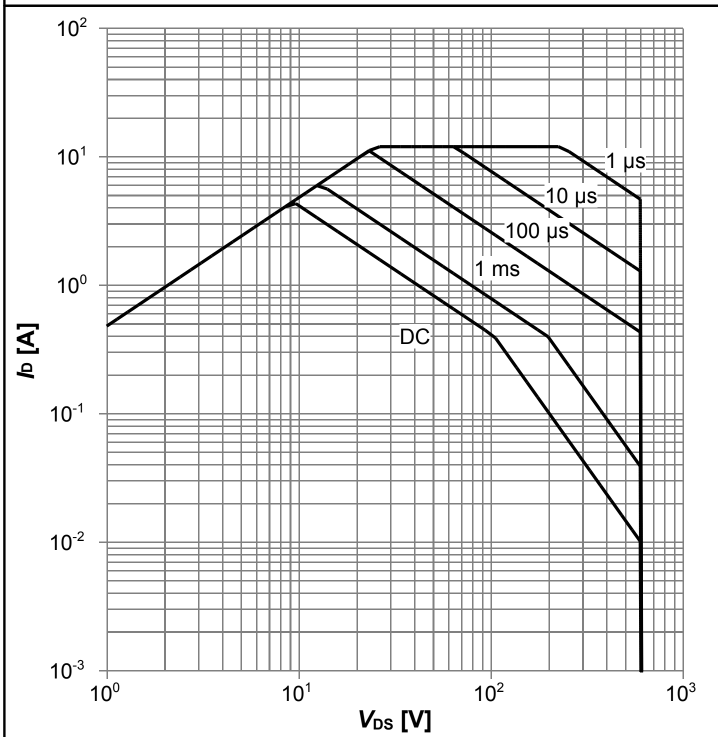
$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$; parameter: t_p

Diagram 6: Safe operating area (FullPAK)



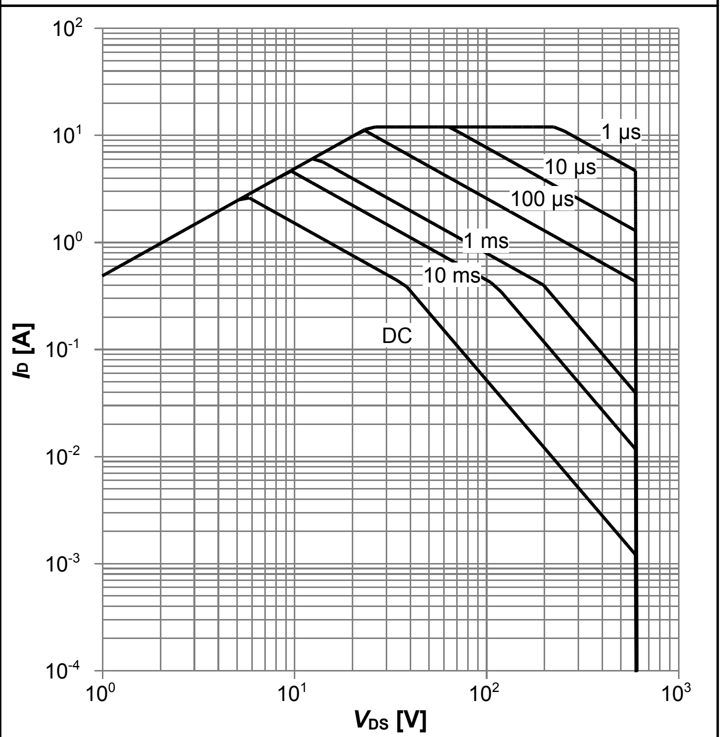
$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$; parameter: t_p

Diagram 7: Safe operating area (Non FullPAK)



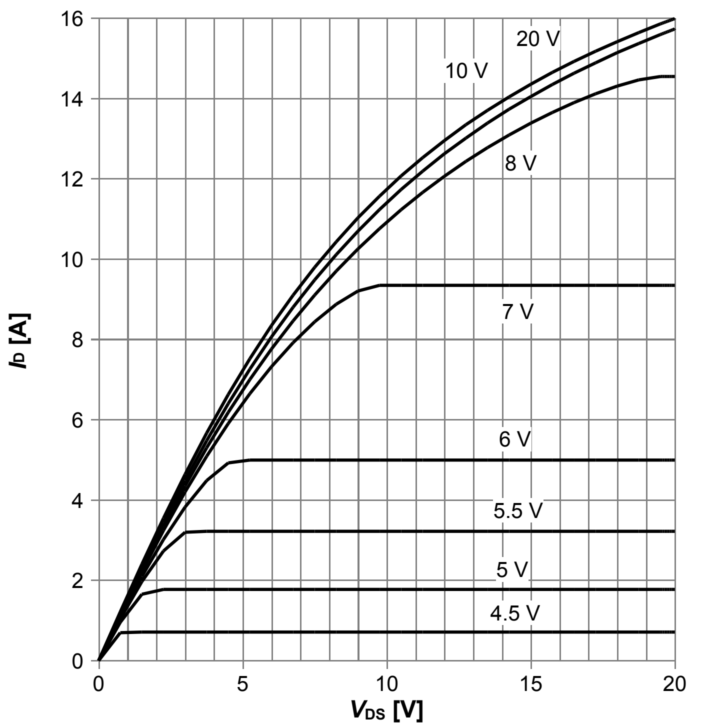
$I_D=f(V_{DS})$; $T_C=80$ °C; $D=0$; parameter: t_p

Diagram 8: Safe operating area (FullPAK)



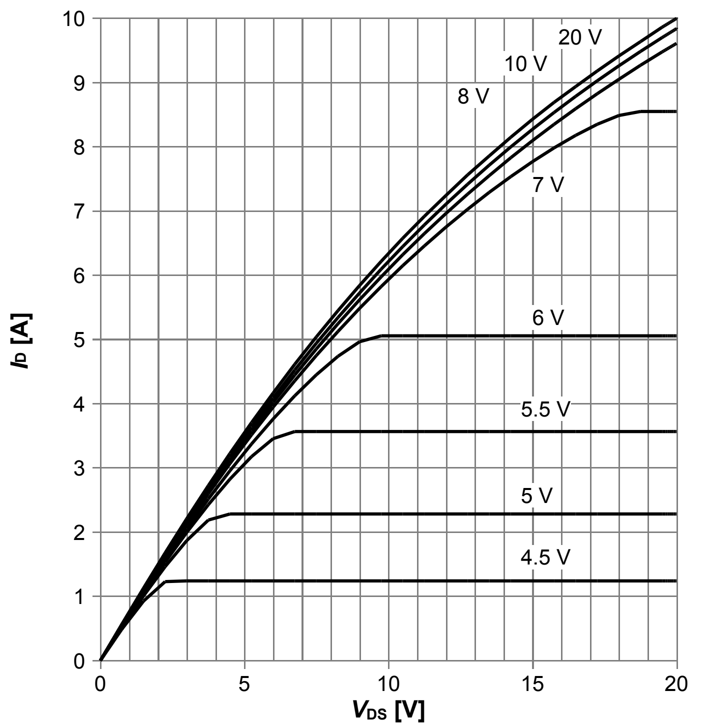
$I_D=f(V_{DS})$; $T_C=80$ °C; $D=0$; parameter: t_p

Diagram 9: Typ. output characteristics



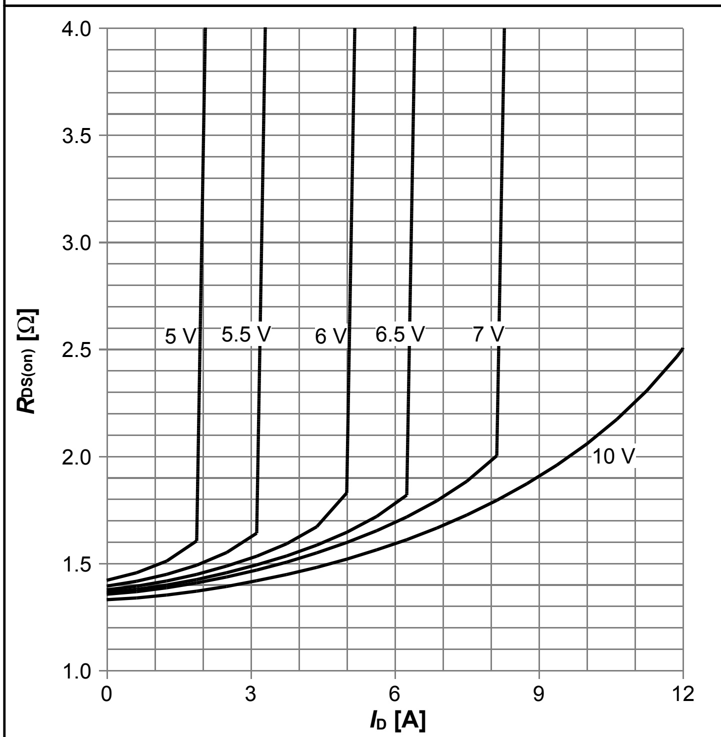
I_D=f(V_{DS}); T_j=25 °C; parameter: V_{GS}

Diagram 10: Typ. output characteristics



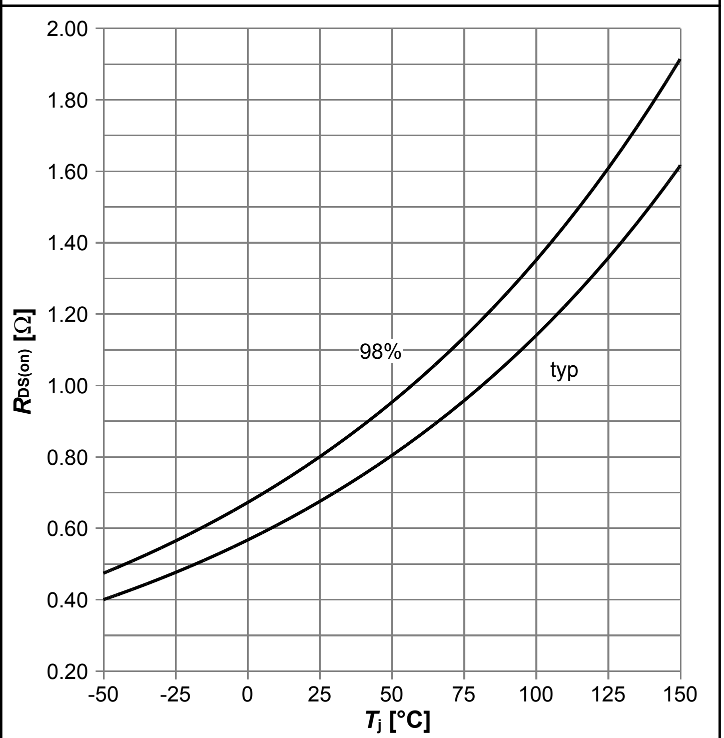
I_D=f(V_{DS}); T_j=125 °C; parameter: V_{GS}

Diagram 11: Typ. drain-source on-state resistance



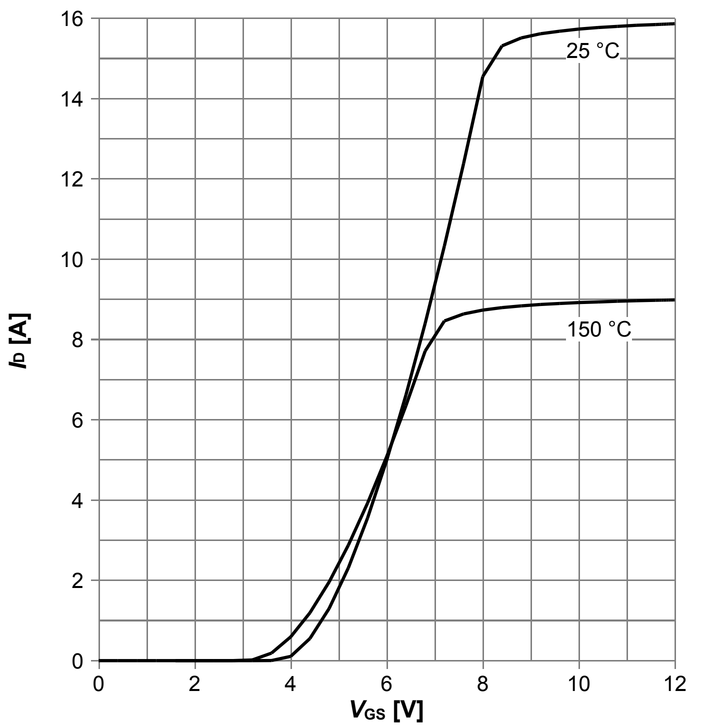
$R_{DS(on)}$=f(I_D); T_j=125 °C; parameter: V_{GS}

Diagram 12: Drain-source on-state resistance



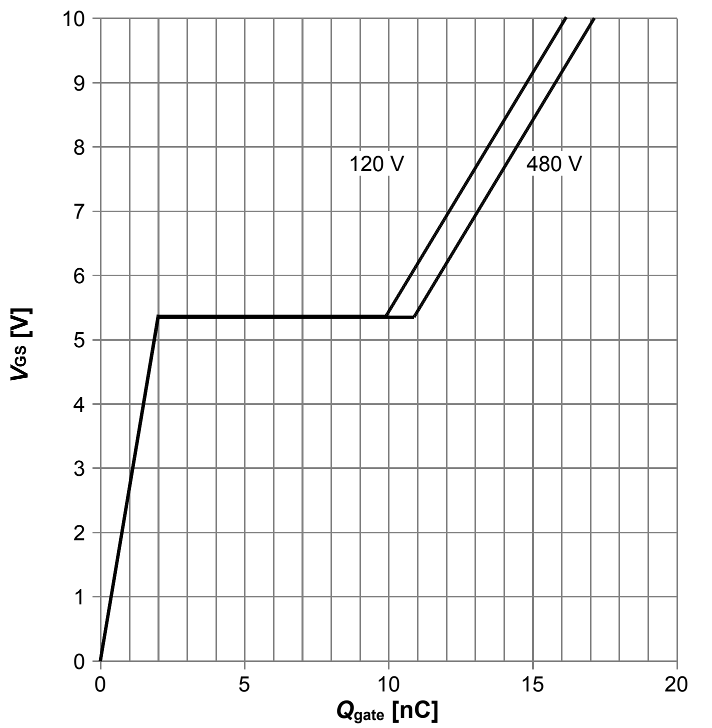
$R_{DS(on)}$=f(T_j); I_D=2.0 A; V_{GS}=10 V

Diagram 13: Typ. transfer characteristics



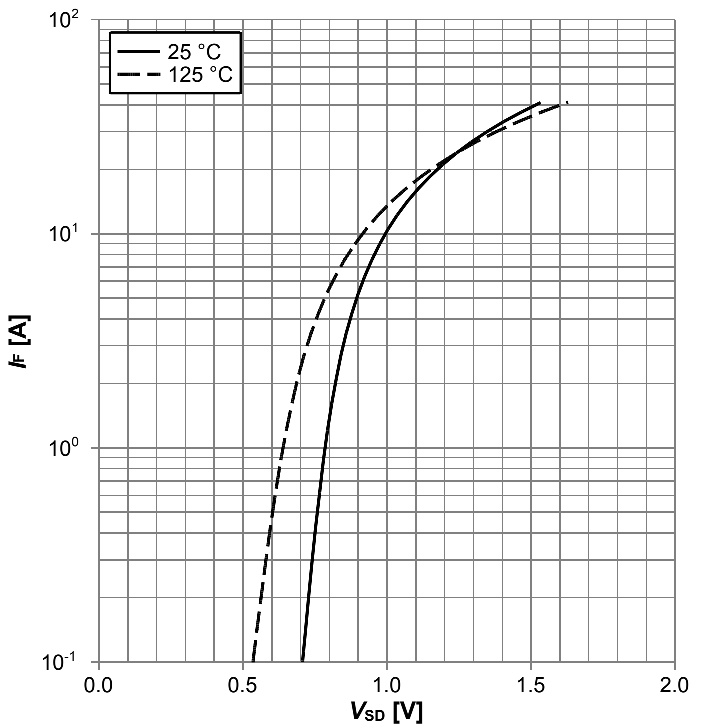
I_D=f(V_{GS}); V_{DS}=20V; parameter: T_j

Diagram 14: Typ. gate charge



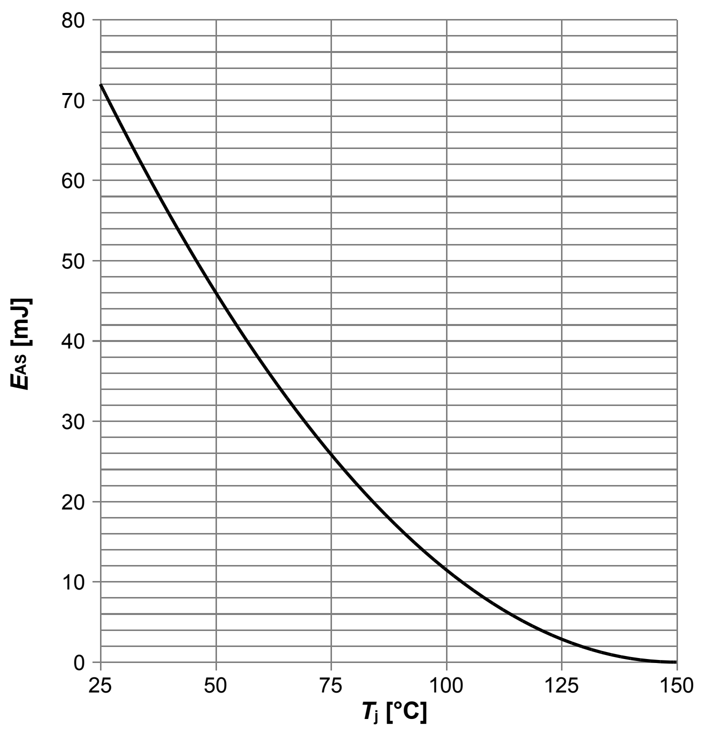
V_{GS}=f(Q_{gate}); I_D=2.5 A pulsed; parameter: V_{DD}

Diagram 15: Forward characteristics of reverse diode



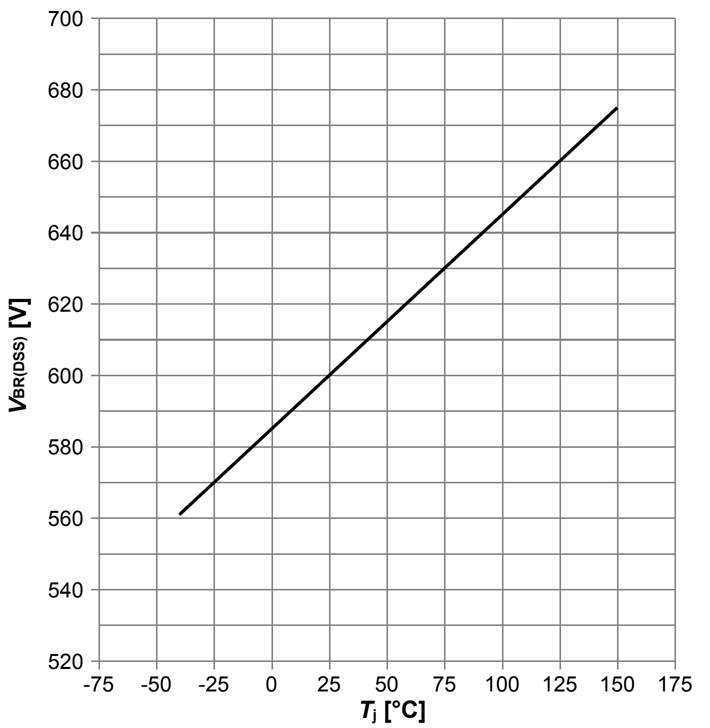
I_F=f(V_{SD}); parameter: T_j

Diagram 16: Avalanche energy



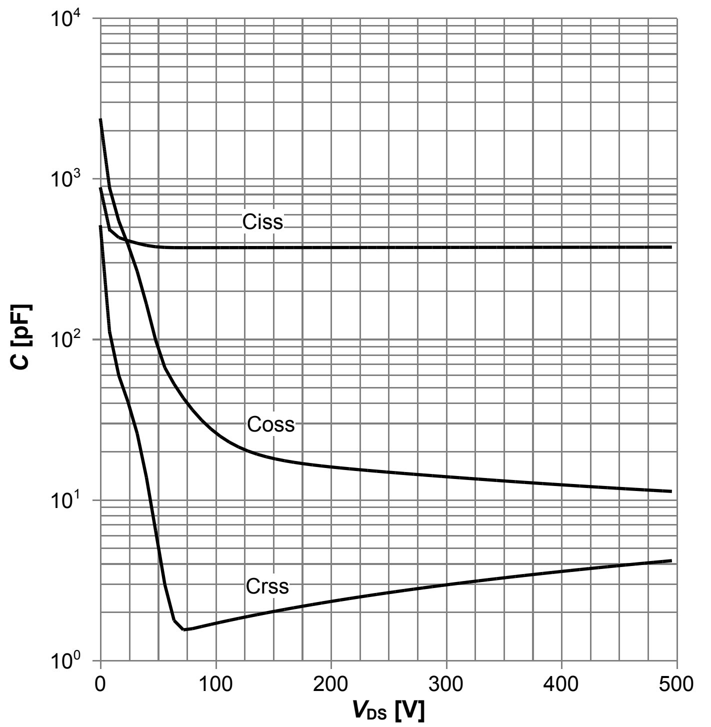
E_{AS}=f(T_j); I_D=1.0 A; V_{DD}=50 V

Diagram 17: Drain-source breakdown voltage



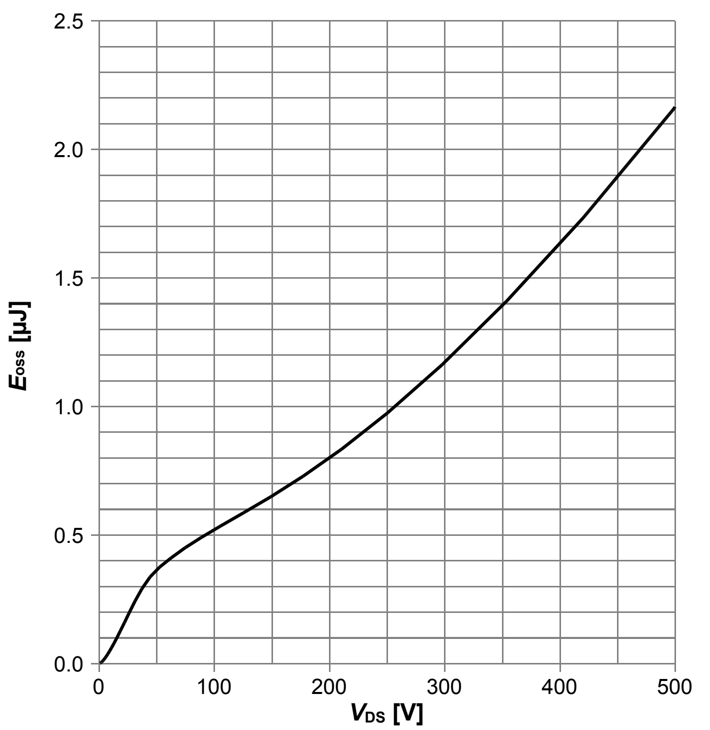
$V_{BR(DSS)}$=f(T_j); I_D=0.25 mA

Diagram 18: Typ. capacitances



C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 19: Typ. Coss stored energy



E_{oss}=f(V_{DS})

5 Test Circuits

Table 9 Diode characteristics

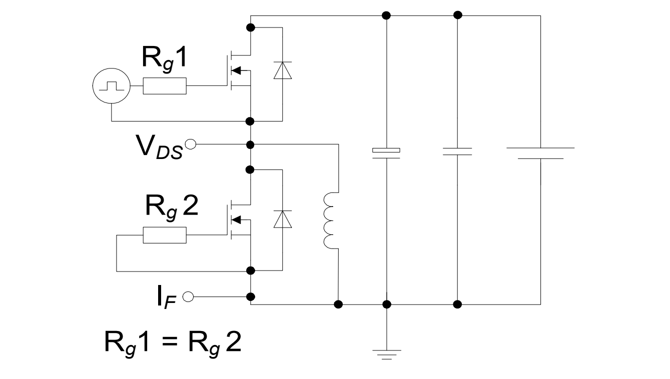
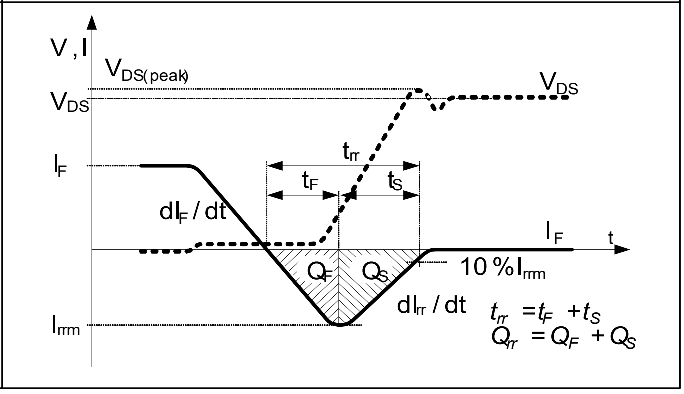
Test circuit for diode characteristics	Diode recovery waveform
	

Table 10 Switching times

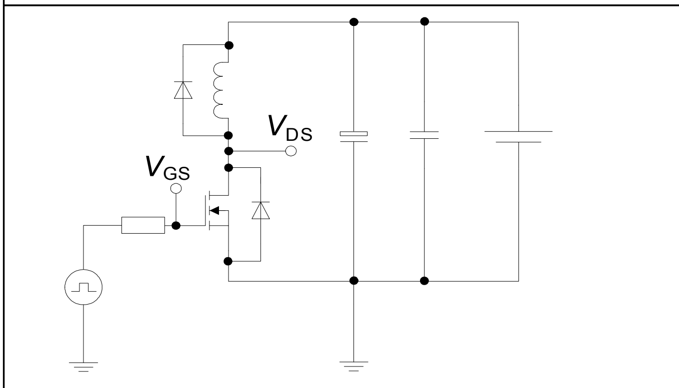
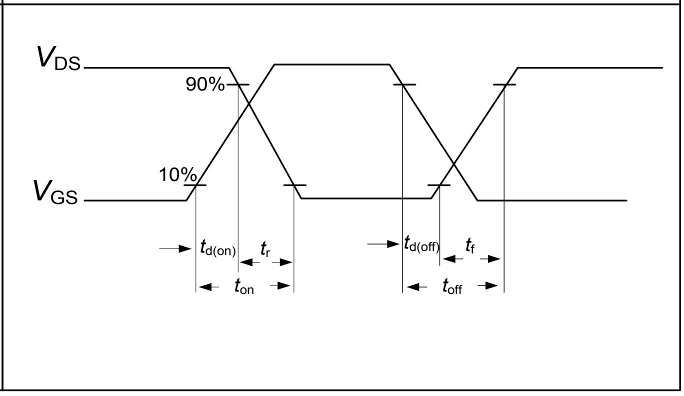
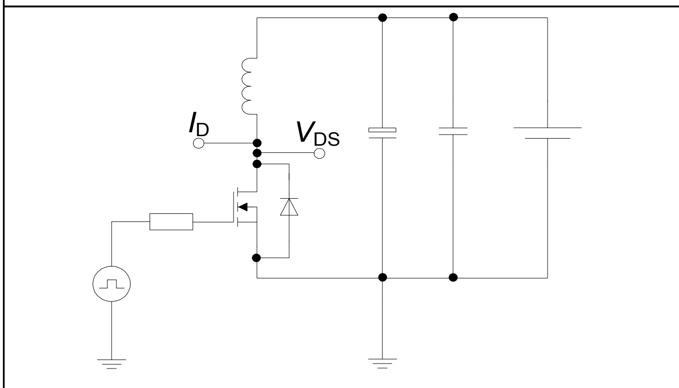
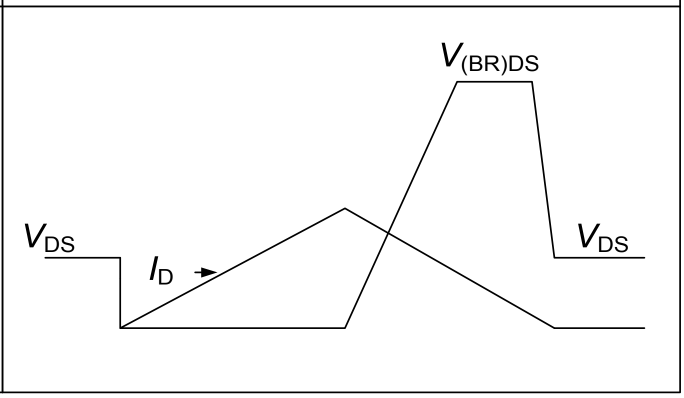
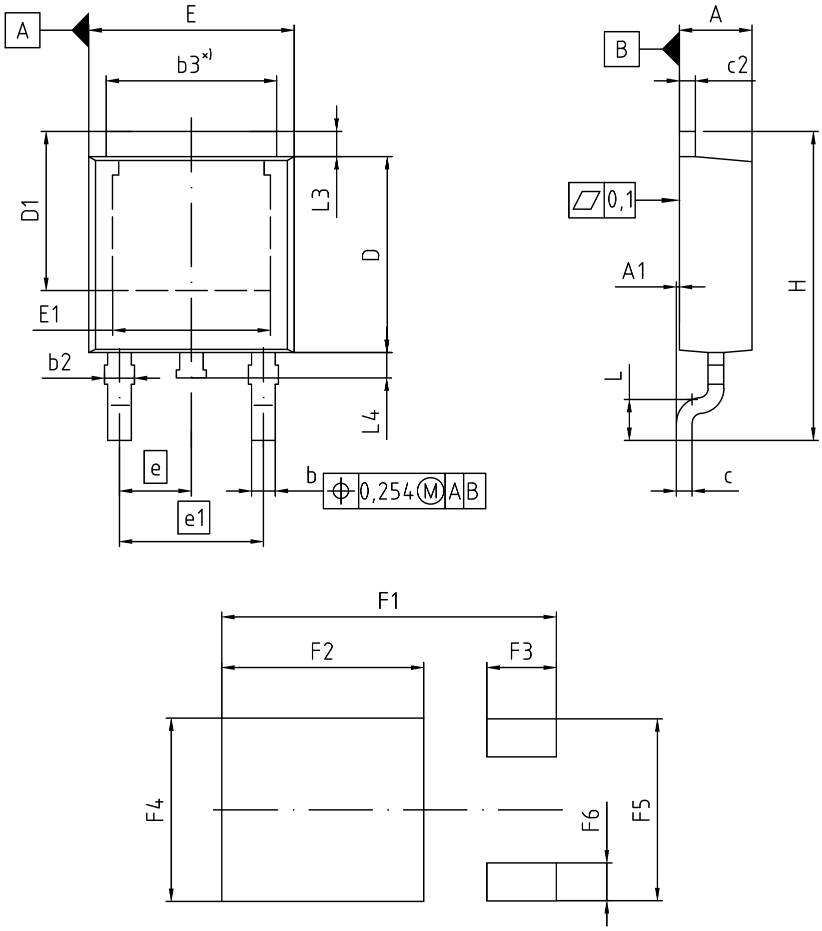
Switching times test circuit for inductive load	Switching times waveform
	

Table 11 Unclamped inductive load

Unclamped inductive load test circuit	Unclamped inductive waveform
	

6 Package Outlines

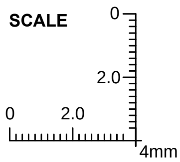


*) mold flash not included

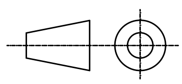
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.16	2.41	0.085	0.095
A1	0.00	0.15	0.000	0.006
b	0.64	0.89	0.025	0.035
b2	0.65	1.15	0.026	0.045
b3	5.00	5.50	0.197	0.217
c	0.46	0.60	0.018	0.024
c2	0.46	0.98	0.018	0.039
D	5.97	6.22	0.235	0.245
D1	5.02	5.84	0.198	0.230
E	6.40	6.73	0.252	0.265
E1	4.70	5.60	0.185	0.220
e	2.29 (BSC)		0.090 (BSC)	
e1	4.57 (BSC)		0.180 (BSC)	
N	3		3	
H	9.40	10.48	0.370	0.413
L	1.18	1.70	0.046	0.067
L3	0.90	1.25	0.035	0.049
L4	0.51	1.00	0.020	0.039
F1	10.60		0.417	
F2	6.40		0.252	
F3	2.20		0.087	
F4	5.80		0.228	
F5	5.76		0.227	
F6	1.20		0.047	

DOCUMENT NO.
Z8B00003328

SCALE



EUROPEAN PROJECTION



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01-09-2015

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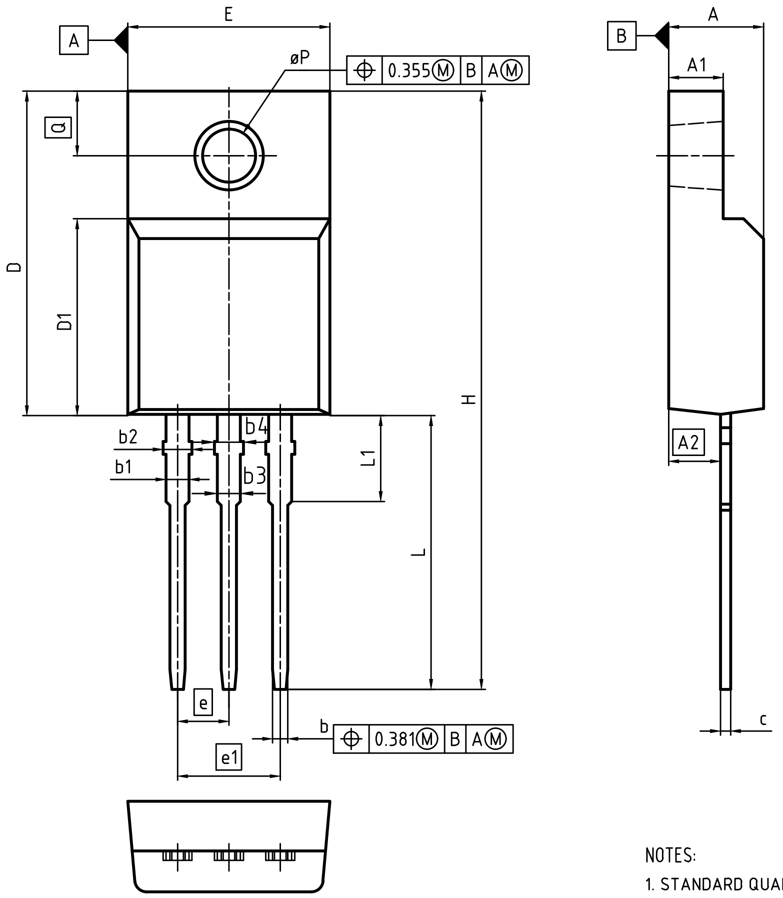
05

Figure 1 Outline PG-TO 252, dimensions in mm/inches



NOTES:
1. STANDARD QUALITY GRADE
2. ALL DIMENSIONS REFER TO JEDEC STANDARD TO-281 NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS

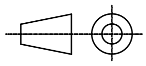
DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.50	4.90	0.177	0.193
A1	2.34	2.80	0.092	0.110
A2	2.42	2.86	0.095	0.113
b	0.65	0.90	0.026	0.035
b1	0.95	1.38	0.037	0.054
b2	1.20	1.50	0.047	0.059
b3	0.65	1.38	0.026	0.054
b4	1.20	1.50	0.047	0.059
c	0.40	0.63	0.016	0.025
D	15.67	16.15	0.617	0.636
D1	8.97	9.83	0.353	0.387
E	10.00	10.65	0.394	0.419
e	2.54 (BSC)		0.100 (BSC)	
e1	5.08		0.200	
N	3		3	
H	28.70	29.75	1.130	1.171
L	12.78	13.75	0.503	0.541
L1	2.83	3.45	0.111	0.136
øP	3.00	3.38	0.118	0.133
Q	3.15	3.50	0.124	0.138

DOCUMENT NO.
Z8B00181328

SCALE 0 2.5 5mm

EUROPEAN PROJECTION



ISSUE DATE
29-04-2016

REVISION
01

Figure 2 Outline PG-TO 220 FullPAK, dimensions in mm/inches

7 Appendix A

Table 12 Related Links

- **IFX CoolMOS^{TM} CE Webpage:** www.infineon.com
- **IFX CoolMOS^{TM} CE application note:** www.infineon.com
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Revision History

IPD60R800CE, IPA60R800CE

Revision: 2016-08-08, Rev. 2.3

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2014-09-25	Release of final version
2.1	2016-03-31	Modified Id, Rthjc. Modified SOA and Zthjc curves
2.2	2016-05-03	Changed TO220 Full PAK package drawing
2.3	2016-08-08	Added Full PAK marking on page 1, revised Full PAK package drawing on page 14 and changed TO252 package solder reflow rating to MSL3 on page 4

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