TEXAS INSTRUMENTS

LM5022-Q1

SNVSAG9 – MARCH 2016

LM5022-Q1 2.2MHz, 60 V Low-Side Controller For Boost and SEPIC

1 Features

- AEC-Q100 Grade 1 Qualified with the following results:
  - Device Temperature Grade 1: -40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C5
- Internal 60-V Start-Up Regulator
- 1-A Peak MOSFET Gate Driver
- V_{IN} Range: 6 V to 60 V (operate down to 3 V after startup)
- Duty Cycle Limit of 90%
- Programmable UVLO with Hysteresis
- Cycle-by-Cycle Current Limit
- Single Resistor Oscillator Frequency Set
- Adjustable Switching Frequency to 2.2MHz
- External Clock Synchronization
- Slope Compensation
- Adjustable Soft Start
- 10-Pin VSSOP Package

2 Applications

- Boost Converter
- SEPIC Converter

3 Description

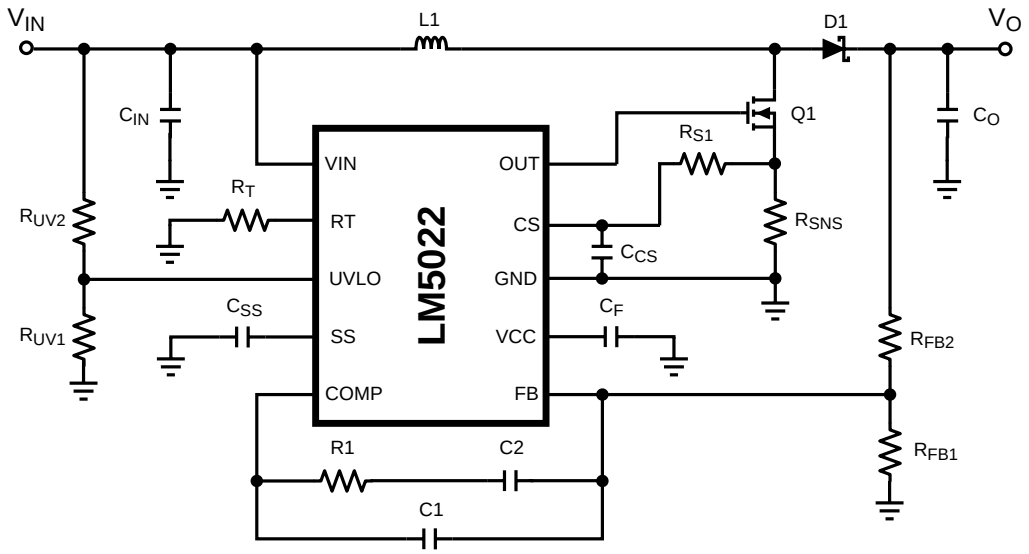
The LM5022-Q1 is a high voltage low-side N-channel MOSFET controller ideal for use in boost and SEPIC regulators. It contains all of the features needed to implement single-ended primary topologies. Output voltage regulation is based on current-mode control, which eases the design of loop compensation while providing inherent input voltage feed-forward. The LM5022-Q1 includes a start-up regulator that operates over a wide input range of 6 V to 60 V. The PWM controller is designed for high-speed capability including an oscillator frequency range up to 2.2 MHz and total propagation delays less than 100 ns. Additional features include an error amplifier, precision reference, line undervoltage lockout, cycle-by-cycle current limit, slope compensation, soft-start, external synchronization capability, and thermal shutdown. The LM5022-Q1 is available in the 10-pin VSSOP package.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM5022-Q1	VSSOP (10)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application



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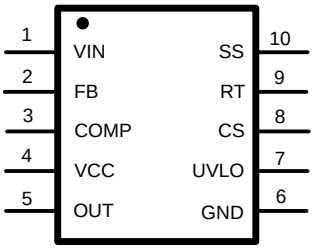
4 Revision History

DATE	REVISION	NOTES
March 2016	*	Initial release.

5 Pin Configuration and Functions

DGS Package
10-Pin VSSOP
Top View



Pin Functions

PIN		TYPE	DESCRIPTION	APPLICATION INFORMATION
NO.	NAME			
1	VIN	I	Source input voltage	Input to the start-up regulator. Operates from 6 V to 60 V.
2	FB	I	Feedback pin	Inverting input to the internal voltage error amplifier. The non-inverting input of the error amplifier connects to a 1.25-V reference.
3	COMP	I/O	Error amplifier output and PWM comparator input	The control loop compensation components connect between this pin and the FB pin.
4	VCC	O	Output of the internal, high voltage linear regulator.	This pin should be bypassed to the GND pin with a ceramic capacitor.
5	OUT	O	Output of MOSFET gate driver	Connect this pin to the gate of the external MOSFET. The gate driver has a 1-A peak current capability.
6	GND	-	System ground	
7	UVLO	I	Input undervoltage lockout	Set the start-up and shutdown levels by connecting this pin to the input voltage through a resistor divider. A 20-µA current source provides hysteresis.
8	CS	I	Current sense input	Input for the switch current used for current mode control and for current limiting.
9	RT/SYNC	I	Oscillator frequency adjust pin and synchronization input	An external resistor connected from this pin to GND sets the oscillator frequency. This pin can also accept an AC-coupled input for synchronization from an external clock.
10	SS	I	Soft-start pin	An external capacitor placed from this pin to ground will be charged by a 10-µA current source, creating a ramp voltage to control the regulator start-up.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
VIN to GND		–0.3	65	V
VCC to GND		–0.3	16	V
RT/SYNC to GND		–0.3	5.5	V
OUT to GND		–1.5V for < 100 ns		
All other pins to GND		–0.3	7	V
Power dissipation		Internally limited		
Junction temperature(3)			150	°C
Soldering information	Vapor phase (60 sec.)		215	°C
	Infrared (15 sec.)		220	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

6.2 ESD Ratings: LM5022-Q1

		VALUE	UNIT
$V_{(ESD)}$	Human body model (HBM), per AEC Q100-002(1)	±2000	V
	Charged device model (CDM), per AEC Q100-011(2)	±750	V

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification. This is the passing level per ANSI/ESDA/JEDEC JS-001. JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process
(2) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	NOM	MAX	UNIT
Supply voltage	6		60	V
External voltage at V_{CC}	7.5		14	V
Junction temperature	–40		125	°C

(1) Operating Ratings are conditions under the device is intended to be functional. For specifications and test conditions, see *Electrical Characteristics*

6.4 Thermal Information

THERMAL METRIC(1)		LM5022-Q1 DGS (VSSOP) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	161.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	81.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	80	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Typical limits apply for T_J = 25°C and are provided for reference purposes only; minimum and maximum limits apply over the junction temperature (T_J) range of –40°C to +125°C. V_{IN} = 24 V and R_T = 27.4 kΩ, unless otherwise indicated.(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYSTEM PARAMETERS						
V_{FB}	FB Pin Voltage		1.225	1.250	1.275	V
START-UP REGULATOR						
VCC(2)	VCC Regulation	10 V ≤ V_{IN} ≤ 60 V, I_{CC} = 1 mA	6.6	7	7.4	V
	VCC Regulation	6 V ≤ V_{IN} < 10 V, VCC Pin Open Circuit	5			
I_{CC}	Supply Current	OUT Pin Capacitance = 0 VCC = 10 V		3.5	4	mA
I_{CC-LIM}	VCC Current Limit	VCC = 0 V, ((3), (2))	15	35		mA
V_{IN} - VCC	Dropout Voltage Across Bypass Switch	I_{CC} = 0 mA, f_{SW} < 200 kHz 6 V ≤ V_{IN} ≤ 8.5 V		200		mV
V_{BYP-HI}	Bypass Switch Turn-off Threshold	V_{IN} increasing		8.7		V
$V_{BYP-HYS}$	Bypass Switch Threshold Hysteresis	V_{IN} Decreasing		260		mV
Z_{VCC}	VCC Pin Output Impedance 0 mA ≤ ICC ≤ 5 mA	V_{IN} = 6 V		58		Ω
		V_{IN} = 8 V		53		
		V_{IN} = 24 V		1.6		
VCC_{-HI}	VCC Pin UVLO Rising Threshold			5		V
VCC_{-HYS}	VCC Pin UVLO Falling Hysteresis			300		mV
I_{VIN}	Start-up Regulator Leakage	V_{IN} = 60 V		150	500	µA
I_{IN-SD}	Shutdown Current	V_{UVLO} = 0 V, VCC = Open Circuit		350	450	µA
ERROR AMPLIFIER						
GBW	Gain Bandwidth			4		MHz
A_{DC}	DC Gain			75		dB
I_{COMP}	COMP Pin Current Sink Capability	V_{FB} = 1.5 V V_{COMP} = 1 V	**5**	17		mA
UVLO						
V_{SD}	Shutdown Threshold		1.22	1.25	1.28	V
I_{SD-HYS}	Shutdown Hysteresis Current Source		16	20	24	µA
CURRENT LIMIT						
$t_{LIM-DLY}$	Delay from ILIM to Output	CS steps from 0 V to 0.6 V OUT transitions to 90% of VCC		30		ns
V_{CS}	Current Limit Threshold Voltage		0.434	0.5	0.55	V
t_{BLK}	Leading Edge Blanking Time			65		ns
R_{CS}	CS Pin Sink Impedance	Blanking active		40	75	Ω
SOFT-START						
I_{SS}	Soft-start Current Source		7	10	13	µA
V_{SS-OFF}	Soft-start to COMP Offset		0.344	0.55	0.75	V

(1) All minimum and maximum limits are specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control. The junction temperature (T_J in °C) is calculated from the ambient temperature (T_A in °C) and power dissipation (P_D in Watts) as follows: $T_J = T_A + (P_D \bullet R_{\theta JA})$ where $R_{\theta JA}$ (in °C/W) is the package thermal impedance provided in the Thermal Information section.
(2) VCC provides bias for the internal gate drive and control circuits.
(3) Device thermal limitations may limit usable range.

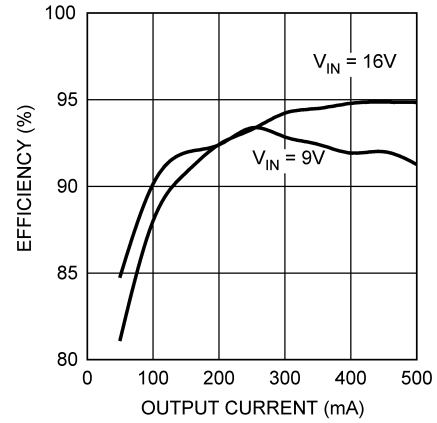
Electrical Characteristics (continued)

Typical limits apply for T_J = 25°C and are provided for reference purposes only; minimum and maximum limits apply over the junction temperature (T_J) range of –40°C to +125°C. V_{IN} = 24 V and R_T = 27.4 kΩ, unless otherwise indicated.(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OSCILLATOR						
f_{SW}	RT to GND = 84.5 kΩ	See(4)	170	200	230	kHz
	RT to GND = 27.4 kΩ	See(4)	525	600	675	kHz
	RT to GND = 16.2 kΩ	See(4)	865	990	1115	kHz
	RT to GND = 6.65 kΩ	See(4)	1910	2240	2570	kHz
$V_{SYNC-HI}$	Synchronization Rising Threshold				3.8	V
PWM COMPARATOR						
$t_{COMP-DLY}$	Delay from COMP to OUT Transition	V_{COMP} = 2 V CS stepped from 0 V to 0.4 V		25		ns
D_{MIN}	Minimum Duty Cycle	V_{COMP} = 0 V			0%	
D_{MAX}	Maximum Duty Cycle		90%	95%		
A_{PWM}	COMP to PWM Comparator Gain			0.33		V/V
$V_{COMP-OC}$	COMP Pin Open Circuit Voltage	V_{FB} = 0 V	4.3	5.2	6.1	V
$I_{COMP-SC}$	COMP Pin Short Circuit Current	V_{COMP} = 0 V, V_{FB} = 0V	0.6	1.1	1.5	mA
SLOPE COMPENSATION						
V_{SLOPE}	Slope Compensation Amplitude		83	110	137	mV
MOSFET DRIVER						
V_{SAT-HI}	Output High Saturation Voltage (VCC – VOUT)	I_{OUT} = 50 mA		0.25	0.75	V
V_{SAT-LO}	Output Low Saturation Voltage (VOUT)	I_{OUT} = 100 mA		0.25	0.75	V
t_{RISE}	OUT Pin Rise Time	OUT Pin load = 1 nF		18		ns
t_{FALL}	OUT Pin Fall Time	OUT Pin load = 1 nF		15		ns
THERMAL CHARACTERISTICS						
T_{SD}	Thermal Shutdown Threshold			165		°C
T_{SD-HYS}	Thermal Shutdown Hysteresis			25		°C

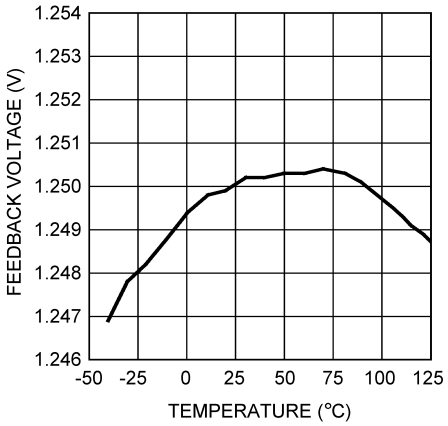
(4) Specification applies to the oscillator frequency.

6.6 Typical Characteristics



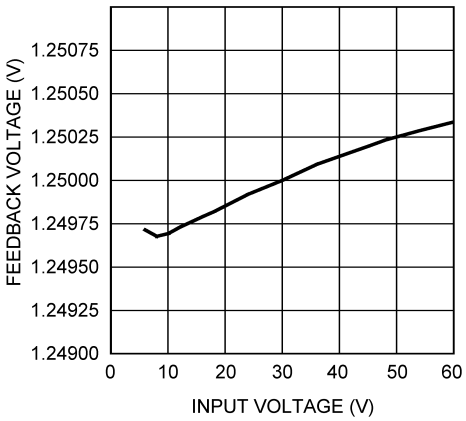
V_O = 40 V

Figure 1. Efficiency, Example Circuit BOM



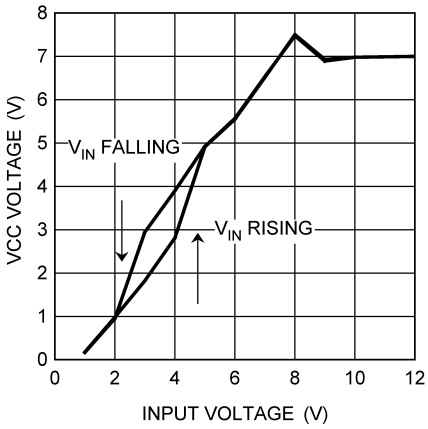
V_{IN} = 24 V

Figure 2. V_{FB} vs. Temperature



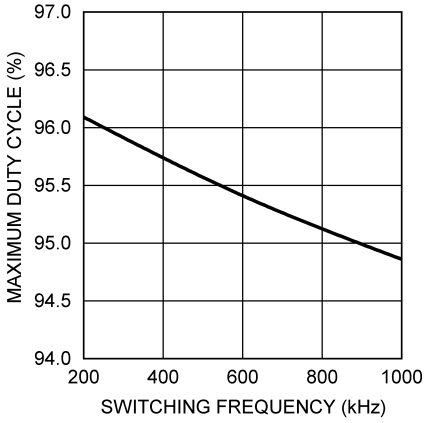
T_A = 25°C

Figure 3. V_{FB} vs. V_{IN}



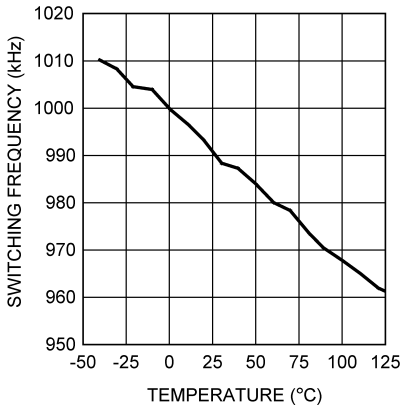
T_A = 25°C

Figure 4. V_{CC} vs. V_{IN}



T_A = 25°C

Figure 5. Maximum Duty Cycle vs. f_{SW}



R_T = 16.2 KΩ

Figure 6. f_{SW} vs. Temperature

Typical Characteristics (continued)

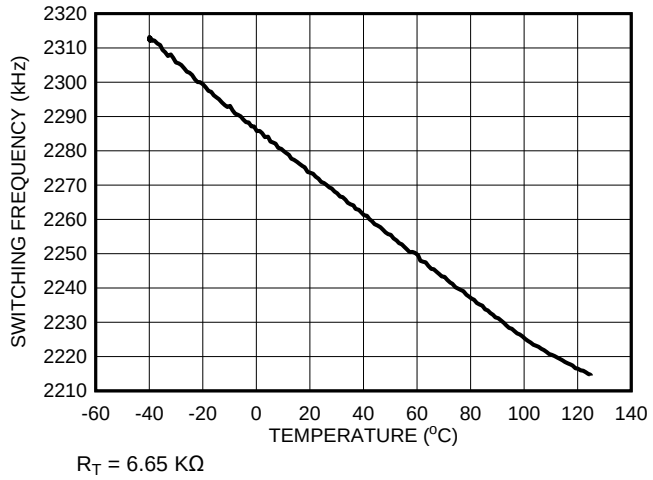


Figure 7. f_{SW} vs. Temperature

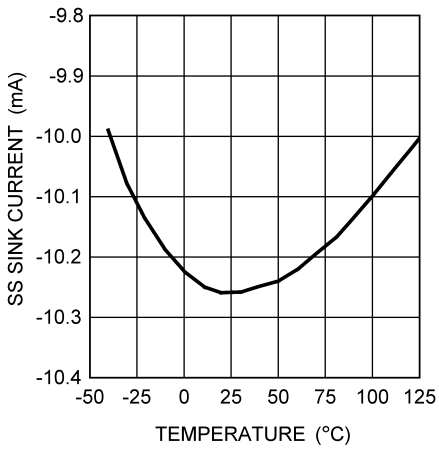


Figure 8. SS vs. Temperature

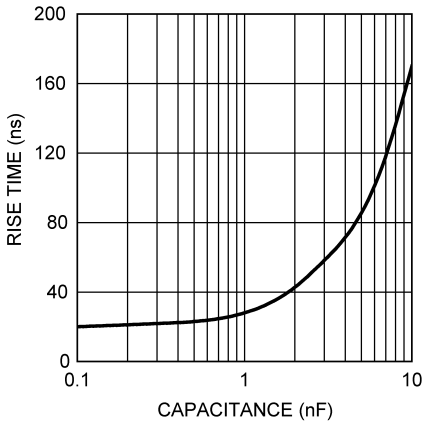


Figure 9. OUT Pin T_{RISE} vs. Gate Capacitance

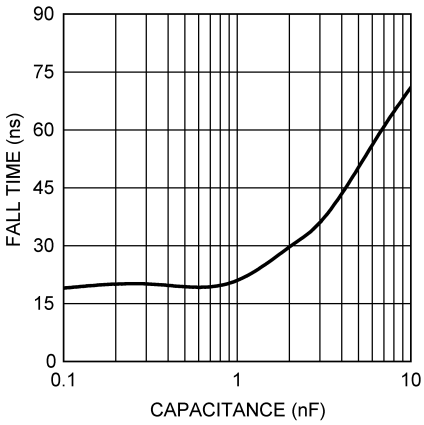


Figure 10. OUT Pin T_{FALL} vs. Gate Capacitance

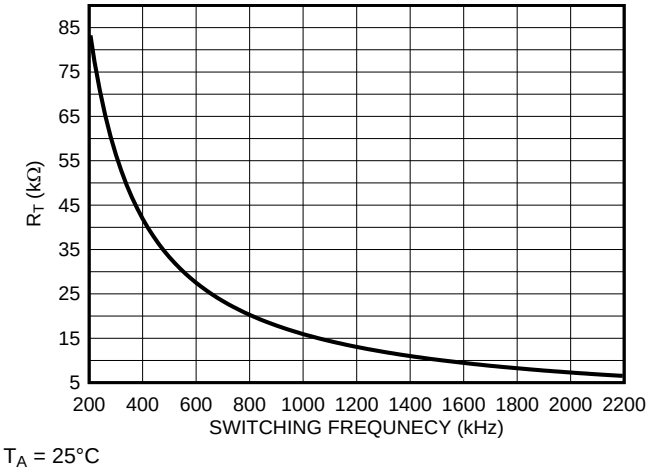


Figure 11. R_T vs. f_{SW}

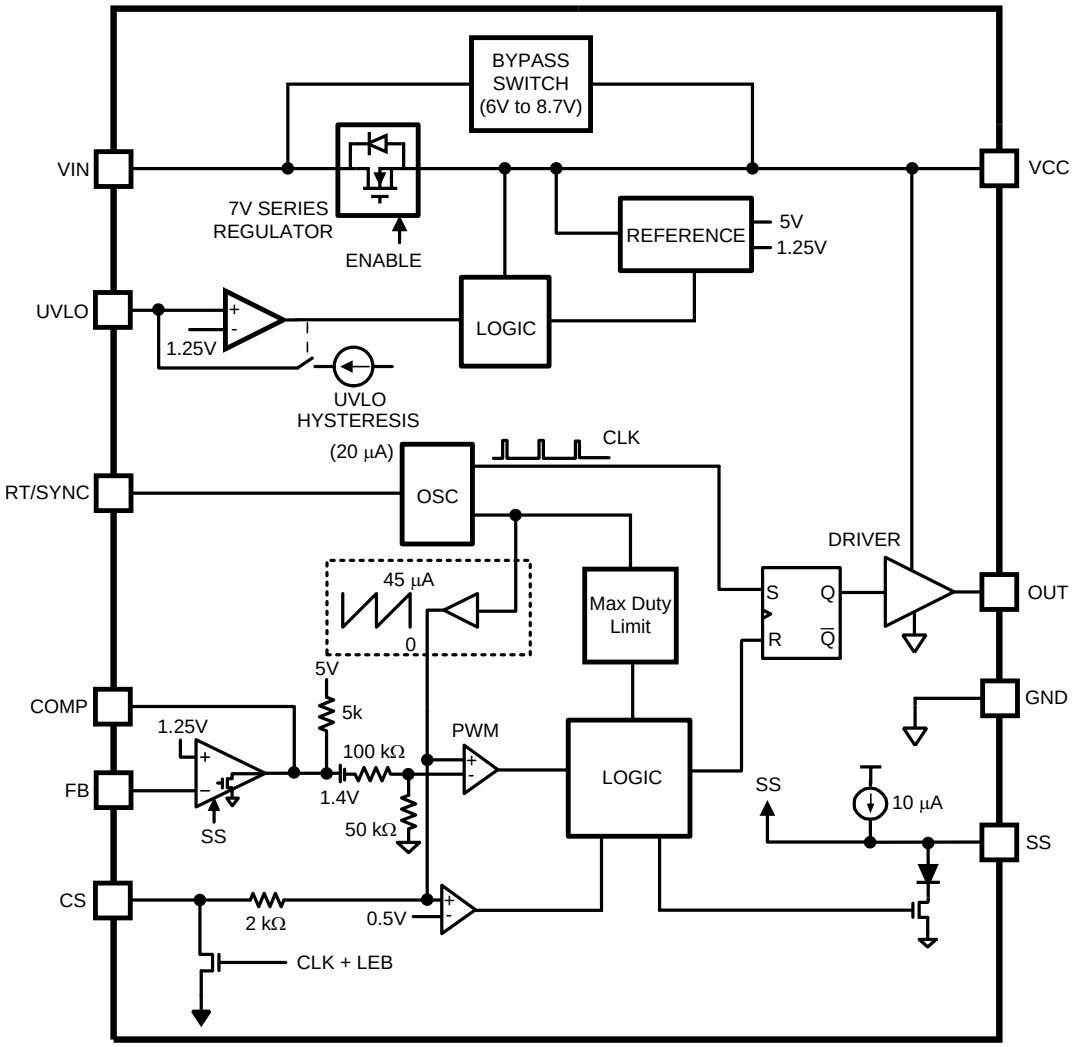
7 Detailed Description

7.1 Overview

The LM5022-Q1 is a low-side N-channel MOSFET controller that contains all of the features needed to implement single ended power converter topologies. The LM5022-Q1 includes a high-voltage startup regulator that operates over a wide input range of 6 V to 60 V. The PWM controller is designed for high speed capability including an oscillator frequency range up to 2.2 MHz and total propagation delays less than 100 ns. Additional features include an error amplifier, precision reference, input under-voltage lockout, cycle-by-cycle current limit, slope compensation, soft-start, oscillator sync capability and thermal shutdown.

The LM5022-Q1 is designed for current-mode control power converters that require a single drive output, such as boost and SEPIC topologies. The LM5022-Q1 provides all of the advantages of current-mode control including input voltage feed-forward, cycle-by-cycle current limiting and simplified loop compensation.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 High Voltage Start-Up Regulator

The LM5022-Q1 contains an internal high-voltage start-up regulator that allows the VIN pin to be connected directly to line voltages as high as 60 V. The regulator output is internally current limited to 35 mA (typical). When power is applied, the regulator is enabled and sources current into an external capacitor, C_F, connected to the VCC pin. The recommended capacitance range for C_F is 0.1 µF to 100 µF. When the voltage on the VCC pin reaches the rising threshold of 5 V, the controller output is enabled. The controller will remain enabled until VCC falls below 4.7 V. In applications using a transformer, an auxiliary winding can be connected through a diode to the VCC pin. This winding should raise the VCC pin voltage to above 7.5 V to shut off the internal startup regulator. Powering VCC from an auxiliary winding improves conversion efficiency while reducing the power dissipated in the controller. The capacitance of C_F must be high enough that it maintains the VCC voltage greater than the VCC UVLO falling threshold (4.7 V) during the initial start-up. During a fault condition when the converter auxiliary winding is inactive, external current draw on the VCC line should be limited such that the power dissipated in the start-up regulator does not exceed the maximum power dissipation capability of the controller.

An external start-up or other bias rail can be used instead of the internal start-up regulator by connecting the VCC and the VIN pins together and feeding the external bias voltage (7.5 V to 14 V) to the two pins.

7.3.2 Input Undervoltage Detector

The LM5022-Q1 contains an input undervoltage lockout (UVLO) circuit. UVLO is programmed by connecting the UVLO pin to the center point of an external voltage divider from VIN to GND. The resistor divider must be designed such that the voltage at the UVLO pin is greater than 1.25 V when V_{IN} is in the desired operating range. If the under voltage threshold is not met, all functions of the controller are disabled and the controller remains in a low power standby state. UVLO hysteresis is accomplished with an internal 20 µA current source that is switched on or off into the impedance of the set-point divider. When the UVLO threshold is exceeded, the current source is activated to instantly raise the voltage at the UVLO pin. When the UVLO pin voltage falls below the 1.25 V threshold the current source is turned off, causing the voltage at the UVLO pin to fall. The UVLO pin can also be used to implement a remote enable / disable function. If an external transistor pulls the UVLO pin below the 1.25 V threshold, the converter will be disabled. This external shutdown method is shown in Figure 12.

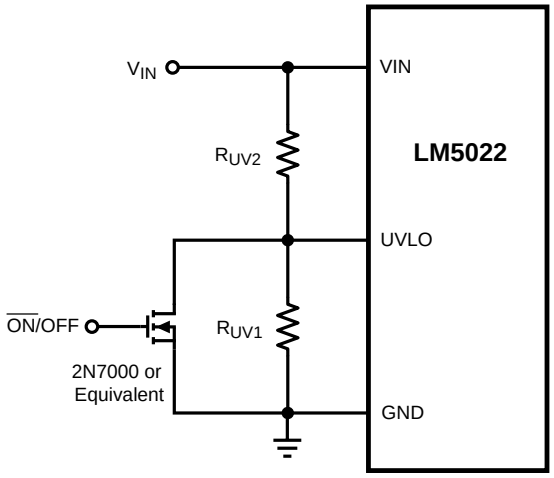


Figure 12. Enable/Disable Using UVLO

Feature Description (continued)

7.3.3 Error Amplifier

An internal high gain error amplifier is provided within the LM5022-Q1. The amplifier's non-inverting input is internally set to a fixed reference voltage of 1.25 V. The inverting input is connected to the FB pin. In non-isolated applications such as the boost converter the output voltage, V_O, is connected to the FB pin through a resistor divider. The control loop compensation components are connected between the COMP and FB pins. For most isolated applications the error amplifier function is implemented on the secondary side of the converter and the internal error amplifier is not used. The internal error amplifier is configured as an open drain output and can be disabled by connecting the FB pin to ground. An internal 5-kΩ pullup resistor between a 5-V reference and COMP can be used as the pull-up for an opto-coupler in isolated applications.

7.3.4 Current Sensing and Current Limiting

The LM5022-Q1 provides a cycle-by-cycle over current protection function. Current limit is accomplished by an internal current sense comparator. If the voltage at the current sense comparator input exceeds 0.5 V, the MOSFET gate drive will be immediately terminated. A small RC filter, located near the controller, is recommended to filter noise from the current sense signal. The CS input has an internal MOSFET which discharges the CS pin capacitance at the conclusion of every cycle. The discharge device remains on an additional 65 ns after the beginning of the new cycle to attenuate leading edge ringing on the current sense signal.

The LM5022-Q1 current sense and PWM comparators are very fast, and may respond to short duration noise pulses. Layout considerations are critical for the current sense filter and sense resistor. The capacitor associated with the CS filter must be located very close to the device and connected directly to the pins of the controller (CS and GND). If a current sense transformer is used, both leads of the transformer secondary should be routed to the sense resistor and the current sense filter network. The current sense resistor can be located between the source of the primary power MOSFET and power ground, but it must be a low inductance type. When designing with a current sense resistor all of the noise sensitive low-power ground connections should be connected together locally to the controller and a single connection should be made to the high current power ground (sense resistor ground point).

7.3.5 PWM Comparator and Slope Compensation

The PWM comparator compares the current ramp signal with the error voltage derived from the error amplifier output. The error amplifier output voltage at the COMP pin is offset by 1.4 V and then further attenuated by a 3:1 resistor divider. The PWM comparator polarity is such that 0 V on the COMP pin will result in a zero duty cycle at the controller output. For duty cycles greater than 50%, current mode control circuits can experience sub-harmonic oscillation. By adding an additional fixed-slope voltage ramp signal (slope compensation) this oscillation can be avoided. Proper slope compensation damps the double pole associated with current mode control (see *Control Loop Compensation*) and eases the design of the control loop compensator. The LM5022-Q1 generates the slope compensation with a sawtooth-waveform current source with a slope of 45 µA × f_{SW}, generated by the clock (see Figure 13). This current flows through an internal 2-kΩ resistor to create a minimum compensation ramp with a slope of 100 mV × f_{SW} (typical). The slope of the compensation ramp increases when external resistance is added for filtering the current sense (R_{S1}) or in the position R_{S2}. As shown in Figure 13 and the *Functional Block Diagram*, the sensed current slope and the compensation slope add together to create the signal used for current limiting and for the control loop itself.

Feature Description (continued)

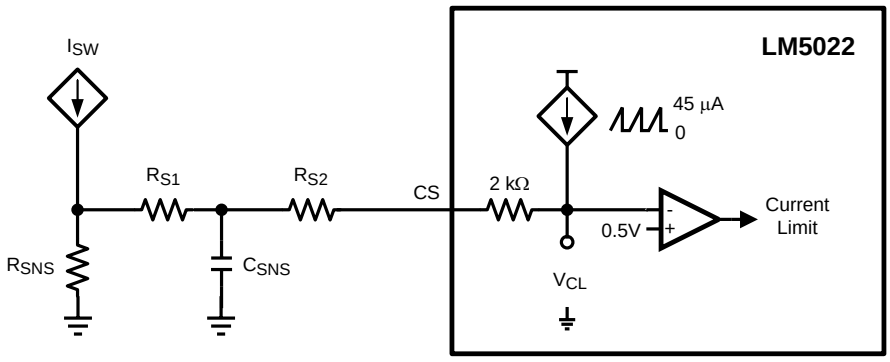


Figure 13. Slope Compensation

In peak current mode control the optimal slope compensation is proportional to the slope of the inductor current during the power switch off-time. For boost converters the inductor current slope while the MOSFET is off is (V_O - V_{IN}) / L. This relationship is combined with the requirements to set the peak current limit and is used to select R_{SNS} and R_{S2} in *Application and Implementation*.

7.3.6 Soft Start

The soft-start feature allows the power converter output to gradually reach the initial steady state output voltage, thereby reducing start-up stresses and current surges. At power on, after the VCC and input under-voltage lockout thresholds are satisfied, an internal 10-µA current source charges an external capacitor connected to the SS pin. The capacitor voltage will ramp up slowly and will limit the COMP pin voltage and the switch current.

7.3.7 MOSFET Gate Driver

The LM5022-Q1 provides an internal gate driver through the OUT pin that can source and sink a peak current of 1 A to control external, ground-referenced N-channel MOSFETs.

7.3.8 Thermal Shutdown

Internal thermal shutdown circuitry is provided to protect the LM5022-Q1 in the event that the maximum junction temperature is exceeded. When activated, typically at 165°C, the controller is forced into a low power standby state, disabling the output driver and the VCC regulator. After the temperature is reduced (typical hysteresis is 25°C) the VCC regulator will be re-enabled and the LM5022-Q1 will perform a soft start.

7.4 Device Functional Modes

7.4.1 Oscillator, Shutdown, and SYNC

A single external resistor, R_T, connected between the RT/SYNC and GND pins sets the LM5022-Q1 oscillator frequency. To set the switching frequency, f_{SW}, R_T can be calculated from:

$$R_T = \frac{\left(1 - 8 \times 10^{-8} \times f_{SW}\right)}{f_{SW} \times 5.77 \times 10^{-11}} \quad (1)$$

where

- f_{SW} is in Hz
- R_T is in Ω

Device Functional Modes (continued)

The LM5022-Q1 can also be synchronized to an external clock. The external clock must have a higher frequency than the free running oscillator frequency set by the R_T resistor. The clock signal should be capacitively coupled into the RT/SYNC pin with a 100-pF capacitor as shown in Figure 14. A peak voltage level greater than 3.8 V at the RT/SYNC pin is required for detection of the sync pulse. The sync pulse width should be set between 15 ns to 150 ns by the external components. The R_T resistor is always required, whether the oscillator is free running or externally synchronized. The voltage at the RT/SYNC pin is internally regulated to 2 V, and the typical delay from a logic high at the RT/SYNC pin to the rise of the OUT pin voltage is 120 ns. R_T should be located very close to the device and connected directly to the pins of the controller (RT/SYNC and GND).

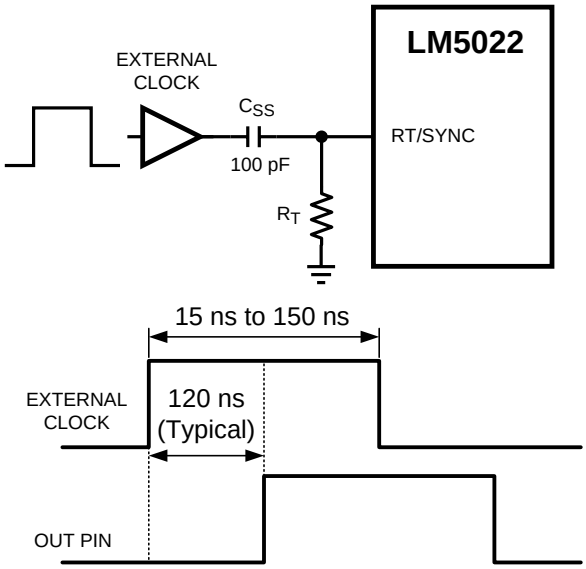


Figure 14. SYNC Operation

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The most common circuit controlled by the LM5022-Q1 is a non-isolated boost regulator. The boost regulator steps up the input voltage and has a duty ratio D of:

$$D = \frac{V_O - V_{IN} + V_D}{V_O + V_D} \quad (2)$$

where

- V_D is the forward voltage drop of the output diode

The following is a design procedure for selecting all the components for the boost converter circuit shown in Figure 15. The application is "in-cabin" automotive, meaning that the operating ambient temperature ranges from –20°C to 85°C. This circuit operates in continuous conduction mode (CCM), where inductor current stays above 0 A at all times, and delivers an output voltage of 40 V ±2% at a maximum output current of 0.5A. Additionally, the regulator must be able to handle a load transient of up to 0.5 A while keeping V_O within ±4%. The voltage input comes from the battery/alternator system of an automobile, where the standard range 9 V to 16 V and transients of up to 32 V must not cause any malfunction.

8.2 Typical Application

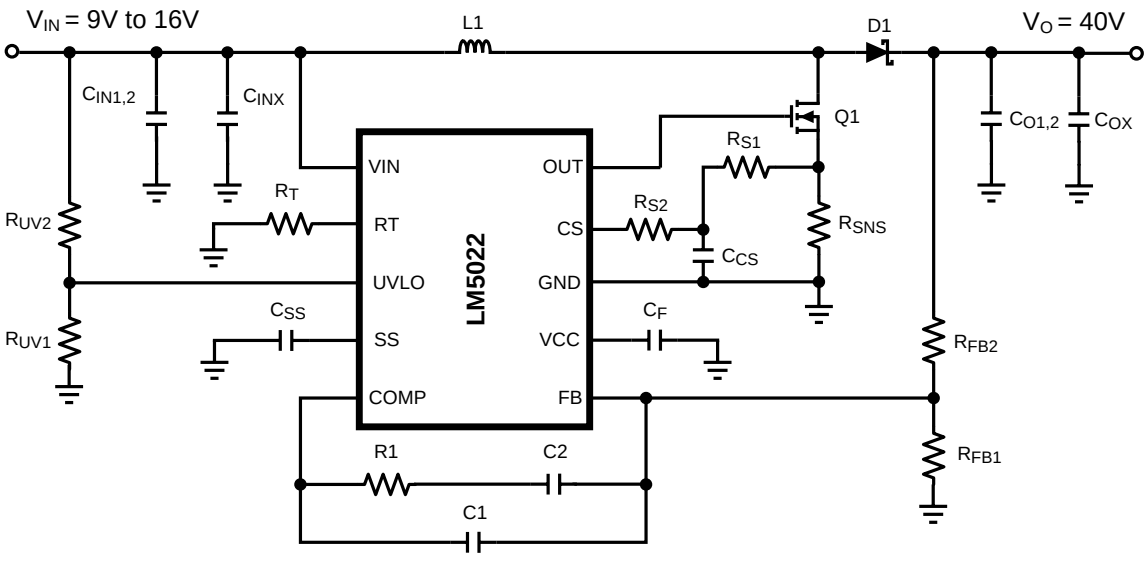


Figure 15. LM5022-Q1 Typical Application

8.2.1 Design Requirements

For typical low-side controller applications, use the parameters listed in Table 1.

Typical Application (continued)

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Minimum input voltage	9 V to 16 V
Minimum output voltage	40 V
Output current	500 mA
Switching frequency	500 kHz

Table 2. BOM for Example Circuit

ID	PART NUMBER	TYPE	SIZE	PARAMETERS	QTY	VENDOR
U1	LM5022-Q1	Low-Side Controller	10-pin VSSOP	60V	1	TI
Q1	Si4850EY	MOSFET	SO-8	60V, 31mΩ, 27nC	1	Vishay
D1	CMSH2-60M	Schottky Diode	SMA	60V, 2A	1	Central Semi
L1	SLF12575T-M3R2	Inductor	12.5 x 12.5 x 7.5 mm	33µH, 3.2A, 40mΩ	1	TDK
Cin1, Cin2	C4532X7R1H475M	Capacitor	1812	4.7µF, 50V, 3mΩ	2	TDK
Co1, Co2	C5750X7R2A475M	Capacitor	2220	4.7µF,100V, 3mΩ	2	TDK
Cf	C2012X7R1E105K	Capacitor	0805	1µF, 25V	1	TDK
Cinx Cox	C2012X7R2A104M	Capacitor	0805	100nF, 100V	2	TDK
C1	VJ0805A561KXXAT	Capacitor	0805	560pF 10%	1	Vishay
C2	VJ0805Y124KXXAT	Capacitor	0805	120nF 10%	1	Vishay
Css	VJ0805Y103KXXAT	Capacitor	0805	10nF 10%	1	Vishay
Ccs	VJ0805Y102KXXAT	Capacitor	0805	1nF 10%	1	Vishay
R1	CRCW08053011F	Resistor	0805	3.01kΩ 1%	1	Vishay
Rfb1	CRCW08056490F	Resistor	0805	649Ω 1%	1	Vishay
Rfb2	CRCW08052002F	Resistor	0805	20kΩ 1%	1	Vishay
Rs1	CRCW0805101J	Resistor	0805	100Ω 5%	1	Vishay
Rs2	CRCW08053571F	Resistor	0805	3.57kΩ 1%	1	Vishay
Rsns	ERJL14KF10C	Resistor	1210	100mΩ, 1%, 0.5W	1	Panasonic
Rt	CRCW08053322F	Resistor	0805	33.2kΩ 1%	1	Vishay
Ruv1	CRCW08052611F	Resistor	0805	2.61kΩ 1%	1	Vishay
Ruv2	CRCW08051002F	Resistor	0805	10kΩ 1%	1	Vishay

8.2.2 Detailed Design Procedure

8.2.2.1 Switching Frequency

The selection of switching frequency is based on the tradeoffs between size, cost, and efficiency. In general, a lower frequency means larger, more expensive inductors and capacitors will be needed. A higher switching frequency generally results in a smaller but less efficient solution, as the power MOSFET gate capacitances must be charged and discharged more often in a given amount of time. For this application, a frequency of 500 kHz was selected as a good compromise between the size of the inductor and efficiency. PCB area and component height are restricted in this application. Following the equation given for R_T in Equation 1, a 33.2-kΩ 1% resistor should be used to switch at 500 kHz.

8.2.2.2 MOSFET

Selection of the power MOSFET is governed by tradeoffs between cost, size, and efficiency. Breaking down the losses in the MOSFET is one way to determine relative efficiencies between different devices. For this example, the SO-8 package provides a balance of a small footprint with good efficiency.

Losses in the MOSFET can be broken down into conduction loss, gate charging loss, and switching loss.

Conduction, or I^2R loss, P_C, is approximately:

$$P_C = D \times \left[\left(\frac{I_O}{1-D} \right)^2 \times R_{DSON} \times 1.3 \right] \quad (3)$$

The factor 1.3 accounts for the increase in MOSFET on resistance due to heating. Alternatively, the factor of 1.3 can be ignored and the maximum on resistance of the MOSFET can be used.

Gate charging loss, P_G, results from the current required to charge and discharge the gate capacitance of the power MOSFET and is approximated as:

$$P_G = VCC \times Q_G \times f_{SW} \quad (4)$$

Q_G is the total gate charge of the MOSFET. Gate charge loss differs from conduction and switching losses because the actual dissipation occurs in the LM5022-Q1 and not in the MOSFET itself. If no external bias is applied to the VCC pin, additional loss in the LM5022-Q1 IC occurs as the MOSFET driving current flows through the VCC regulator. This loss, P_{VCC}, is estimated as:

$$P_{VCC} = (V_{IN} - VCC) \times Q_G \times f_{SW} \quad (5)$$

Switching loss, P_{SW}, occurs during the brief transition period as the MOSFET turns on and off. During the transition period both current and voltage are present in the channel of the MOSFET. The loss can be approximated as:

$$P_{SW} = 0.5 \times V_{IN} \times [I_O / (1 - D)] \times (t_R + t_F) \times f_{SW} \quad (6)$$

where

- t_R is the rise time of the MOSFET
- t_F is the fall time of the MOSFET

For this example, the maximum drain-to-source voltage applied across the MOSFET is V_O plus the ringing due to parasitic inductance and capacitance. The maximum drive voltage at the gate of the high side MOSFET is VCC, or 7 V typical. The MOSFET selected must be able to withstand 40V plus any ringing from drain to source, and be able to handle at least 7V plus ringing from gate to source. A minimum voltage rating of $50V_{D-S}$ and $10V_{G-S}$ MOSFET will be used. Comparing the losses in a spreadsheet leads to a $60V_{D-S}$ rated MOSFET in SO-8 with an R_{DSON} of 22 mΩ (the maximum vallue is 31 mΩ), a gate charge of 27 nC, and rise and falls times of 10 ns and 12 ns, respectively.

8.2.2.3 Output Diode

The boost regulator requires an output diode D1 (see Figure 15) to carrying the inductor current during the MOSFET off-time. The most efficient choice for D1 is a Schottky diode due to low forward drop and near-zero reverse recovery time. D1 must be rated to handle the maximum output voltage plus any switching node ringing when the MOSFET is on. In practice, all switching converters have some ringing at the switching node due to the diode parasitic capacitance and the lead inductance. D1 must also be rated to handle the average output current, I_O.

The overall converter efficiency becomes more dependent on the selection of D1 at low duty cycles, where the boost diode carries the load current for an increasing percentage of the time. This power dissipation can be calculating by checking the typical diode forward voltage, V_D, from the I-V curve on the diode's datasheet and then multiplying it by I_O. Diode datasheets will also provide a typical junction-to-ambient thermal resistance, $R_{\theta JA}$, which can be used to estimate the operating die temperature of the Schottky. Multiplying the power dissipation ($P_D = I_O \times V_D$) by $R_{\theta JA}$ gives the temperature rise. The diode case size can then be selected to maintain the Schottky diode temperature below the operational maximum.

In this example a Schottky diode rated to 60 V and 1 A will be suitable, as the maximum diode current will be 0.5 A. A small case such as SOD-123 can be used if a small footprint is critical. Larger case sizes generally have lower $R_{\theta JA}$ and lower forward voltage drop, so for better efficiency the larger SMA case size will be used.

8.2.2.4 Boost Inductor

The first criterion for selecting an inductor is the inductance itself. In fixed-frequency boost converters this value is based on the desired peak-to-peak ripple current, Δi_L, which flows in the inductor along with the average inductor current, I_L. For a boost converter in CCM I_L is greater than the average output current, I_O. The two currents are related by the following expression:

$$I_L = I_O / (1 - D) \tag{7}$$

As with switching frequency, the inductance used is a tradeoff between size and cost. Larger inductance means lower input ripple current, however because the inductor is connected to the output during the off-time only there is a limit to the reduction in output ripple voltage. Lower inductance results in smaller, less expensive magnetics. An inductance that gives a ripple current of 30% to 50% of I_L is a good starting point for a CCM boost converter. Minimum inductance should be calculated at the extremes of input voltage to find the operating condition with the highest requirement:

$$L_1 = \frac{V_{IN} \times D}{f_{SW} \times \Delta i_L} \tag{8}$$

By calculating in terms of amperes, volts, and megahertz, the inductance value will come out in micro henries.

In order to ensure that the boost regulator operates in CCM a second equation is needed, and must also be evaluated at the corners of input voltage to find the minimum inductance required:

$$L_2 = \frac{D(1\text{-}D) \times V_{IN}}{I_O \times f_{SW}} \tag{9}$$

By calculating in terms of volts, amps and megahertz the inductance value will come out in µH.

For this design Δi_L will be set to 40% of the maximum I_L. Duty cycle is evaluated first at $V_{IN(MIN)}$ and at $V_{IN(MAX)}$. Second, the average inductor current is evaluated at the two input voltages. Third, the inductor ripple current is determined. Finally, the inductance can be calculated, and a standard inductor value selected that meets all the criteria.

1. Inductance for Minimum Input Voltage

$$D_{VIN(MIN)} = (40 - 9 + 0.5) / (40 + 0.5) = 78\% \; I_{L\text{-}VIN(MIN)} = 0.5 / (1 - 0.78) = 2.3 \text{ A} \; \Delta i_L = 0.4 \times 2.3 \text{ A} = 0.92 \text{ A} \tag{10}$$

$$L_{1\text{-}VIN(MIN)} = \frac{9 \times 0.78}{0.5 \times 0.92} = 15.3 \; \mu H \tag{11}$$

$$L_{2\text{-}VIN(MIN)} = \frac{0.78 \times 0.22 \times 9}{0.5 \times 0.5} = 6.2 \; \mu H \tag{12}$$

2. Inductance for Maximum Input Voltage

$$D_{VIN(MAX)} = (40 - 16 + 0.5) / (40 + 0.5) = 60\% \; I_{L\text{-}VIN(MIAX)} = 0.5 / (1 - 0.6) = 1.25\text{A} \; \Delta i_L = 0.4 \times 1.25 \text{ A} = 0.5 \text{ A} \tag{13}$$

$$L_{1\text{-}VIN(MAX)} = \frac{16 \times 0.6}{0.5 \times 0.5} = 38.4 \; \mu H \tag{14}$$

$$L_{2\text{-}VIN(MAX)} = \frac{0.6 \times 0.4 \times 16}{0.5 \times 0.5} = 15.4 \; \mu H \tag{15}$$

Maximum average inductor current occurs at $V_{IN(MIN)}$, and the corresponding inductor ripple current is 0.92 $A_{P\text{-}P}$. Selecting an inductance that exceeds the ripple current requirement at $V_{IN(MIN)}$ and the requirement to stay in CCM for $V_{IN(MAX)}$ provides a tradeoff that allows smaller magnetics at the cost of higher ripple current at maximum input voltage. For this example, a 33-µH inductor will satisfy these requirements.

The second criterion for selecting an inductor is the peak current carrying capability. This is the level above which the inductor will saturate. In saturation the inductance can drop off severely, resulting in higher peak current that may overheat the inductor or push the converter into current limit. In a boost converter, peak current, I_{PK}, is equal to the maximum average inductor current plus one half of the ripple current. First, the current ripple must be determined under the conditions that give maximum average inductor current:

$$\Delta i_L = \frac{V_{IN} \times D}{f_{SW} \times L} \quad (16)$$

Maximum average inductor current occurs at $V_{IN(MIN)}$. Using the selected inductance of 33 µH yields the following:

$$\Delta i_L = (9 \times 0.78) / (0.5 \times 33) = 425\ mA_{P-P} \quad (17)$$

The highest peak inductor current over all operating conditions is therefore:

$$I_{PK} = I_L + 0.5 \times \Delta i_L = 2.3 + 0.213 = 2.51\ A \quad (18)$$

Hence an inductor must be selected that has a peak current rating greater than 2.5 A and an average current rating greater than 2.3A. One possibility is an off-the-shelf 33 µH ±20% inductor that can handle a peak current of 3.2 A and an average current of 3.4 A. Finally, the inductor current ripple is recalculated at the maximum input voltage:

$$\Delta i_{L\text{-}VIN(MAX)} = (16 \times 0.6) / (0.5 \times 33) = 0.58A_{P-P} \quad (19)$$

8.2.2.5 Output Capacitor

The output capacitor in a boost regulator supplies current to the load during the MOSFET on-time and also filters the AC portion of the load current during the off-time. This capacitor determines the steady state output voltage ripple, ΔV_O, a critical parameter for all voltage regulators. Output capacitors are selected based on their capacitance, C_O, their equivalent series resistance (ESR) and their RMS or AC current rating.

The magnitude of ΔV_O is comprised of three parts, and in steady state the ripple voltage during the on-time is equal to the ripple voltage during the off-time. For simplicity the analysis will be performed for the MOSFET turning off (off-time) only. The first part of the ripple voltage is the surge created as the output diode D1 turns on. At this point inductor/diode current is at the peak value, and the ripple voltage increase can be calculated as:

$$\Delta V_{O1} = I_{PK} \times ESR \quad (20)$$

The second portion of the ripple voltage is the increase due to the charging of C_O through the output diode. This portion can be approximated as:

$$\Delta V_{O2} = (I_O / C_O) \times (D / f_{SW}) \quad (21)$$

The final portion of the ripple voltage is a decrease due to the flow of the diode/inductor current through the output capacitor's ESR. This decrease can be calculated as:

$$\Delta V_{O3} = \Delta i_L \times ESR \quad (22)$$

The total change in output voltage is then:

$$\Delta V_O = \Delta V_{O1} + \Delta V_{O2} - \Delta V_{O3} \quad (23)$$

The combination of two positive terms and one negative term may yield an output voltage ripple with a net rise or a net fall during the converter off-time. The ESR of the output capacitor(s) has a strong influence on the slope and direction of ΔV_O. Capacitors with high ESR such as tantalum and aluminum electrolytic create an output voltage ripple that is dominated by ΔV_{O1} and ΔV_{O3}, with a shape shown in Figure 16. Ceramic capacitors, in contrast, have very low ESR and lower capacitance. The shape of the output ripple voltage is dominated by ΔV_{O2}, with a shape shown in Figure 17.

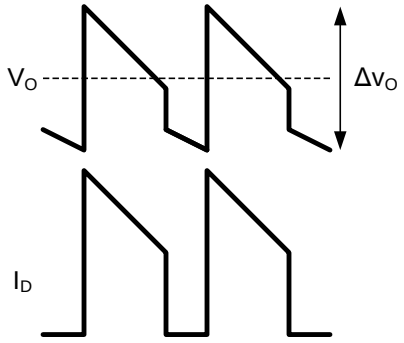


Figure 16. ΔV_O Using High ESR Capacitors

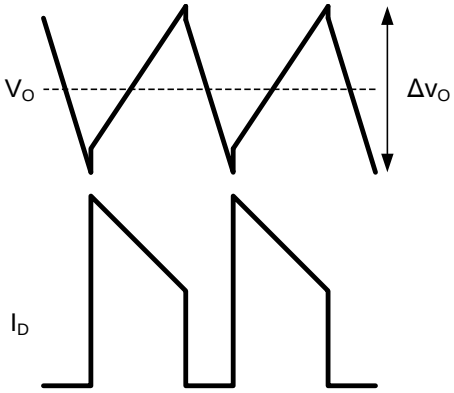


Figure 17. ΔV_O Using Low ESR Capacitors

For this example the small size and high temperature rating of ceramic capacitors make them a good choice. The output ripple voltage waveform of Figure 17 is assumed, and the capacitance will be selected first. The desired ΔV_O is ±2% of 40V, or $0.8V_{P-P}$. Beginning with the calculation for ΔV_{O2}, the required minimum capacitance is:

$$C_{O\text{-}MIN} = (I_O / \Delta V_O) \times (D_{MAX} / f_{SW})\ C_{O\text{-}MIN} = (0.5 / 0.8) \times (0.77 / 5 \times 10^5) = 0.96\ \mu F \quad (24)$$

The next higher standard 20% capacitor value is 1 µF, however to provide margin for component tolerance and load transients two capacitors rated 4.7 µF each will be used. Ceramic capacitors rated 4.7 µF ±20% are available from many manufacturers. The minimum quality dielectric that is suitable for switching power supply output capacitors is X5R, while X7R (or better) is preferred. Careful attention must be paid to the DC voltage rating and case size, as ceramic capacitors can lose 60% or more of their rated capacitance at the maximum DC voltage. This is the reason that ceramic capacitors are often de-rated to 50% of their capacitance at their working voltage. The output capacitors for this example will have a 100V rating in a 2220 case size.

The typical ESR of the selected capacitors is 3 mΩ each, and in parallel is approximately 1.5 mΩ. The worst-case value for ΔV_{O1} occurs during the peak current at minimum input voltage:

$$\Delta V_{O1} = 2.5 \times 0.0015 = 4\ mV \quad (25)$$

The worst-case capacitor charging ripple occurs at maximum duty cycle:

$$\Delta V_{O2} = (0.5 / 9.4 \times 10^{-6}) \times (0.77 / 5 \times 10^5) = 82\ mV \quad (26)$$

Finally, the worst-case value for ΔV_{O3} occurs when inductor ripple current is highest, at maximum input voltage:

$$\Delta V_{O3} = 0.58 \times 0.0015 = 1\ mV\ (negligible) \quad (27)$$

The output voltage ripple can be estimated by summing the three terms:

$$\Delta V_O = 4\ mV + 82\ mV - 1\ mV = 85\ mV \quad (28)$$

The RMS current through the output capacitor(s) can be estimated using the following, worst-case equation:

$$I_{O\text{-}RMS} = 1.13 \times I_L \times \sqrt{D \times (1 - D)} \quad (29)$$

The highest RMS current occurs at minimum input voltage. For this example the maximum output capacitor RMS current is:

$$I_{O\text{-}RMS(MAX)} = 1.13 \times 2.3 \times (0.78 \times 0.22)^{0.5} = 1.08\ A_{RMS} \quad (30)$$

These 2220 case size devices are capable of sustaining RMS currents of over 3A each, making them more than adequate for this application.

8.2.2.6 VCC Decoupling Capacitor

The VCC pin should be decoupled with a ceramic capacitor placed as close as possible to the VCC and GND pins of the LM5022-Q1. The decoupling capacitor should have a minimum X5R or X7R type dielectric to ensure that the capacitance remains stable over voltage and temperature, and be rated to a minimum of 470 nF. One good choice is a 1-µF device with X7R dielectric and 1206 case size rated to 25 V.

8.2.2.7 Input Capacitor

The input capacitors to a boost regulator control the input voltage ripple, ΔV_{IN}, hold up the input voltage during load transients, and prevent impedance mismatch (also called power supply interaction) between the LM5022-Q1 and the inductance of the input leads. Selection of input capacitors is based on their capacitance, ESR, and RMS current rating. The minimum value of ESR can be selected based on the maximum output current transient, I_{STEP}, using the following expression:

$$ESR_{MIN} = \frac{(1\text{-}D) \times \Delta v_{IN}}{2 \times I_{STEP}} \quad (31)$$

For this example the maximum load step is equal to the load current, or 0.5A. The maximum permissible ΔV_{IN} during load transients is $4\%_{P\text{-}P}$. ΔV_{IN} and duty cycle are taken at minimum input voltage to give the worst-case value:

$$ESR_{MIN} = [(1 - 0.77) \times 0.36] / (2 \times 0.5) = 83\ m\Omega \quad (32)$$

The minimum input capacitance can be selected based on ΔV_{IN}, based on the drop in V_{IN} during a load transient, or based on prevention of power supply interaction. In general, the requirement for greatest capacitance comes from the power supply interaction. The inductance and resistance of the input source must be estimated, and if this information is not available, they can be assumed to be 1 µH and 0.1 Ω, respectively. Minimum capacitance is then estimated as:

$$C_{MIN} = \frac{2 \times L_S \times V_O \times I_O}{V_{IN}^2 \times R_S} \quad (33)$$

As with ESR, the worst-case, highest minimum capacitance calculation comes at the minimum input voltage. Using the default estimates for L_S and R_S, minimum capacitance is:

$$C_{MIN} = \frac{2 \times 1\mu \times 40 \times 0.5}{9^2 \times 0.1} = 4.9\ \mu F \quad (34)$$

The next highest standard 20% capacitor value is 6.8 µF, but because the actual input source impedance and resistance are not known, two 4.7 µF capacitors will be used. In general, doubling the calculated value of input capacitance provides a good safety margin. The final calculation is for the RMS current. For boost converters operating in CCM this can be estimated as:

$$I_{RMS} = 0.29 \times \Delta i_{L(MAX)} \quad (35)$$

From the inductor section, maximum inductor ripple current is 0.58 A, hence the input capacitor(s) must be rated to handle $0.29 \times 0.58 = 170\ mA_{RMS}$.

The input capacitors can be ceramic, tantalum, aluminum, or almost any type, however the low capacitance requirement makes ceramic capacitors particularly attractive. As with the output capacitors, the minimum quality dielectric used should X5R, with X7R or better preferred. The voltage rating for input capacitors need not be as conservative as the output capacitors, as the need for capacitance decreases as input voltage increases. For this example, the capacitor selected will be 4.7 µF ±20%, rated to 50 V, in the 1812 case size. The RMS current rating of these capacitors is over 2A each, more than enough for this application.

8.2.2.8 Current Sense Filter

Parasitic circuit capacitance, inductance and gate drive current create a spike in the current sense voltage at the point where Q1 turns on. In order to prevent this spike from terminating the on-time prematurely, every circuit should have a low-pass filter that consists of C_{CS} and R_{S1}, shown in Figure 15. The time constant of this filter should be long enough to reduce the parasitic spike without significantly affecting the shape of the actual current sense voltage. The recommended range for R_{S1} is between 10 Ω and 500 Ω, and the recommended range for C_{CS} is between 100 pF and 2.2 nF. For this example, the values of R_{S1} and C_{CS} will be 100Ω and 1 nF, respectively.

8.2.2.9 R_{SNS}, R_{S2} and Current Limit

The current sensing resistor R_{SNS} is used for steady state regulation of the inductor current and to sense overcurrent conditions. The slope compensation resistor is used to ensure control loop stability, and both resistors affect the current limit threshold. The R_{SNS} value selected must be low enough to keep the power dissipation to a minimum, yet high enough to provide good signal-to-noise ratio for the current sensing circuitry. R_{SNS}, and R_{S2} should be set so that the current limit comparator, with a threshold of 0.5 V, trips before the sensed current exceeds the peak current rating of the inductor, without limiting the output power in steady state.

For this example the peak current, at $V_{IN(MIN)}$, is 2.5 A, while the inductor itself is rated to 3.2 A. The threshold for current limit, I_{LIM}, is set slightly between these two values to account for tolerance of the circuit components, at a level of 3 A. The required resistor calculation must take into account both the switch current through R_{SNS} and the compensation ramp current flowing through the internal 2 kΩ, R_{S1} and R_{S2} resistors. R_{SNS} should be selected first because it is a power resistor with more limited selection. The following equation should be evaluated at $V_{IN(MIN)}$, when duty cycle is highest:

$$R_{SNS} = \frac{L \times f_{SW} \times V_{CL}}{(V_O - V_{IN}) \times 3 \times D + L \times f_{SW} \times I_{LIM}} \tag{36}$$

$$R_{SNS} = \frac{33 \times 0.5 \times 0.5}{(40 - 9) \times 3 \times 0.78 + 33 \times 0.5 \times 3} = 0.068\Omega$$

where

- L is in µH
- f_{SW} in MHz (37)

The closest 5% value is 100 mΩ. Power dissipation in R_{SNS} can be estimated by calculating the average current. The worst-case average current through R_{SNS} occurs at minimum input voltage/maximum duty cycle and can be calculated as:

$$P_{CS} = \left[\left(\frac{I_O}{1-D}\right)^2 \times R_{SNS}\right] \times D \tag{38}$$

$$P_{CS} = [(0.5 / 0.22)^2 \times 0.1] \times 0.78 = 0.4W \tag{39}$$

For this example a 0.1 Ω ±1%, thick-film chip resistor in a 1210 case size rated to 0.5W will be used.

With R_{SNS} selected, R_{S2} can be determined using the following expression:

$$R_{S2} = \frac{V_{CL} - I_{ILIM} \times R_{SNS}}{45\mu \times D} - 2000 - R_{S1} \tag{40}$$

$$R_{S2} = \frac{0.5 - 3 \times 0.1}{45\mu \times 0.78} - 2000 - 100 = 3598\Omega \tag{41}$$

The closest 1% tolerance value is 3.57 kΩ.

8.2.2.10 Control Loop Compensation

The LM5022-Q1 uses peak current-mode PWM control to correct changes in output voltage due to line and load transients. Peak current-mode provides inherent cycle-by-cycle current limiting, improved line transient response, and easier control loop compensation.

The control loop is comprised of two parts. The first is the power stage, which consists of the pulse width modulator, output filter, and the load. The second part is the error amplifier, which is an op-amp configured as an inverting amplifier. Figure 18 shows the regulator control loop components.

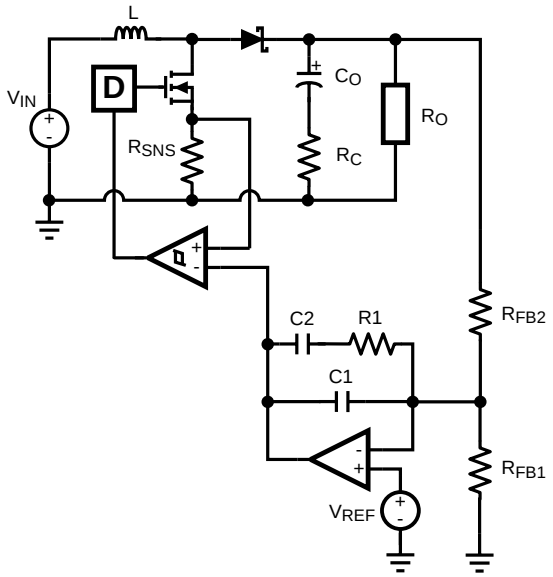


Figure 18. Power Stage and Error Amplifier

One popular method for selecting the compensation components is to create Bode plots of gain and phase for the power stage and error amplifier. Combined, they make the overall bandwidth and phase margin of the regulator easy to determine. Software tools such as Excel, MathCAD, and Matlab are useful for observing how changes in compensation or the power stage affect system gain and phase.

The power stage in a CCM peak current mode boost converter consists of the DC gain, A_{PS}, a single low frequency pole, f_{LFP}, the ESR zero, f_{ZESR}, a right-half plane zero, f_{RHP}, and a double pole resulting from the sampling of the peak current. The power stage transfer function (also called the Control-to-Output transfer function) can be written:

$$G_{PS} = A_{PS} \times \frac{\left(1+\frac{s}{\omega_{ZESR}}\right)\left(1-\frac{s}{\omega_{RHP}}\right)}{\left(1+\frac{s}{\omega_{LEP}}\right)\left(1+\frac{s}{Q_n \times \omega_n}+\frac{s^2}{\omega^2_n}\right)}$$

where

- the DC gain is defined as: (42)

$$A_{PS} = \frac{(1 - D) \times R_O}{2 \times R_{SNS}}$$

where (43)

$$R_O = V_O / I_O \quad (44)$$

The system ESR zero is:

$$\omega_{ZESR} = \frac{1}{R_C \times C_O} \quad (45)$$

The low frequency pole is:

$$\omega_{LEP} = \frac{1}{0.5 \times (R_O + ESR) \times C_O} \quad (46)$$

The right-half plane zero is:

$$\omega_{RHP} = \frac{R_O \times \left(\frac{V_{IN}}{V_O}\right)^2}{L} \quad (47)$$

The sampling double pole quality factor is:

$$Q_n = \frac{1}{\pi \left[-D + 0.5 + (1 - D)\frac{S_e}{S_n}\right]} \quad (48)$$

The sampling double corner frequency is:

$$\omega_n = \pi \times f_{SW} \quad (49)$$

The natural inductor current slope is:

$$S_n = R_{SNS} \times V_{IN} / L \quad (50)$$

The external ramp slope is:

$$S_e = 45\ \mu A \times (2000 + R_{S1} + R_{S2})] \times f_{SW} \quad (51)$$

In the equation for A_{PS}, DC gain is highest when input voltage and output current are at the maximum. In this the example those conditions are V_{IN} = 16 V and I_O = 500 mA.

DC gain is 44 dB. The low frequency pole $f_P = 2\pi\omega_P$ is at 423 Hz, the ESR zero $f_Z = 2\pi\omega_Z$ is at 5.6 MHz, and the right-half plane zero $f_{RHP} = 2\pi\omega_{RHP}$ is at 61 kHz. The sampling double-pole occurs at one-half of the switching frequency. Proper selection of slope compensation (via R_{S2}) is most evident the sampling double pole. A well-selected R_{S2} value eliminates peaking in the gain and reduces the rate of change of the phase lag. Gain and phase plots for the power stage are shown in Figure 19 and Figure 20.

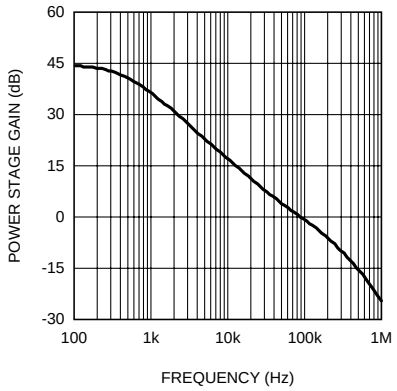


Figure 19. Power Stage Gain and Phase

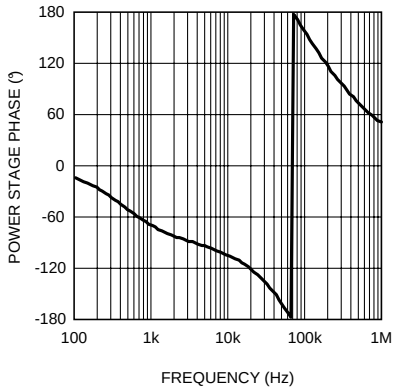


Figure 20. Power Stage Gain and Phase

The single pole causes a roll-off in the gain of –20 dB/decade at lower frequency. The combination of the RHP zero and sampling double pole maintain the slope out to beyond the switching frequency. The phase tends towards –90° at lower frequency but then increases to –180° and beyond from the RHP zero and the sampling double pole. The effect of the ESR zero is not seen because its frequency is several decades above the switching frequency. The combination of increasing gain and decreasing phase makes converters with RHP zeroes difficult to compensate. Setting the overall control loop bandwidth to 1/3 to 1/10 of the RHP zero frequency minimizes these negative effects, but requires a compromise in the control loop bandwidth. If this loop were left uncompensated, the bandwidth would be 89 kHz and the phase margin -54°. The converter would oscillate, and therefore is compensated using the error amplifier and a few passive components.

The transfer function of the compensation block, G_{EA}, can be derived by treating the error amplifier as an inverting op-amp with input impedance Z_I and feedback impedance Z_F. The majority of applications will require a Type II, or two-pole one-zero amplifier, shown in Figure 18. The LaPlace domain transfer function for this Type II network is given by the following:

$$G_{EA} = \frac{Z_F}{Z_I} = \frac{1}{R_{FB2}\,(C1 + C2)} \times \frac{s \times R1 \times C2 + 1}{s\left(\frac{s \times R1 \times C1 \times C2}{C1 + C2} + 1\right)} \quad (52)$$

Many techniques exist for selecting the compensation component values. The following method is based upon setting the mid-band gain of the error amplifier transfer function first and then positioning the compensation zero and pole:

1. *Determine the desired control loop bandwidth:* The control loop bandwidth, f_{0dB}, is the point at which the total control loop gain ($H = G_{PS} \times G_{EA}$) is equal to 0 dB. For this example, a low bandwidth of 10 kHz, or approximately 1/6th of the RHP zero frequency, is chosen because of the wide variation in input voltage.
2. *Determine the gain of the power stage at f_{0dB}:* This value, A, can be read graphically from the gain plot of G_{PS} or calculated by replacing the 's' terms in G_{PS} with '$2\pi f_{0dB}$'. For this example the gain at 10 kHz is approximately 16 dB.
3. *Calculate the negative of A and convert it to a linear gain:* By setting the mid-band gain of the error amplifier to the negative of the power stage gain at f_{0dB}, the control loop gain will equal 0 dB at that frequency. For this example, –16 dB = 0.15V/V.
4. *Select the resistance of the top feedback divider resistor R_{FB2}:* This value is arbitrary, however selecting a resistance between 10 kΩ and 100 kΩ will lead to practical values of R1, C1 and C2. For this example, R_{FB2} = 20 kΩ 1%.
5. *Set R1 = A × R_{FB2}:* For this example: R1 = 0.15 × 20000 = 3 kΩ
6. *Select a frequency for the compensation zero, f_{Z1}:* The suggested placement for this zero is at the low frequency pole of the power stage, f_{LFP} = ωLFP / 2π. For this example, $f_{Z1} = f_{LFP}$ = 423 Hz
7. *Set*

   $$C2 = \frac{1}{2\pi \times R1 \times f_{Z1}}:$$

   For this example, C2 = 125 nF
8. *Select a frequency for the compensation pole, f_{P1}:* The suggested placement for this pole is at one-fifth of the switching frequency. For this example, f_{P1} = 100 kHz
9. **Set**

   $$C1 = \frac{C2}{2\pi \times C2 \times R1 \times f_{P1} - 1}:$$

   For this example, C1 = 530 pF
10. *Plug the closest 1% tolerance values for R_{FB2} and R1, then the closest 10% values for C1 and C2 into G_{EA} and model the error amp:* The open-loop gain and bandwidth of the LM5022-Q1's internal error amplifier are 75 dB and 4 MHz, respectively. Their effect on G_{EA} can be modeled using the following expression:

    $$OPG = \frac{2\pi \times GBW}{s + \frac{2\pi \times GBW}{A_{DC}}}$$

    A_{DC} is a linear gain, the linear equivalent of 75 dB is approximately 5600V/V. C1 = 560 pF 10%, C2 = 120 nF 10%, R1 = 3.01 kΩ 1%
11. *Plot or evaluate the actual error amplifier transfer function:*

    $$G_{EA\text{-}ACTUAL} = \frac{G_{EA} \times OPG}{1 + G_{EA} \times OPG}$$

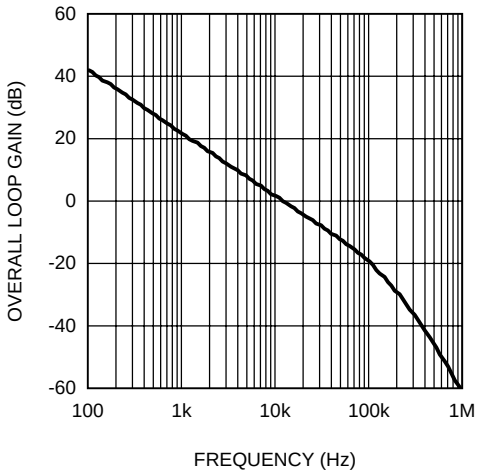


Figure 21. Overall Loop Gain and Phase

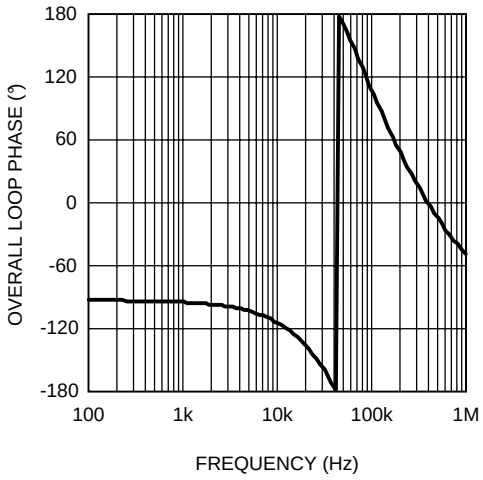


Figure 22. Overall Loop Gain and Phase

12. *Plot or evaluate the complete control loop transfer function:* The complete control loop transfer function is obtained by multiplying the power stage and error amplifier functions together. The bandwidth and phase margin can then be read graphically or evaluated numerically. The bandwidth of this example circuit at V_{IN} = 16 V is 10.5 kHz, with a phase margin of 66°.
13. *Re-evaluate at the corners of input voltage and output current:* Boost converters exhibit significant change in their loop response when V_{IN} and I_O change. With the compensation fixed, the total control loop gain and phase should be checked to ensure a minimum phase margin of 45° over both line and load.

8.2.2.11 Efficiency Calculations

A reasonable estimation for the efficiency of a boost regulator controlled by the LM5022-Q1 can be obtained by adding together the loss is each current carrying element and using the equation:

$$\eta = \frac{P_O}{P_O + P_{total\text{-}loss}} \tag{53}$$

The following shows an efficiency calculation to complement the circuit design from *Device Functional Modes*. Output power for this circuit is 40 V x 0.5 A = 20 W. Input voltage is assumed to be 13.8 V, and the calculations used assume that the converter runs in CCM. Duty cycle for V_{IN} = 13.8V is 66%, and the average inductor current is 1.5 A.

8.2.2.11.1 Chip Operating Loss

This term accounts for the current drawn at the VIN pin. This current, I_{IN}, drives the logic circuitry and the power MOSFETs. The gate driving loss term from *MOSFET* is included in the chip operating loss. For the LM5022-Q1, I_{IN} is equal to the steady state operating current, I_{CC}, plus the MOSFET driving current, I_{GC}. Power is lost as this current passes through the internal linear regulator of the LM5022-Q1.

$$I_{GC} = Q_G \times f_{SW}\ I_{GC} = 27\ nC \times 500\ kHz = 13.5\ mA \quad (54)$$

I_{CC} is typically 3.5 mA, taken from the Electrical Characteristics table. Chip Operating Loss is then:

$$P_Q = V_{IN} \times (I_Q + I_{GC})\ P_Q = 13.8 \times (3.5\ m + 13.5m) = 235\ mW \quad (55)$$

8.2.2.11.2 MOSFET Switching Loss

$$P_{SW} = 0.5 \times V_{IN} \times I_L \times (t_R + t_F) \times f_{SW}\ P_{SW} = 0.5 \times 13.8 \times 1.5 \times (10\ ns + 12\ ns) \times 5 \times 10^5 = 114\ mW \quad (56)$$

8.2.2.11.3 MOSFET and R_{SNS} Conduction Loss

$$P_C = D \times (I_L^2 \times (R_{DSON} \times 1.3 + R_{SNS}))\ P_C = 0.66 \times (1.5^2 \times (0.029 + 0.1)) = 192\ mW \quad (57)$$

8.2.2.11.4 Output Diode Loss

The average output diode current is equal to I_O, or 0.5 A. The estimated forward drop, V_D, is 0.5 V. The output diode loss is therefore:

$$P_{D1} = I_O \times V_D\ P_{D1} = 0.5 \times 0.5 = 0.25\ W \quad (58)$$

8.2.2.11.5 Input Capacitor Loss

This term represents the loss as input ripple current passes through the ESR of the input capacitor bank. In this equation 'n' is the number of capacitors in parallel. The 4.7 µF input capacitors selected have a combined ESR of approximately 1.5 mΩ, and Δi_L for a 13.8V input is 0.55A:

$$P_{CIN} = \frac{I_{IN\text{-}RMS}^2 \times ESR}{n} \quad (59)$$

$$I_{IN\text{-}RMS} = 0.29 \times \Delta i_L = 0.29 \times 0.55 = 0.16\ A\ P_{CIN} = [0.16^2 \times 0.0015] / 2 = 0.02\ mW\ (negligible) \quad (60)$$

8.2.2.11.6 Output Capacitor Loss

This term is calculated using the same method as the input capacitor loss, substituting the output capacitor RMS current for V_{IN} = 13.8 V. The output capacitors' combined ESR is also approximately 1.5 mΩ.

$$I_{O\text{-}RMS} = 1.13 \times 1.5 \times (0.66 \times 0.34)^{0.5} = 0.8\ A\ P_{CO} = [0.8 \times 0.0015] / 2 = 0.6\ mW \quad (61)$$

8.2.2.11.7 Boost Inductor Loss

The typical DCR of the selected inductor is 40 mΩ.

$$P_{DCR} = I_L^2 \times DCR\ P_{DCR} = 1.5^2 \times 0.04 = 90\ mW \quad (62)$$

Core loss in the inductor is estimated to be equal to the DCR loss, adding an additional 90 mW to the total inductor loss.

8.2.2.11.8 Total Loss

$$P_{LOSS} = \text{Sum of All Loss Terms} = 972\ mW \quad (63)$$

8.2.2.11.9 Efficiency

$$\eta = 20 / (20 + 0.972) = 95\% \quad (64)$$

8.2.3 Application Curves

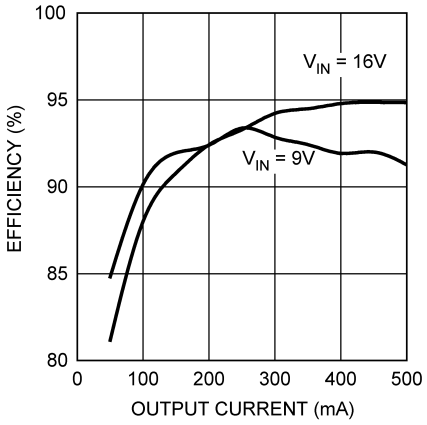
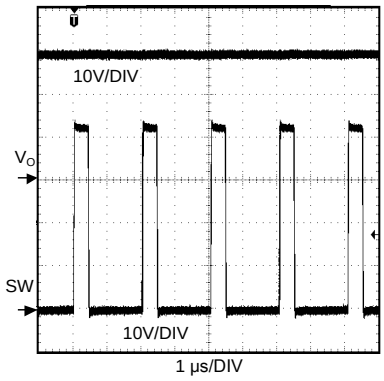
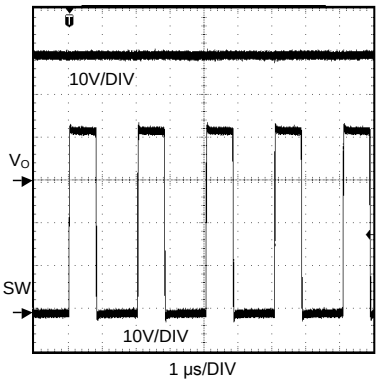


Figure 23. Efficiency vs. Load Current



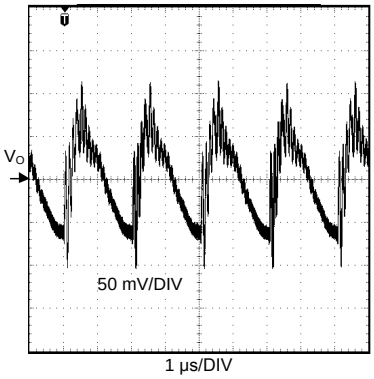
VIN = 9-V I_O = 0.5-A

Figure 24. SW Node Voltage



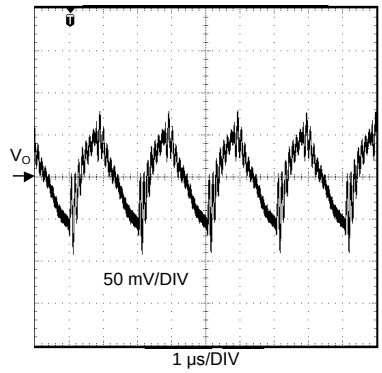
VIN = 16-V I_O = 0.5-A

Figure 25. SW Node Voltage



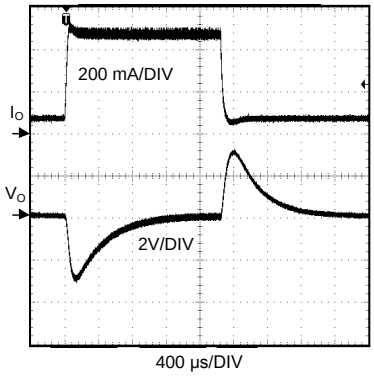
VIN = 9-V I_O = 0.5-A

Figure 26. Output Voltage Ripple (AC Coupled)



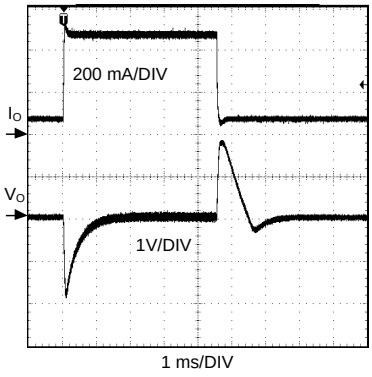
VIN = 16-V I_O = 0.5-A

Figure 27. Output Voltage Ripple (AC Coupled)



VIN = 9-V I_O = 50mA - 500mA

Figure 28. Load Transient Response



VIN = 16-V I_O = 50mA - 500mA

Figure 29. Load Transient Response

9 Power Supply Recommendations

LM5022-Q1 is a power management device. The power supply for the device can be any DC voltage source within the specified input range.

10 Layout

10.1 Layout Guidelines

To produce an optimal power solution with the LM5022-Q1, good layout and design of the PCB are as critical as component selection. The following are the several guidelines in order to create a good layout of the PCB, as based on Figure 15.

1. Using a low ESR ceramic capacitor, place C_{INX} as close as possible to the VIN and GND pins of the LM5022-Q1.
2. Using a low ESR ceramic capacitor, place C_{OX} close to the load as possible of the LM5022-Q1
3. Using a low ESR ceramic capacitor place C_F close to the VCC and GND pins of the LM5022-Q1
4. Minimize the loop area formed by the output capacitor connections (C_{o1}, C_{o2}), by D1 and R_{sns}. Making sure the cathode of D1 and R_{sns} are position next to each other and place C_{o1}(+)and C_{o1}(-) close to D1 cathode and R_{sns} (-) respectively.
5. R_{sns} (+) should be connected to the CS pin with a separate trace made as short as possible. This trace should be routed away from the inductor and the switch node (where D1, Q1, and L1 connect).
6. Minimize the trace length to the FB pin by positioning R_{FB1} and R_{FB2} close to the LM5022-Q1
7. Route the VOUT sense path away from noisy node and connect it as close as possible to the positive side of C_{OX}.

10.1.1 Filter Capacitors

The low-value ceramic filter capacitors are most effective when the inductance of the current loops that they filter, is minimized. Place C_{INX} as close as possible to the VIN and GND pins of the LM5022-Q1. Place C_{OX} close to the load, and C_F next to the VCC and GND pins of the LM5022-Q1.

10.1.2 Sense Lines

The top of R_{SNS} should be connected to the CS pin with a separate trace, made as short as possible. Route this trace away from the inductor and the switch node (where D1, Q1, and L1 connect). For the voltage loop, keep $R_{FB1}$and R_{FB2} close to the LM5022-Q1 and run a trace, as close as possible, to the positive side of C_{OX} to R_{FB2}. As with the CS line, the FB line should be routed away from the inductor and the switch node. These measures minimize the length of high impedance lines and reduce noise pickup.

Layout Guidelines (continued)

10.1.3 Compact Layout

1. Parasitic inductance can be reduced by keeping the power path components close together. As described above in point 4 in the *Layout Guidelines*, keep the high slew-rate current loops as tight as possible. Short, thick traces or copper pours (shapes) are best
2. The switch node should be just large enough to connect all the components together without excessive heating from the current it carries. The LM5022-Q1 (boost converter) operates in two distinct cycles whose high current paths are shown in Figure 30:

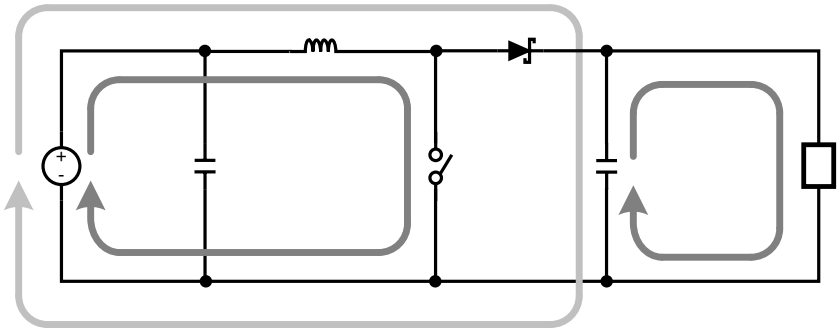


Figure 30. Boost Converter Current Loops

The dark grey, inner loops represent the high current paths during the MOSFET on-time. The light grey, outer loop represents the high current path during the off-time.

10.1.4 Ground Plane and Shape Routing

The diagram of Figure 30 is useful for analyzing the flow of continuous current vs. the flow of pulsating currents. The circuit paths with current flow during both the on-time and off-time are considered to be continuous current, while those that carry current during the on-time or off-time only are pulsating currents. Preference in routing should be given to the pulsating current paths, as these are the portions of the circuit most likely to emit EMI. The ground plane of a PCB is a conductor and return path, and it is susceptible to noise injection just as any other circuit path. The continuous current paths on the ground net can be routed on the system ground plane with less risk of injecting noise into other circuits. The path between the input source, input capacitor and the MOSFET and the path between the output capacitor and the load are examples of continuous current paths. In contrast, the path between the grounded side of the power switch and the negative output capacitor terminal carries a large high slew-rate pulsating current. This path should be routed with a short, thick shape, preferably on the component side of the PCB. Too keep the parasitic inductance low, multiple vias in parallel should be placed on the negative pads of the input and output capacitors to connect the component side to the ground plane. Vias should not be placed directly at the grounded side of the MOSFET (or R_{SNS}) as they tend to inject noise into the ground plane. A second pulsating current loop is the gate drive loop formed by the OUT and VCC pins, Q1, R_{SNS} and capacitor C_F. These loops must be kept small.

10.2 Layout Example

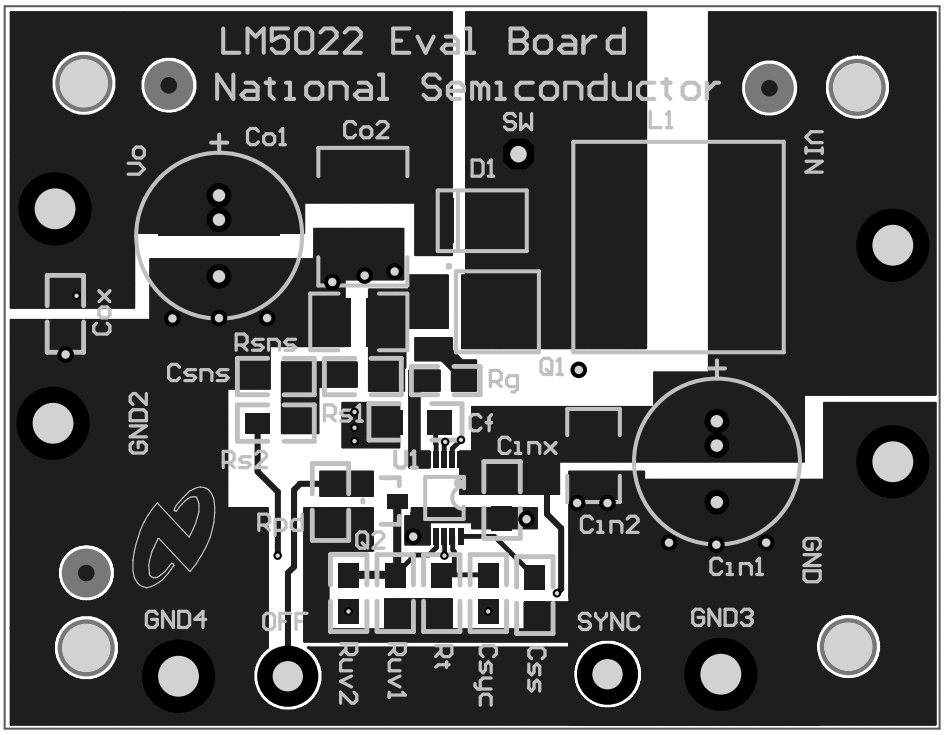


Figure 31. Typical Top Layer Overlay of the LM5022 Evaluation Board

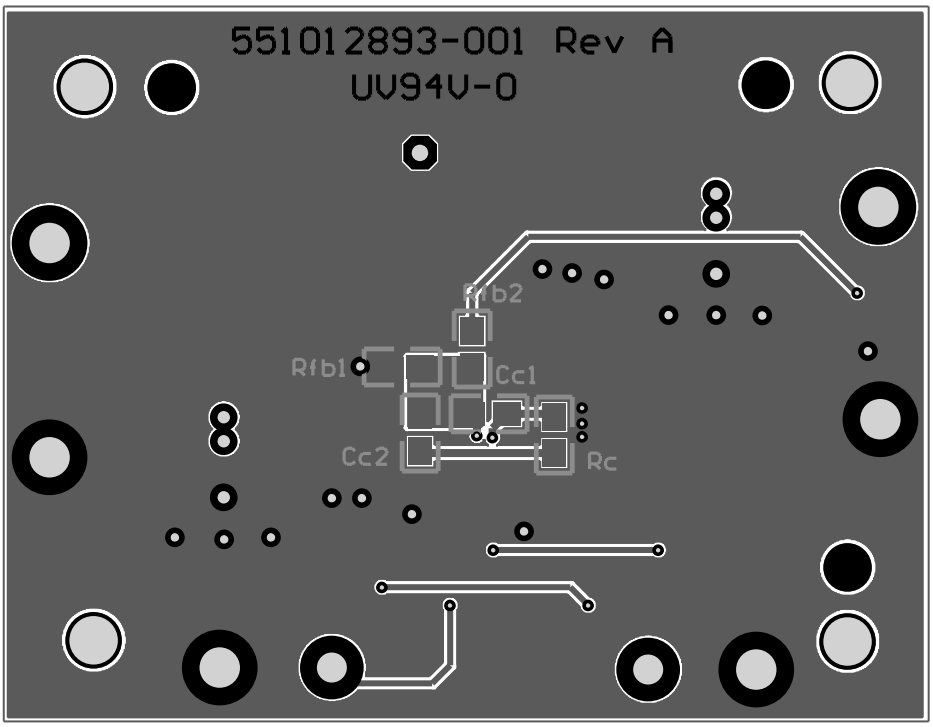


Figure 32. Typical Bottom Layer Overlay of the LM5022 Evaluation Board

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.1.2 Design Support

WEBENCH software uses an iterative design procedure and accesses comprehensive databases of components. For more details, go to www.ti.com/webench.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5022QDGSRQ1	ACTIVE	VSSOP	DGS	10	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	5Q22	Samples
LM5022QDGSTQ1	ACTIVE	VSSOP	DGS	10	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	5Q22	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF LM5022-Q1 :

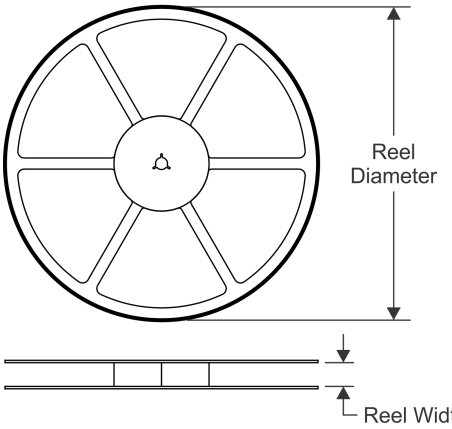
- Catalog: LM5022

NOTE: Qualified Version Definitions:

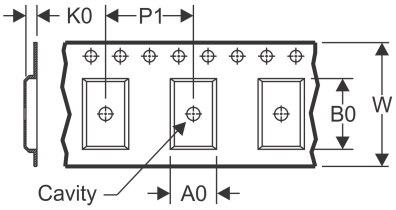
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

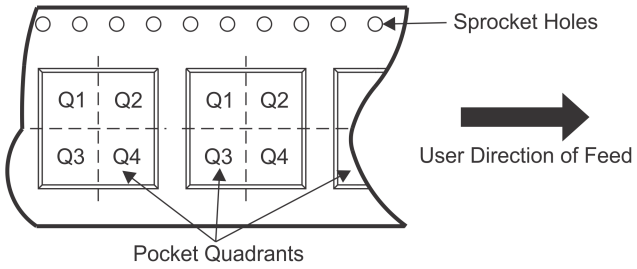


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

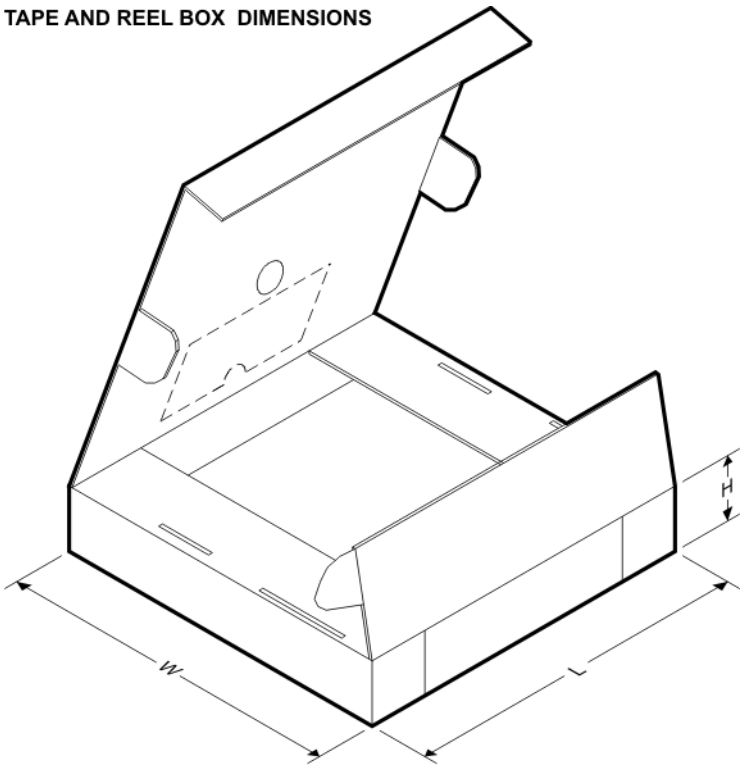
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5022QDGSRQ1	VSSOP	DGS	10	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5022QDGSTQ1	VSSOP	DGS	10	250	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

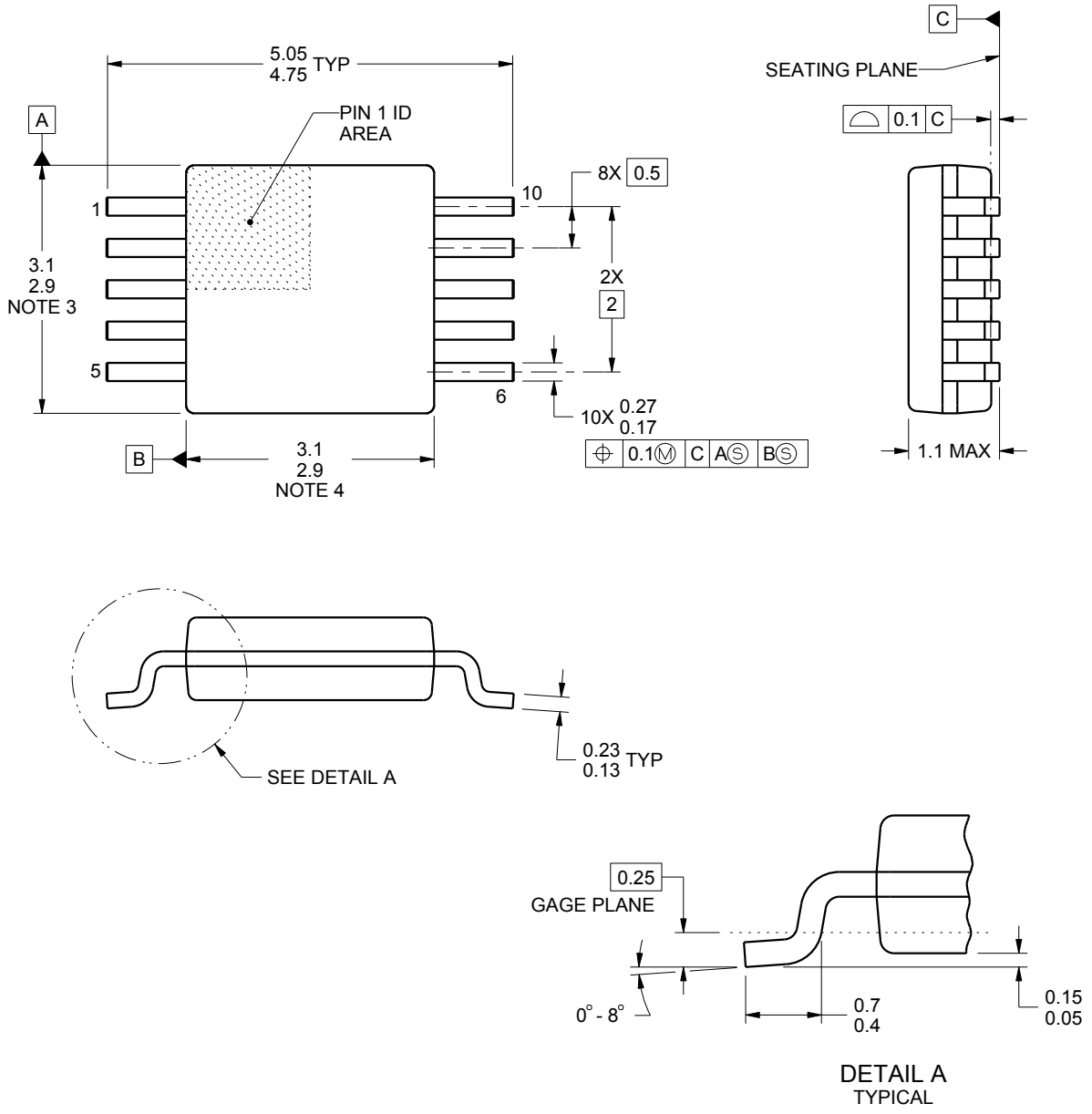
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5022QDGSRQ1	VSSOP	DGS	10	1000	208.0	191.0	35.0
LM5022QDGSTQ1	VSSOP	DGS	10	250	208.0	191.0	35.0

PACKAGE OUTLINE

DGS0010A

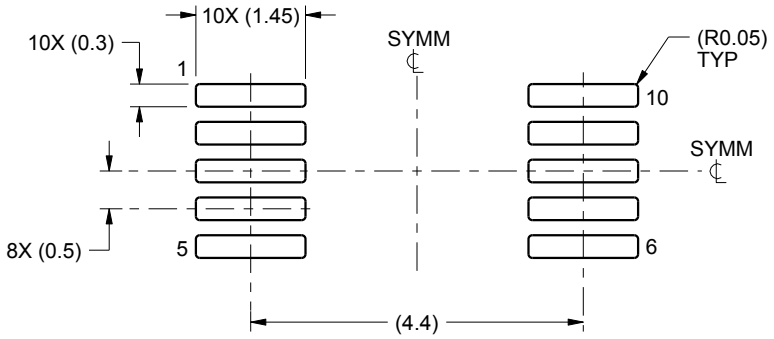
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

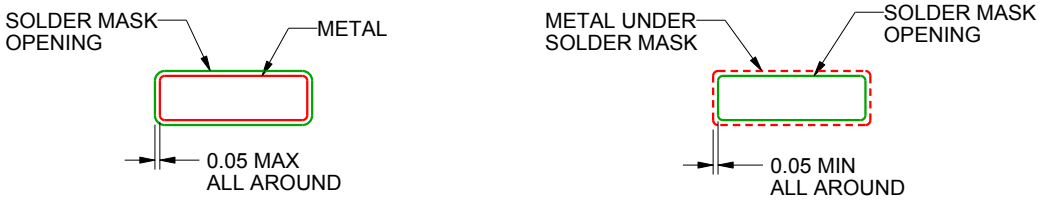


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

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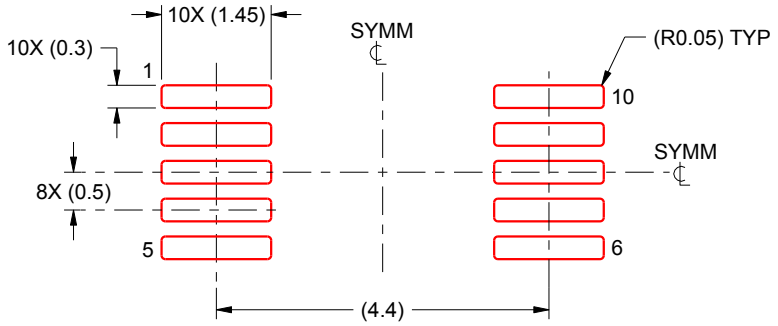
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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