

SN54ALS373A, SN54AS373, SN74ALS373A, SN74AS373 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SDAS083C – APRIL 1982 – REVISED MARCH 2002

- Eight Latches in a Single Package
- 3-State Bus-Driving True Outputs
- Full Parallel Access for Loading
- Buffered Control Inputs
- pnp Inputs Reduce dc Loading on Data Lines

description

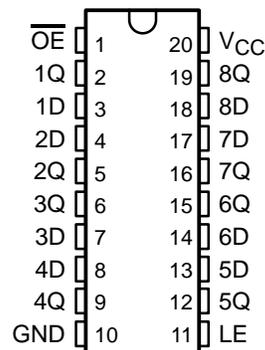
These octal transparent D-type latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

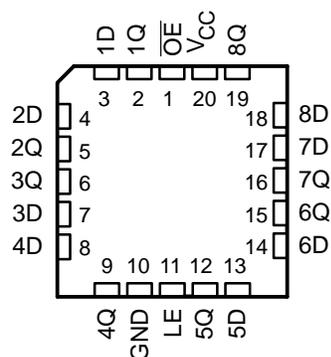
A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without interface or pullup components.

\overline{OE} does not affect internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off.

SN54ALS373A, . . . J OR W PACKAGE
SN54AS373 . . . J PACKAGE
SN74ALS373A, SN74AS373 . . . DW, N, OR NS PACKAGE
(TOP VIEW)



SN54ALS373A, SN54AS373 . . . FK PACKAGE
(TOP VIEW)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54ALS373A, SN54AS373, SN74ALS373A, SN74AS373

OCTAL TRANSPARENT D-TYPE LATCHES

WITH 3-STATE OUTPUTS

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ORDERING INFORMATION

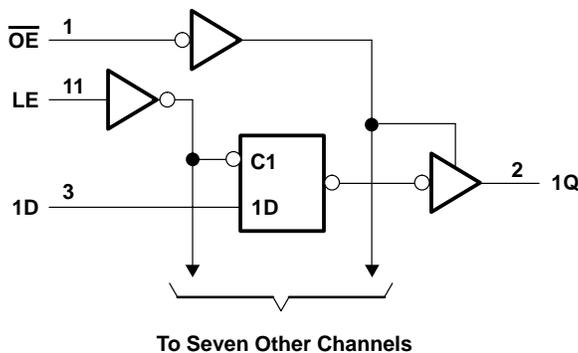
| T _A | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING | |
|----------------|-----------|---------------|-----------------------|------------------|-------|
| 0°C to 70°C | PDIP – N | Tube | SN74ALS373AN | SN74ALS373AN | |
| | | | SN74AS373N | SN74AS373N | |
| | SOIC – DW | Tube | SN74ALS373ADW | ALS373A | |
| | | | SN74ALS373ADWR | | |
| | | | Tape and reel | SN74AS373DW | AS373 |
| | | | | SN74AS373DWR | |
| | SOP – NS | Tape and reel | SN74ALS373ANSR | ALS373A | |
| SN74AS373NSR | | | 74AS373 | | |
| –55°C to 125°C | CDIP – J | Tube | SNJ54ALS373AJ | SNJ54ALS373AJ | |
| | | | SNJ54AS373J | SNJ54AS373J | |
| | CFP – W | Tube | SNJ54ALS373AW | SNJ54ALS373AW | |
| | LCCC – FK | Tube | SNJ54ALS373AFK | SNJ54ALS373AFK | |
| | | | SNJ54AS373FK | SNJ54AS373FK | |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE (each latch)

| INPUTS | | | OUTPUT |
|-----------------|----|---|----------------|
| \overline{OE} | LE | D | Q |
| L | H | H | H |
| L | H | L | L |
| L | L | X | Q ₀ |
| H | X | X | Z |

logic diagram (positive logic)



SN54ALS373A, SN54AS373, SN74ALS373A, SN74AS373 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (SN54ALS373A, SN74ALS373A) (unless otherwise noted)†

| | | |
|--|------------------|--------|
| Supply voltage, V_{CC} | 7 V | |
| Input voltage, V_I | 7 V | |
| Voltage applied to any output in the high state or power-off state | 5.5 V | |
| Package thermal impedance, θ_{JA} (see Note 1): | DW package | 58°C/W |
| | N package | 69°C/W |
| | NS package | 60°C/W |
| Storage temperature range, T_{stg} | –65°C to 150°C | |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

| | | SN54ALS373A | | | SN74ALS373A | | | UNIT |
|----------|--------------------------------|-------------|-----|-----|-------------|-----|------|------|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V_{CC} | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| V_{IH} | High-level input voltage | 2 | | | 2 | | | V |
| V_{IL} | Low-level input voltage | | | 0.7 | | | 0.8 | V |
| I_{OH} | High-level output current | | | –1 | | | –2.6 | mA |
| I_{OL} | Low-level output current | | | 12 | | | 24 | mA |
| T_A | Operating free-air temperature | –55 | | 125 | 0 | | 70 | °C |

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

| | | SN54ALS373A | | SN74ALS373A | | UNIT |
|-------------|-----------------------------|-------------|-----|-------------|-----|------|
| | | MIN | MAX | MIN | MAX | |
| f_{clock} | Clock frequency | | | | | MHz |
| t_w | Pulse duration, LE high | 12 | | 10 | | ns |
| t_{su} | Setup time, data before LE↓ | 10 | | 10 | | ns |
| t_h | Hold time, data after LE↓ | 7 | | 7 | | ns |



SN54ALS373A, SN54AS373, SN74ALS373A, SN74AS373

OCTAL TRANSPARENT D-TYPE LATCHES

WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SN54ALS373A | | | SN74ALS373A | | | UNIT |
|-----------------|---|---------------------------|-------------|------|------|-------------|------|-----|---------------|
| | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| V_{IK} | $V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$ | | -1.5 | | | -1.5 | | | V |
| V_{OH} | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$, $I_{OH} = -0.4\text{ mA}$ | | $V_{CC}-2$ | | | $V_{CC}-2$ | | | V |
| | $V_{CC} = 4.5\text{ V}$ | $I_{OH} = -1\text{ mA}$ | 2.4 | 3.3 | | | | | |
| | | $I_{OH} = -2.6\text{ mA}$ | | | | 2.4 | 3.2 | | |
| V_{OL} | $V_{CC} = 4.5\text{ V}$ | $I_{OL} = 12\text{ mA}$ | 0.25 | 0.4 | 0.25 | 0.4 | | | |
| | | $I_{OL} = 24\text{ mA}$ | | | | 0.35 | 0.5 | | |
| I_{OZH} | $V_{CC} = 5.5\text{ V}$, | $V_O = 2.7\text{ V}$ | 20 | | | 20 | | | μA |
| I_{OZL} | $V_{CC} = 5.5\text{ V}$, | $V_O = 0.4\text{ V}$ | -20 | | | -20 | | | μA |
| I_I | $V_{CC} = 5.5\text{ V}$, | $V_I = 7\text{ V}$ | 0.1 | | | 0.1 | | | mA |
| I_{IH} | $V_{CC} = 5.5\text{ V}$, | $V_I = 2.7\text{ V}$ | 20 | | | 20 | | | μA |
| I_{IL} | $V_{CC} = 5.5\text{ V}$, | $V_I = 0.4\text{ V}$ | -0.1 | | | -0.1 | | | mA |
| $I_{O\ddagger}$ | $V_{CC} = 5.5\text{ V}$, | $V_O = 2.25\text{ V}$ | -20 | -112 | -30 | -112 | | | mA |
| I_{CC} | $V_{CC} = 5.5\text{ V}$ | Outputs high | 9 | 16 | 9 | 16 | | | |
| | | Outputs low | 16 | 25 | 16 | 25 | | | |
| | | Outputs disabled | 17 | 27 | 17 | 27 | | | |

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current, I_{OS} .

switching characteristics (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$, $C_L = 50\text{ pF}$, $R_1 = 500\ \Omega$, $R_2 = 500\ \Omega$, $T_A = \text{MIN to MAX}\S$ | | | | UNIT |
|-----------|-----------------|-------------|--|-----|-------------|-----|------|
| | | | SN54ALS373A | | SN74ALS373A | | |
| | | | MIN | MAX | MIN | MAX | |
| t_{PLH} | D | Q | 2 | 17 | 2 | 12 | ns |
| t_{PHL} | | | 1 | 19 | 4 | 16 | |
| t_{PLH} | LE | Any Q | 6 | 29 | 6 | 22 | ns |
| t_{PHL} | | | 1 | 27 | 7 | 23 | |
| t_{PZH} | \overline{OE} | Any Q | 6 | 22 | 1 | 18 | ns |
| t_{PZL} | | | 5 | 24 | 5 | 20 | |
| t_{PHZ} | \overline{OE} | Any Q | 2 | 16 | 1 | 10 | ns |
| t_{PLZ} | | | 2 | 24 | 2 | 12 | |

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



SN54ALS373A, SN54AS373, SN74ALS373A, SN74AS373 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (SN54AS373, SN74AS373) (unless otherwise noted)†

| | | |
|--|------------------|--------|
| Supply voltage, V_{CC} | 7 V | |
| Input voltage, V_I | 7 V | |
| Voltage applied to any output in the high state or power-off state | 5.5 V | |
| Package thermal impedance, θ_{JA} (see Note 1): | DW package | 58°C/W |
| | N package | 69°C/W |
| | NS package | 60°C/W |
| Storage temperature range, T_{stg} | –65°C to 150°C | |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 2: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

| | | SN54AS373 | | | SN74AS373 | | | UNIT |
|----------|--------------------------------|-----------|-----|-----|-----------|-----|-----|------|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V_{CC} | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| V_{IH} | High-level input voltage | 2 | | | 2 | | | V |
| V_{IL} | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| I_{OH} | High-level output current | | | –12 | | | –15 | mA |
| I_{OL} | Low-level output current | | | 32 | | | 48 | mA |
| T_A | Operating free-air temperature | –55 | | 125 | 0 | | 70 | °C |

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

| | | SN54AS373 | | SN74AS373 | | UNIT |
|-------------|-----------------------------|-----------|-----|-----------|-----|------|
| | | MIN | MAX | MIN | MAX | |
| f_{clock} | Clock frequency | | | | | MHz |
| t_w | Pulse duration, LE high | 5.5* | | 4.5* | | ns |
| t_{su} | Setup time, data before LE↓ | 2* | | 2* | | ns |
| t_h | Hold time, data after LE↓ | 3* | | 3* | | ns |

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.



SN54ALS373A, SN54AS373, SN74ALS373A, SN74AS373

OCTAL TRANSPARENT D-TYPE LATCHES

WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SN54AS373 | | | SN74AS373 | | | UNIT |
|-----------------|---|--------------------------|------------|------|-----|------------|------|-----|---------------|
| | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| V_{IK} | $V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$ | | -1.2 | | | -1.2 | | | V |
| V_{OH} | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$, $I_{OH} = -2\text{ mA}$ | | $V_{CC}-2$ | | | $V_{CC}-2$ | | | V |
| | $V_{CC} = 4.5\text{ V}$ | $I_{OH} = -12\text{ mA}$ | 2.4 | 3.2 | | | | | |
| | | $I_{OH} = -15\text{ mA}$ | | | | | 2.4 | 3.3 | |
| V_{OL} | $V_{CC} = 4.5\text{ V}$ | $I_{OL} = 32\text{ mA}$ | 0.27 | | 0.5 | | | | V |
| | | $I_{OL} = 48\text{ mA}$ | | | | | 0.32 | 0.5 | |
| I_{OZH} | $V_{CC} = 5.5\text{ V}$, | $V_O = 2.7\text{ V}$ | 50 | | | 50 | | | μA |
| I_{OZL} | $V_{CC} = 5.5\text{ V}$, | $V_O = 0.4\text{ V}$ | -50 | | | -50 | | | μA |
| I_I | $V_{CC} = 5.5\text{ V}$, | $V_I = 7\text{ V}$ | 0.1 | | | 0.1 | | | mA |
| I_{IH} | $V_{CC} = 5.5\text{ V}$, | $V_I = 2.7\text{ V}$ | 20 | | | 20 | | | μA |
| I_{IL} | $V_{CC} = 5.5\text{ V}$, | $V_I = 0.4\text{ V}$ | -0.02 | -0.5 | | -0.02 | -0.5 | | mA |
| $I_{O\ddagger}$ | $V_{CC} = 5.5\text{ V}$, | $V_O = 2.25\text{ V}$ | -30 | -112 | | -30 | -112 | | mA |
| I_{CC} | $V_{CC} = 5.5\text{ V}$ | Outputs high | 55 | 90 | | 55 | 90 | | mA |
| | | Outputs low | 55 | 85 | | 55 | 85 | | |
| | | Outputs disabled | 65 | 100 | | 65 | 100 | | |

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current, I_{OS} .

switching characteristics (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$, $C_L = 50\text{ pF}$, $R_1 = 500\ \Omega$, $R_2 = 500\ \Omega$, $T_A = \text{MIN to MAX}\S$ | | | | UNIT |
|-----------|-----------------|-------------|--|------|-----------|------|------|
| | | | SN54AS373 | | SN74AS373 | | |
| | | | MIN | MAX | MIN | MAX | |
| t_{PLH} | D | Q | 3 | 9 | 3.5 | 6 | ns |
| t_{PHL} | | | 3 | 8 | 3.5 | 6 | |
| t_{PLH} | LE | Any Q | 6.5 | 14.5 | 6.5 | 11.5 | ns |
| t_{PHL} | | | 5 | 9 | 5 | 7.5 | |
| t_{PZH} | \overline{OE} | Any Q | 2 | 7.5 | 2 | 6.5 | ns |
| t_{PZL} | | | 4.5 | 10.5 | 4.5 | 9.5 | |
| t_{PHZ} | \overline{OE} | Any Q | 3 | 10 | 3 | 6.5 | ns |
| t_{PLZ} | | | 3 | 8 | 3 | 7 | |

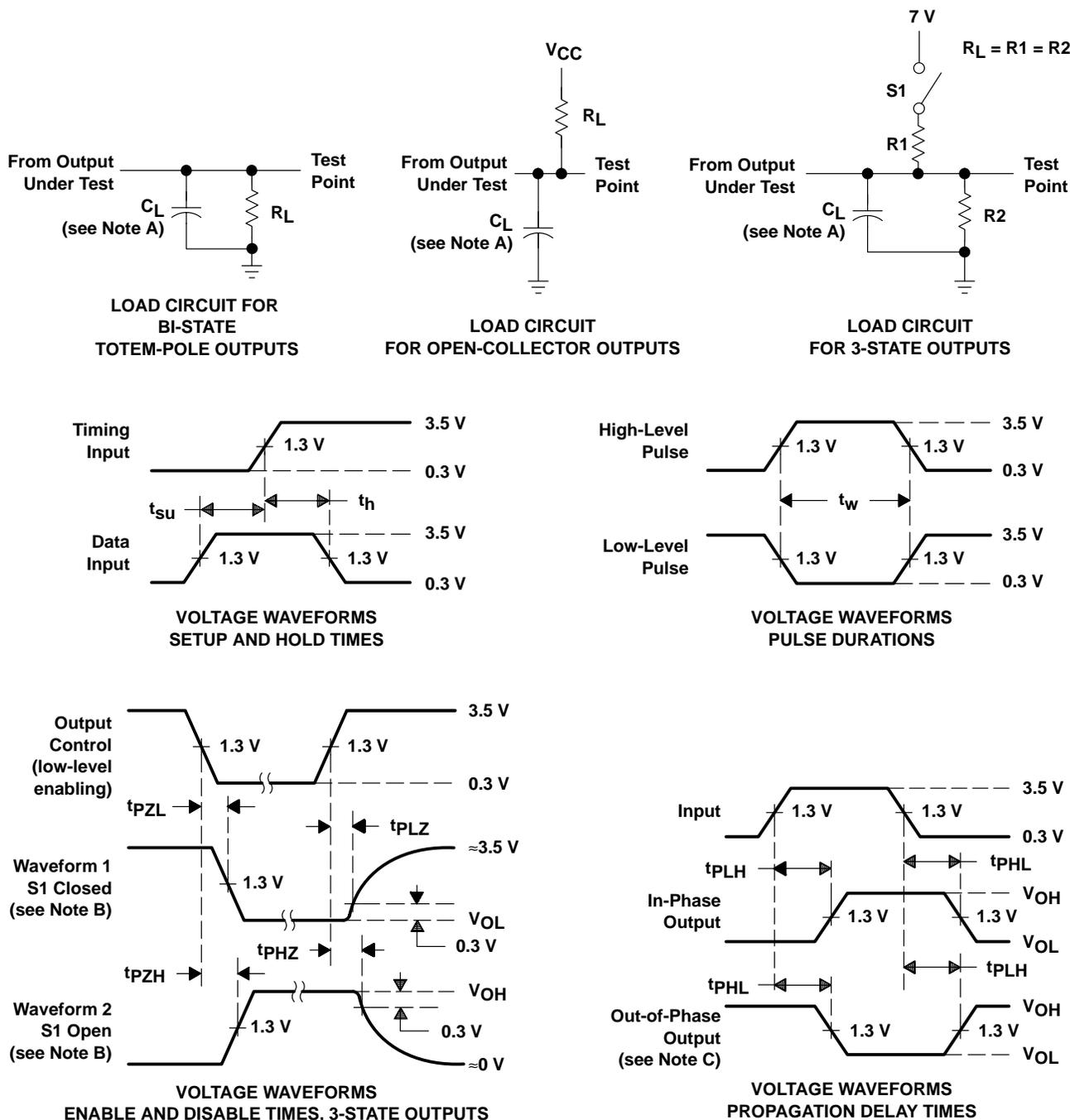
§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



SN54ALS373A, SN54AS373, SN74ALS373A, SN74AS373 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
 D. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|------------------|--------------------------------------|----------------------|--------------|---------------------------------|-------------------------|
| 83020012A | ACTIVE | LCCC | FK | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 83020012A SNJ54ALS 373AFK | Samples |
| 8302001RA | ACTIVE | CDIP | J | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 8302001RA SNJ54ALS373AJ | Samples |
| JM38510/37203B2A | ACTIVE | LCCC | FK | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 37203B2A | Samples |
| JM38510/37203BRA | ACTIVE | CDIP | J | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 37203BRA | Samples |
| M38510/37203B2A | ACTIVE | LCCC | FK | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 37203B2A | Samples |
| M38510/37203BRA | ACTIVE | CDIP | J | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 37203BRA | Samples |
| SN54ALS373AJ | ACTIVE | CDIP | J | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | SN54ALS373AJ | Samples |
| SN74ALS373ADBR | ACTIVE | SSOP | DB | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | G373A | Samples |
| SN74ALS373ADW | ACTIVE | SOIC | DW | 20 | 25 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS373A | Samples |
| SN74ALS373ADWR | ACTIVE | SOIC | DW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS373A | Samples |
| SN74ALS373AN | ACTIVE | PDIP | N | 20 | 20 | RoHS & Non-Green | NIPDAU | N / A for Pkg Type | 0 to 70 | SN74ALS373AN | Samples |
| SN74ALS373ANSR | ACTIVE | SO | NS | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS373A | Samples |
| SN74AS373N | ACTIVE | PDIP | N | 20 | 20 | RoHS & Non-Green | NIPDAU | N / A for Pkg Type | 0 to 70 | SN74AS373N | Samples |
| SN74AS373NSR | ACTIVE | SO | NS | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74AS373 | Samples |
| SNJ54ALS373AFK | ACTIVE | LCCC | FK | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 83020012A SNJ54ALS 373AFK | Samples |
| SNJ54ALS373AJ | ACTIVE | CDIP | J | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 8302001RA SNJ54ALS373AJ | Samples |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54ALS373A, SN74ALS373A :

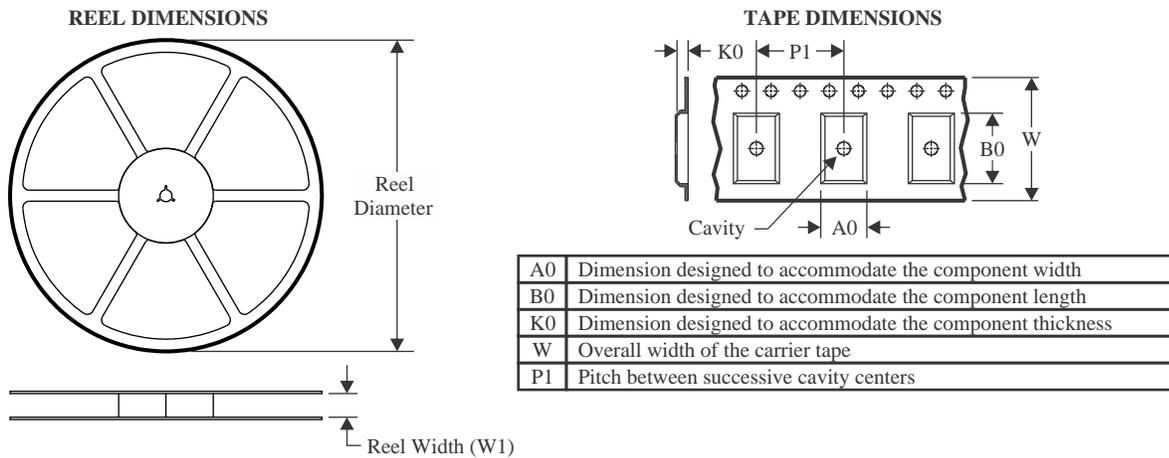
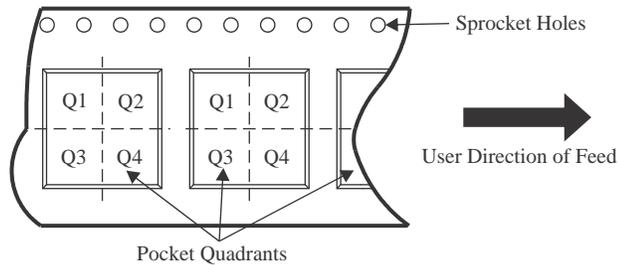
● Catalog : [SN74ALS373A](#)

● Military : [SN54ALS373A](#)

NOTE: Qualified Version Definitions:

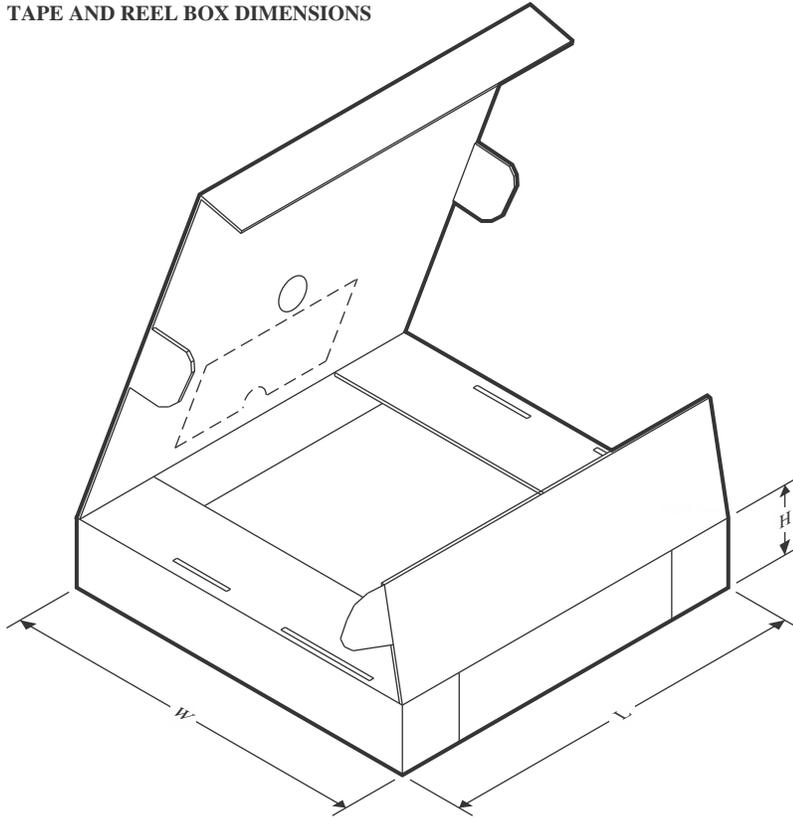
● Catalog - TI's standard catalog product

- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


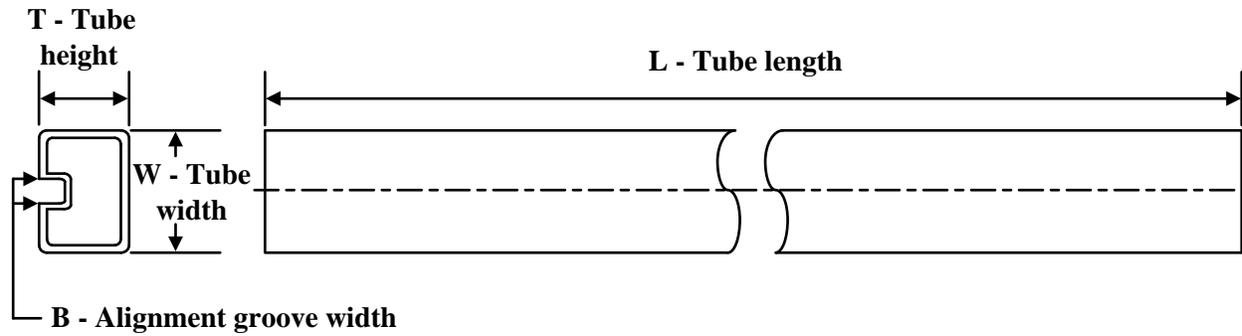
*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74ALS373ADBR | SSOP | DB | 20 | 2000 | 330.0 | 16.4 | 8.2 | 7.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74ALS373ADWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74ALS373ANSR | SO | NS | 20 | 2000 | 330.0 | 24.4 | 8.4 | 13.0 | 2.5 | 12.0 | 24.0 | Q1 |
| SN74AS373NSR | SO | NS | 20 | 2000 | 330.0 | 24.4 | 8.4 | 13.0 | 2.5 | 12.0 | 24.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74ALS373ADBR | SSOP | DB | 20 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74ALS373ADWR | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74ALS373ANSR | SO | NS | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74AS373NSR | SO | NS | 20 | 2000 | 367.0 | 367.0 | 45.0 |

TUBE


*All dimensions are nominal

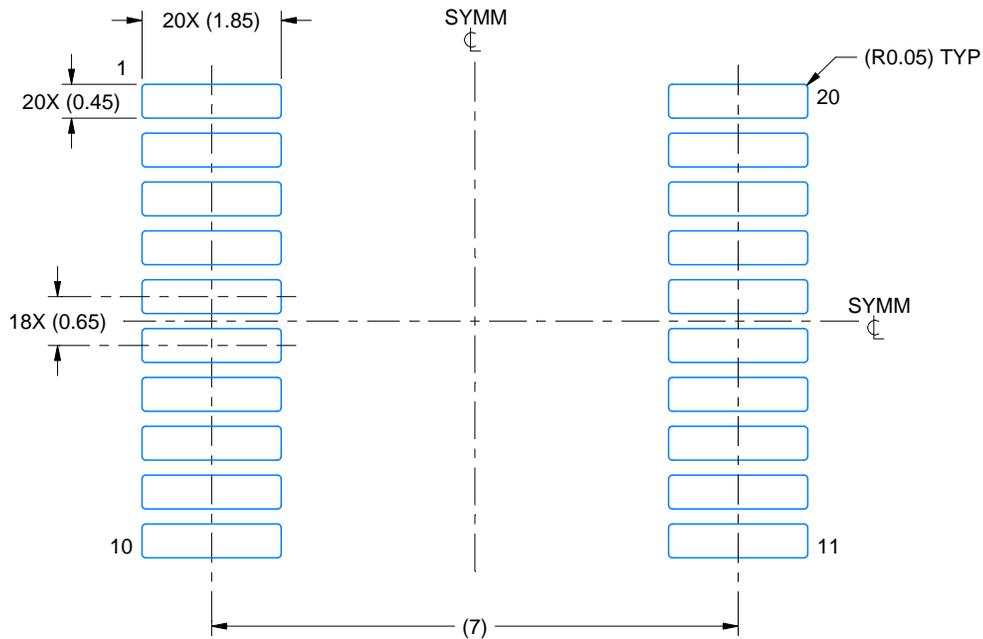
| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|------------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| 83020012A | FK | LCCC | 20 | 1 | 506.98 | 12.06 | 2030 | NA |
| JM38510/37203B2A | FK | LCCC | 20 | 1 | 506.98 | 12.06 | 2030 | NA |
| M38510/37203B2A | FK | LCCC | 20 | 1 | 506.98 | 12.06 | 2030 | NA |
| SN74ALS373ADW | DW | SOIC | 20 | 25 | 507 | 12.83 | 5080 | 6.6 |
| SN74ALS373AN | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| SN74AS373N | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| SNJ54ALS373AFK | FK | LCCC | 20 | 1 | 506.98 | 12.06 | 2030 | NA |

EXAMPLE BOARD LAYOUT

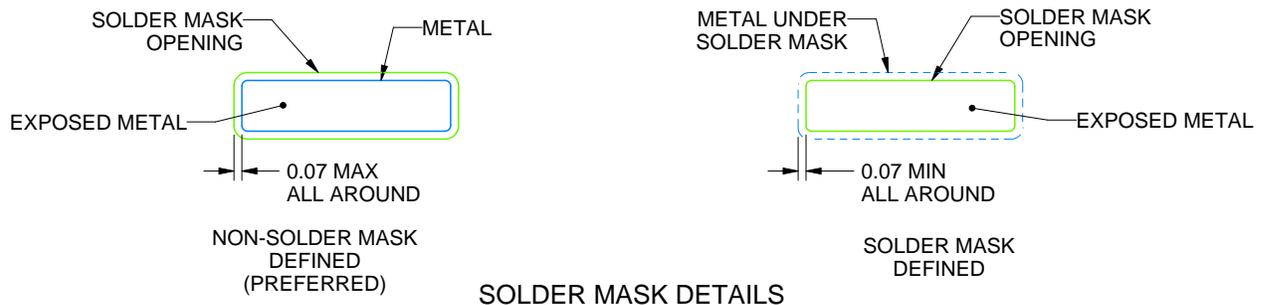
DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

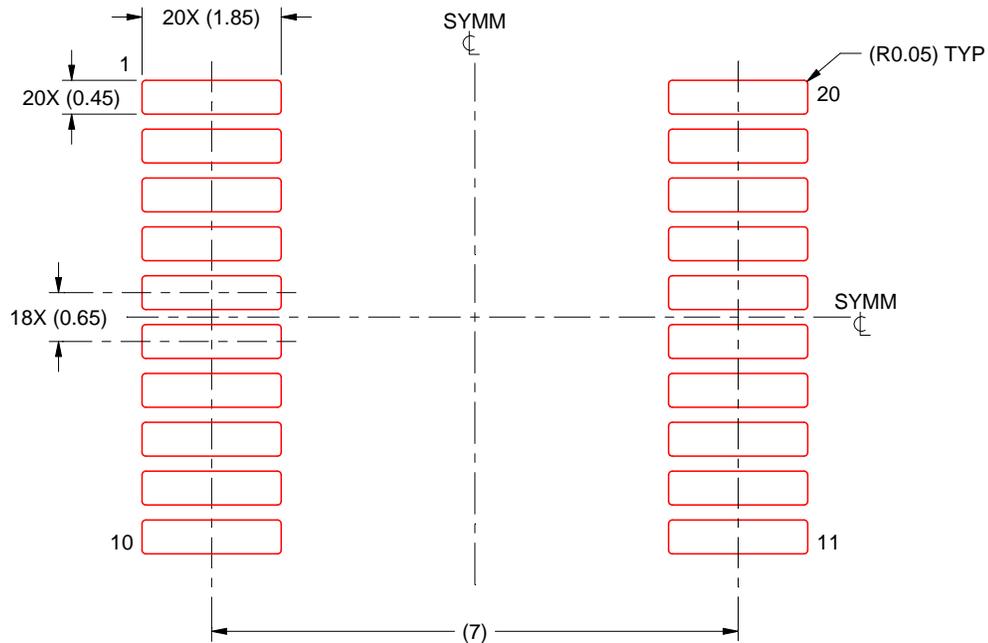
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

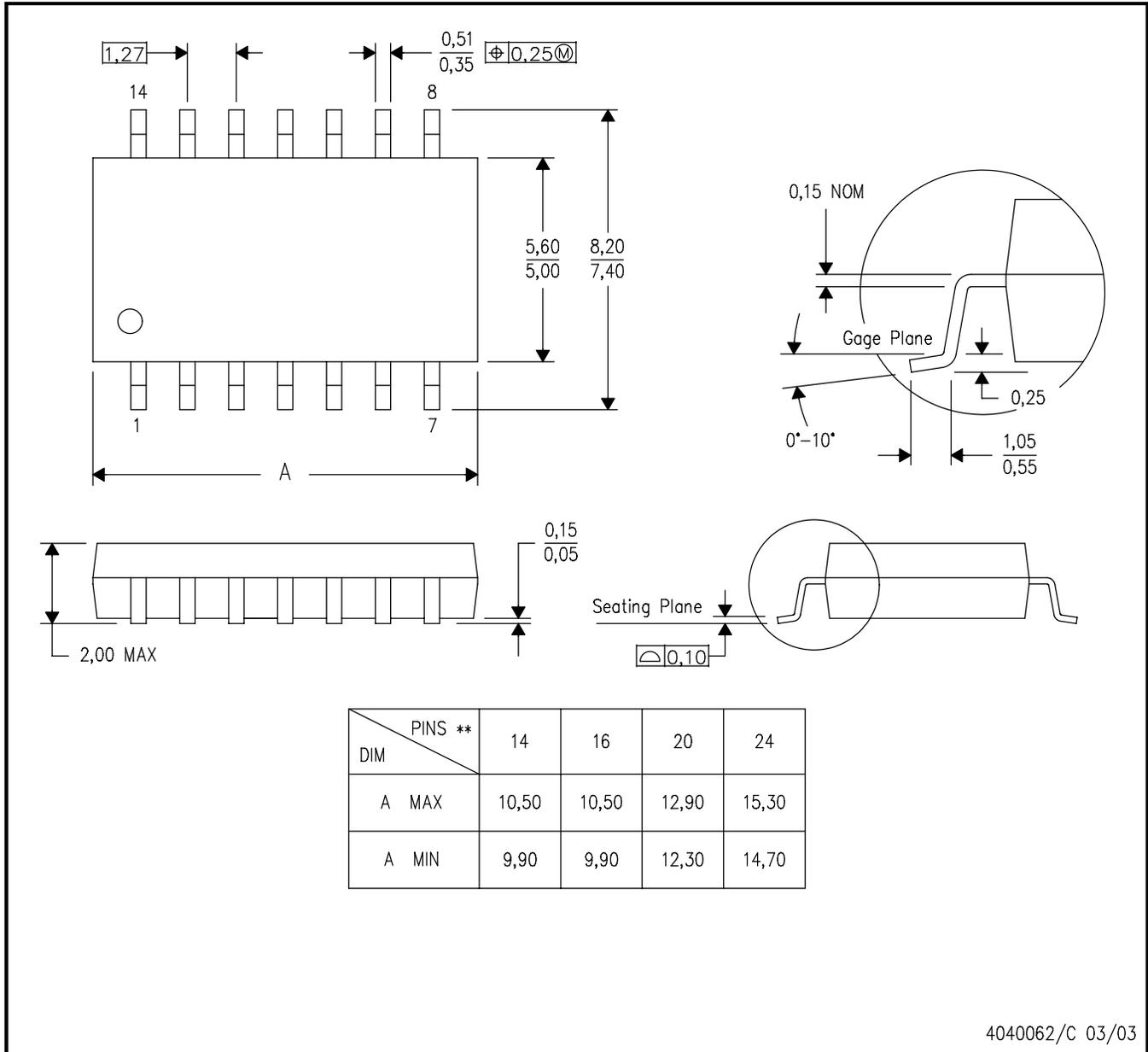
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

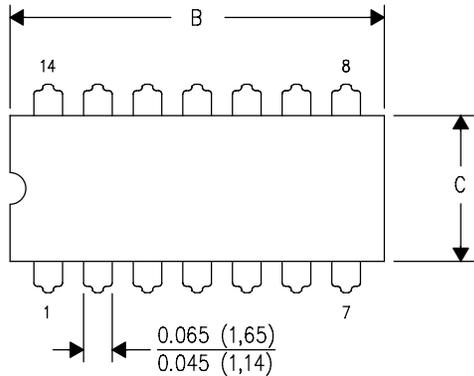
14-PINS SHOWN



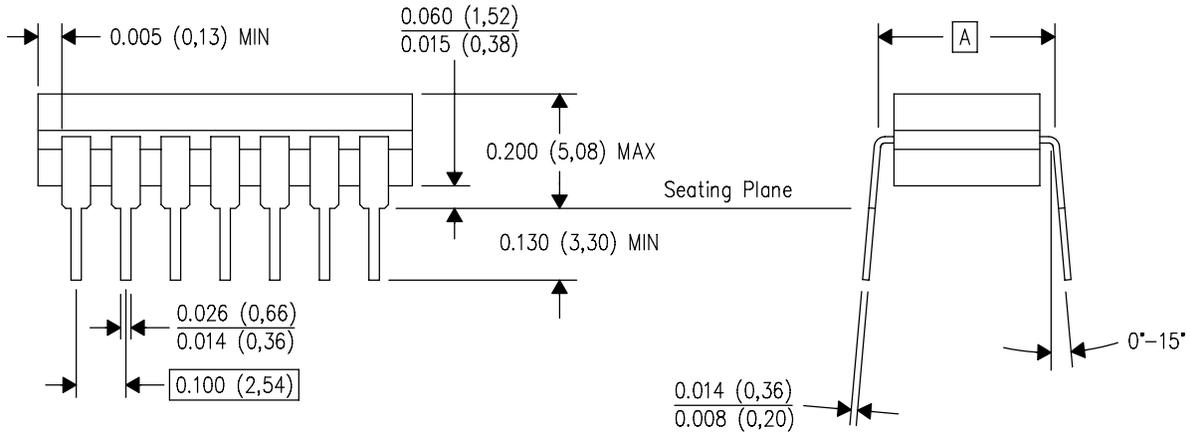
- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R-GDIP-T**)
14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

GENERIC PACKAGE VIEW

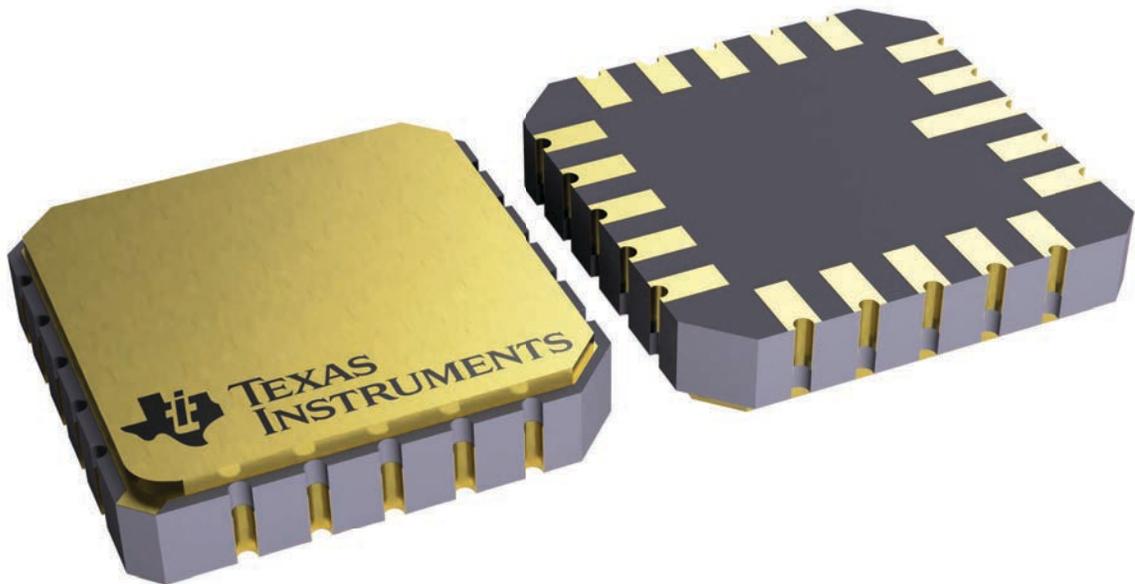
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

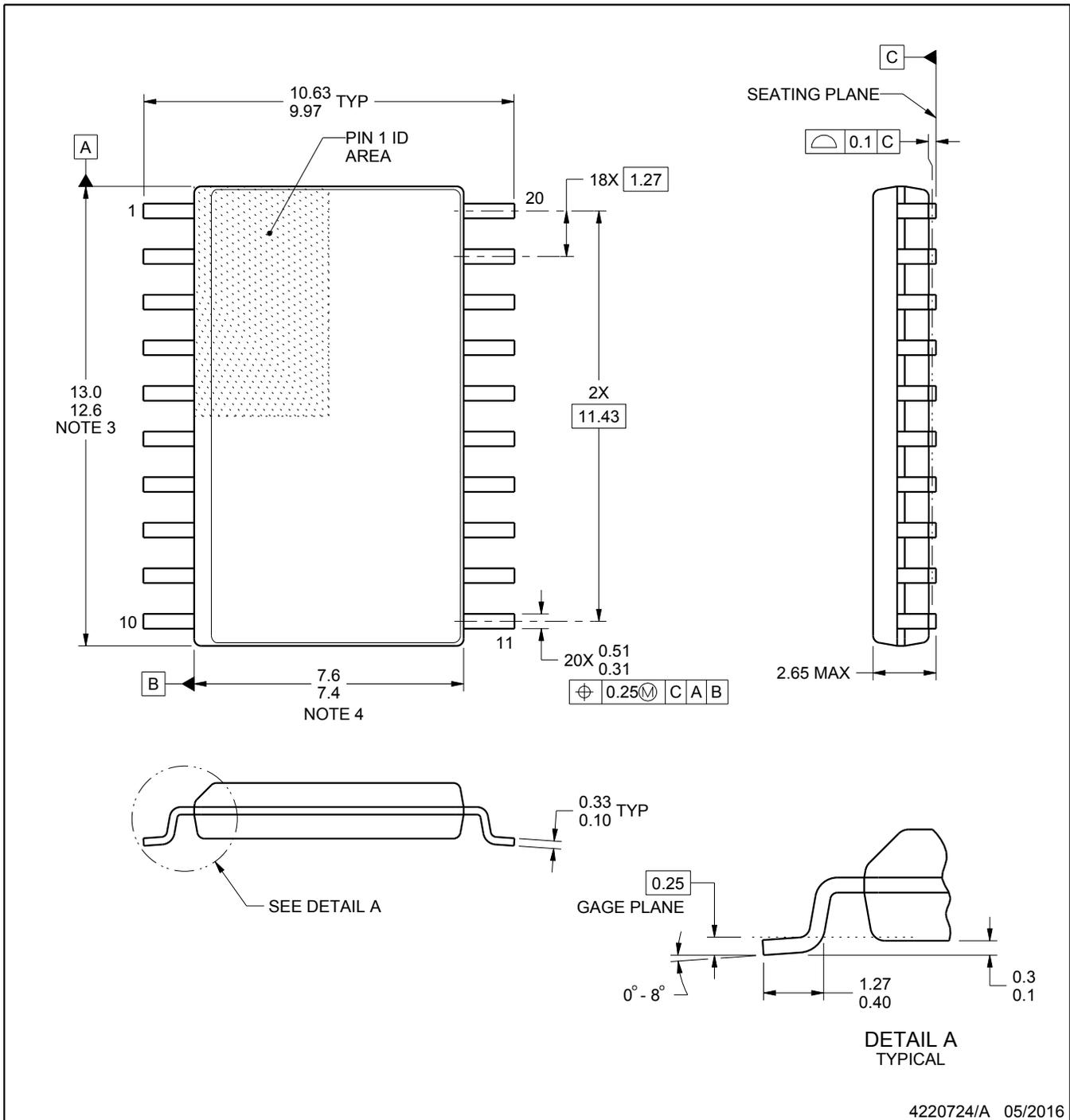
DW0020A



PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

NOTES:

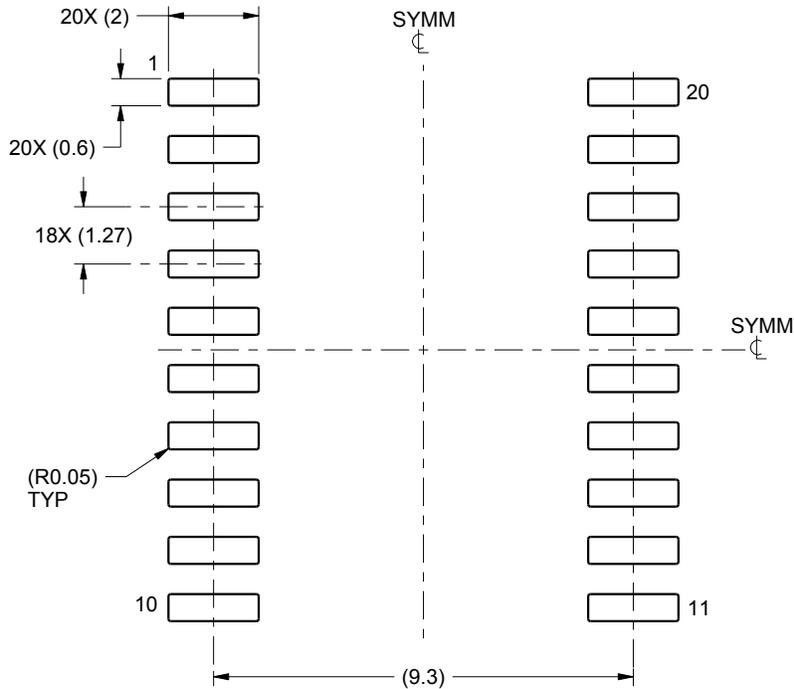
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

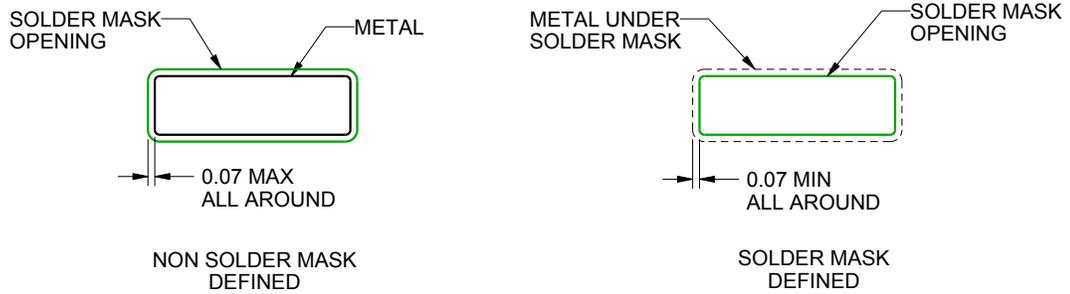
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

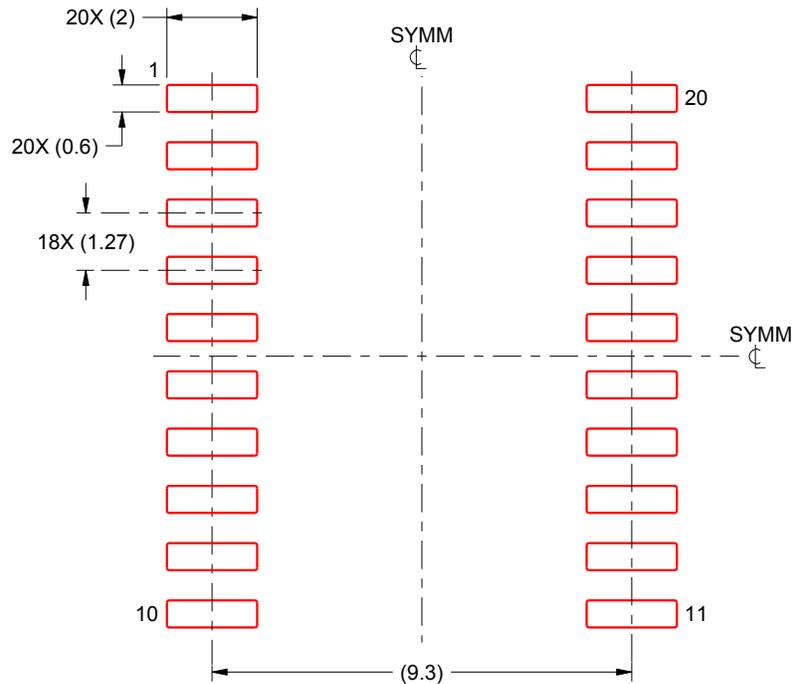
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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