# MOSFET – Dual N-Channel, Dual SO-8FL 40 V, 10 mΩ, 53 A

## **Features**

- Small Footprint (5x6 mm) for Compact Designs
- Low R<sub>DS(on)</sub> to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- NVMFD5853NWF Wettable Flanks Product
- AEC-Q101 Qualified and PPAP Capable
- This is a Pb-Free and Halogen-Free Device

## MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit	
Drain-to-Source Voltage			$V_{DSS}$	40	V	
Gate-to-Source Voltage	9		V <sub>GS</sub>	±20	V	
Continuous Drain Cur-	Steady State	T <sub>C</sub> = 25°C	I <sub>D</sub>	53	Α	
rent $R_{\theta JC}$ (Notes 1, 2, 3)		T <sub>C</sub> = 100°C		37		
Power Dissipation		T <sub>C</sub> = 25°C	$P_{D}$	58	W	
R <sub>θJC</sub> (Notes 1, 2)		T <sub>C</sub> = 100°C		29		
Continuous Drain Cur-		T <sub>A</sub> = 25°C	I <sub>D</sub>	12	Α	
rent R <sub>θJA</sub> (Notes 1, 2 & 3)  Power Dissipation	Steady State	T <sub>A</sub> = 100°C		8.7		
		T <sub>A</sub> = 25°C	$P_{D}$	3.1	W	
R <sub>θJA</sub> (Notes 1 & 2)		T <sub>A</sub> = 100°C		1.6		
Pulsed Drain Current	T <sub>A</sub> = 25	°C, t <sub>p</sub> = 10 μs	I <sub>DM</sub>	165	Α	
Operating Junction and Storage Temperature			T <sub>J</sub> , T <sub>stg</sub>	-55 to 175	°C	
Source Current (Body Diode)			Is	53	Α	
Single Pulse Drain-to-Source Avalanche Energy (T <sub>J</sub> = 25°C, I <sub>L(pk)</sub> = 28.3 A, L = 0.1 mH)			E <sub>AS</sub>	40	mJ	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		TL	260	°C		

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

## THERMAL RESISTANCE MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Value	Unit
Junction-to-Case - Steady State (Note 2)	$R_{\theta JC}$	2.6	°C/W
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	48	

- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- 2. Surface-mounted on FR4 board using a 650 mm<sup>2</sup>, 2 oz. Cu pad.
- 3. Continuous DC current rating. Maximum current for pulses as long as 1 second are higher but are dependent on pulse duration and duty cycle.

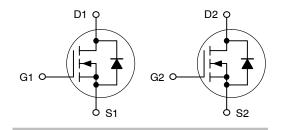


## ON Semiconductor®

## http://onsemi.com

V <sub>(BR)DSS</sub>	R <sub>DS(on)</sub> MAX	I <sub>D</sub> MAX
40 V	10 mΩ @ 10 V	53 A

#### **Dual N-Channel**







5853N = NVMFD5853N 5853WF = NVMFD5853NWF A = Assembly Location Y = Year W = Work Week

W = Work Week
ZZ = Lot Traceability

## **ORDERING INFORMATION**

Device	Package	Shipping <sup>†</sup>
NVMFD5853NT1G	DFN8 (Pb-Free)	1500 / Tape & Reel
NVMFD5853NWFT1G	DFN8 (Pb-Free)	1500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# **ELECTRICAL CHARACTERISTICS** (T<sub>J</sub> = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Тур	Max	Unit
OFF CHARACTERISTICS	ı		I			1	
Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA		40			٧
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> /T <sub>J</sub>				41.5		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V.	T <sub>J</sub> = 25°C			1.0	μΑ
		$V_{GS} = 0 V$ , $V_{DS} = 40 V$	T <sub>J</sub> = 125°C			100	1
Gate-to-Source Leakage Current	I <sub>GSS</sub>	$V_{DS} = 0 V, V_{GS}$	= ±20 V			±100	nA
ON CHARACTERISTICS (Note 4)							
Gate Threshold Voltage	V <sub>GS(TH)</sub>	$V_{GS} = V_{DS}, I_D =$	250 μΑ	2.0		4.0	V
Threshold Temperature Coefficient	V <sub>GS(TH)</sub> /T <sub>J</sub>				-7.2		mV/°C
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub>	= 15 A		8.4	10	mΩ
Forward Transconductance	9FS	$V_{DS} = 5 \text{ V}, I_D =$	= 15 A		44		S
CHARGES AND CAPACITANCES	•					•	•
Input Capacitance	C <sub>iss</sub>				1225		pF
Output Capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V, f = 1.0 MH	z, V <sub>DS</sub> = 25 V		150		1
Reverse Transfer Capacitance	C <sub>rss</sub>				100		1
Total Gate Charge	Q <sub>G(TOT)</sub>				24		nC
Threshold Gate Charge	Q <sub>G(TH)</sub>	$V_{GS} = 10 \text{ V}, V_{DS} = 32 \text{ V},$ $I_{D} = 15 \text{ A}$			1.5		1
Gate-to-Source Charge	Q <sub>GS</sub>				5.2		1
Gate-to-Drain Charge	$Q_{GD}$				6.6		1
Plateau Voltage	V <sub>GP</sub>				4.1		V
SWITCHING CHARACTERISTICS (No	ote 5)						
Turn-On Delay Time	t <sub>d(on)</sub>	$V_{GS} = 10 \text{ V}, V_{DS} = 20 \text{ V},$ $I_{D} = 15 \text{ A}, R_{G} = 2.5 \Omega$			9		ns
Rise Time	t <sub>r</sub>				20		1
Turn-Off Delay Time	t <sub>d(off)</sub>				21		1
Fall Time	t <sub>f</sub>				3		1
DRAIN-SOURCE DIODE CHARACTE	RISTICS						
Forward Diode Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0 V,	T <sub>J</sub> = 25°C		0.82	1.1	٧
		I <sub>S</sub> = 15 A	T <sub>J</sub> = 125°C		0.72		1
Reverse Recovery Time	t <sub>RR</sub>	$V_{GS} = 0 \text{ V, } d_{IS}/d_t = 100 \text{ A/}\mu\text{s,}$ $I_S = 15 \text{ A}$			16		ns
Charge Time	t <sub>a</sub>				10		
Discharge Time	t <sub>b</sub>				6		1
•							

<sup>4.</sup> Pulse Test: pulse width = 300  $\mu$ s, duty cycle  $\leq$  2%. 5. Switching characteristics are independent of operating junction temperatures.

## TYPICAL CHARACTERISTICS

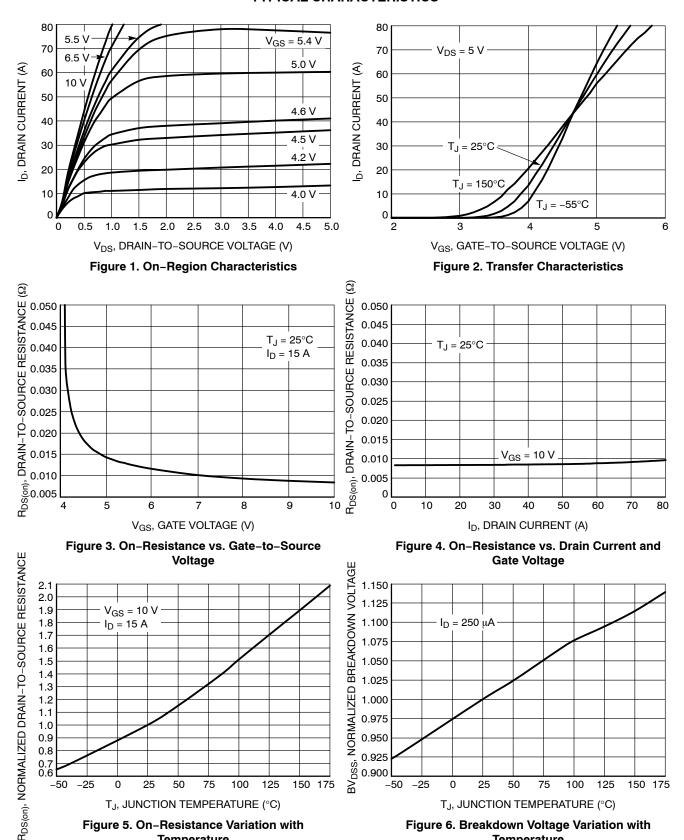


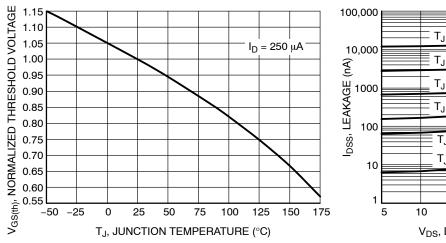
Figure 6. Breakdown Voltage Variation with

**Temperature** 

Figure 5. On-Resistance Variation with

**Temperature** 

#### **TYPICAL CHARACTERISTICS**



100,000  $T_J = 175^{\circ}C$ 10,000  $T_J = 150^{\circ}C$   $T_J = 100^{\circ}C$   $T_J = 85^{\circ}C$ 10  $T_J = 85^{\circ}C$   $T_J = 50^{\circ}C$   $T_J = 50^{\circ}C$   $T_J = 50^{\circ}C$  $T_J = 50^{\circ}C$ 

Figure 7. Threshold Voltage Variation with Temperature

Figure 8. Drain-to-Source Leakage Current vs. Voltage

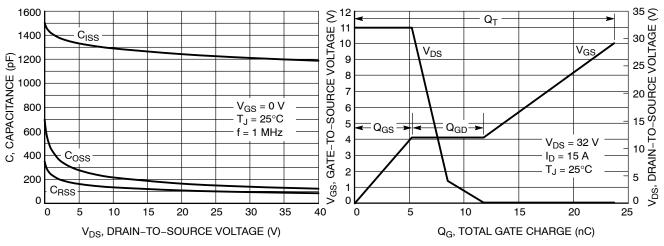


Figure 9. Capacitance Variation

Figure 10. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

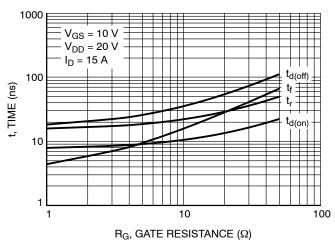


Figure 11. Resistive Switching Time Variation vs. Gate Resistance

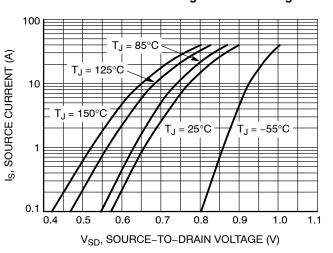
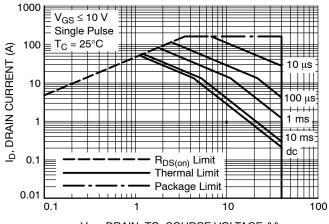


Figure 12. Diode Forward Voltage vs. Current

## **TYPICAL CHARACTERISTICS**



V<sub>DS</sub>, DRAIN-TO-SOURCE VOLTAGE (V)

Figure 13. Maximum Rated Forward Biased Safe Operating Area

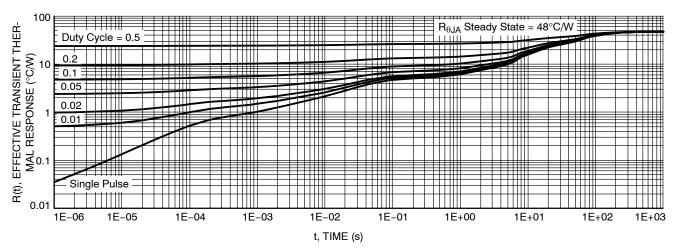
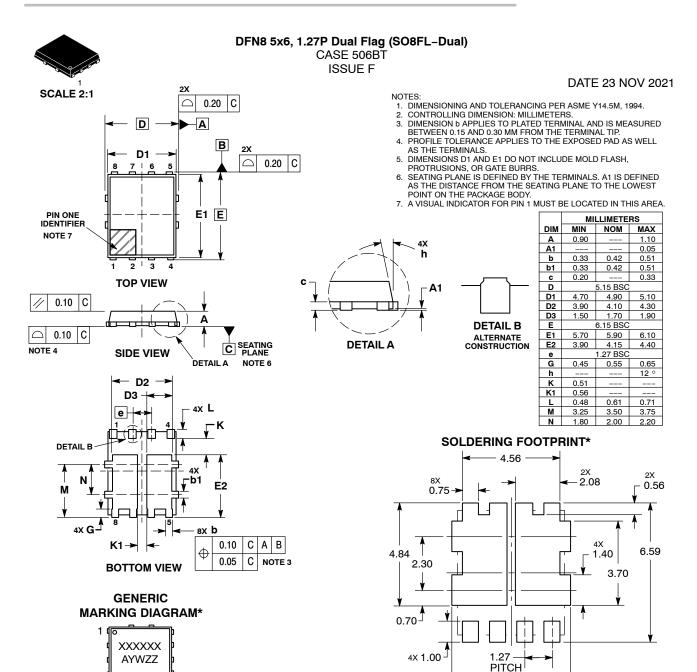


Figure 14. Thermal Impedance (Junction-to-Ambient)





\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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*Tł	nis information is generic. Please refer to
d	evice data sheet for actual part marking.
Ρ	b-Free indicator, "G" or microdot "■", may
0	r may not be present. Some products may
n	ot follow the Generic Marking.

XXXXXX = Specific Device Code

= Work Week

= Lot Traceability

= Year

Υ

W

77

**DOCUMENT NUMBER:** 

= Assembly Location

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DESCRIPTION: DFN8 5X6, 1.27P DUAL FLAG (SO8FL-DUAL)

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