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April 1st, 2010
Renesas Electronics Corporation

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HD74HC Series Common Information

September 2000

Customer Service Division
Semiconductor & Integrated Circuits
Hitachi, Ltd.

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Outline of Hitachi High-Speed CMOS Logic

Features of High-Speed CMOS Logic

Hitachi's HS-CMOS logics–the HD74HC series–and the HCT series based on the EIA/JEDEC specification. Their specification are shown in the Maximum Ratings and the Electrical Characteristics Tables. The HS-CMOS has the characteristics of both standard CMOS logic series and LS-TTL series.

The features of this logic are:

- High-Speed equivalent to the LS-TTL's
- Capable of driving 10LS-TTL loads
  (Capable of driving 15LS-TTL loads in bus drivers)
- Maximum input current of ± 1 μA at 6 V power supply
- Wide supply voltage range: HC series 2 to 6 V
  HCT series 4.5 to 5.5 V
- Wide noise margin
- V_{CC} assurance of Electrical Characteristics at 2.0, 4.5 and 6.0 V
- Low Static Power Consumption 1/2 of EIA/JEDEC

Type Name of High-Speed CMOS Logic

The JEDEC has divided the HS-CMOS's into two types: HC and HCT. The HC type has the CMOS logic level for inputs and outputs with buffers. The HCT type has the TTL logic level for inputs and the outputs have buffers.

The industry-standarized maximum ratings and recommended operating range are shown below. Limits for the static characteristics are shown below (right): Table 1 is in the industry-standard and Table 2 is the Hitachi specifications.

The Hitachi specifications is used throughout this data book. Additional specification are shown in the individual data sheets. Switching characteristics are specified under the following conditions:

- Input pulse voltage: + V_{CC}
- Load capacitance: 50 pF
- Input pulse rise/fall time: 6 ns

Switching times measured from 50% point of input voltage to 50% point of output voltage

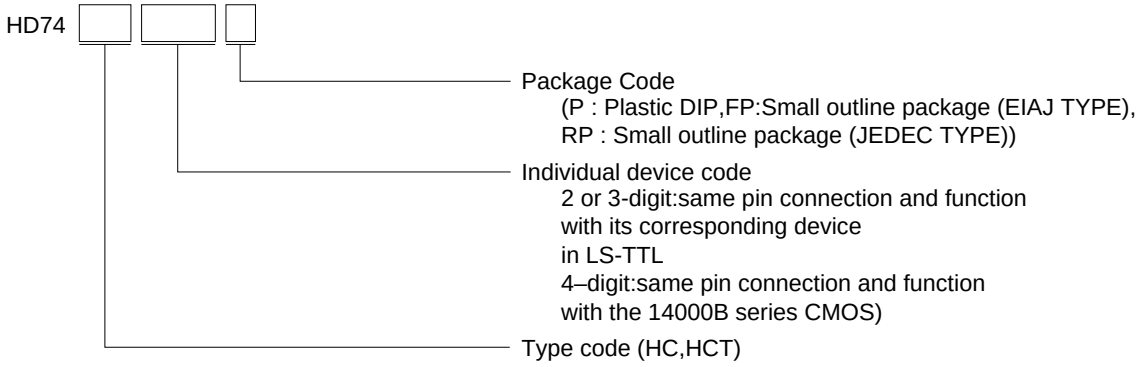
- Three different supply voltages: 2.0, 4.5 and 6.0 V

Input Levels of Each Series Type (V_{CC} = 5 V)

	Input level		
Type	**V_{IH}**	**V_{IL}**	**Remarks**
HC series	3.5 V	1.5 V	—
HCT series	2.0 V	0.8 V	TTL logic level for inputs

Outline of Hitachi High-Speed CMOS Logic

Type Name of HS-CMOS Logic



Absolute Maximum Ratings (Voltages Referenced to GND)

Item	Symbol	Rating	Unit
Supply voltage	V_{CC}	–0.5 to +7	V
I/O voltage	V_{IN}, V_{OUT}	–0.5 to V_{CC} +0.5	V
I/O diode current	I_{IK}, I_{OK}	±20	mA
Output current	I_O	±25	mA
V_{CC}, GND current	I_{CC}, I_{GND}	±50	mA
Power dissipation	P_T	500	mW
Storage temperature Range	Tstg	–65 to +150	˚C

Additional specification values are shown on the individual data sheets.

Recommended Operating Range

HD74HC

Item	Symbol	Rating	Unit	Condition
Supply voltage	V_{CC}	2 to 6	V	
I/O voltage	V_{IN}, V_{OUT}	0 to V_{CC}	V	
Operating temperature	Ta	–40 to +85	˚C	
Input rise/fall time	tr, tf	0 to 1000	ns	V_{CC} = 2.0 V
		0 to 500		V_{CC} = 4.5 V
		0 to 400		V_{CC} = 6.0 V

HD74HCT

Item	Symbol	Rating	Unit	Condition
Supply voltage	V_{CC}	4.5 to 5.5	V	
I/O voltage	V_{IN}, V_{OUT}	0 to V_{CC}	V	
Operating temperature	Ta	–40 to +85	˚C	
Input rise/fall time	tr, tf	0 to 1000	ns	V_{CC} = 2.0 V
		0 to 500		V_{CC} = 4.5 V
		0 to 400		V_{CC} = 6.0 V

HD74HC14, HC132

Item	Symbol	Rating	Unit	Condition
Input rise/fall time	tr, tf	0 to unlimited	ns	V_{CC} = 2.0 V
		0 to unlimited		V_{CC} = 4.5 V
		0 to unlimited		V_{CC} = 6.0 V

HD74HC123A, HC221, HC423A

Item	Symbol	Rating	Unit	Condition
A, B Input rise/fall time	tr, tf	0 to unlimited	ns	V_{CC} = 2.0 V
		0 to unlimited		V_{CC} = 4.5 V
		0 to unlimited		V_{CC} = 6.0 V
CLR Input rise/fall time	tr, tf	0 to 1000	ns	V_{CC} = 2.0 V
		0 to 500		V_{CC} = 4.5 V
		0 to 400		V_{CC} = 6.0 V

HD74HC4538

Item	Symbol	Rating	Unit	Condition
A, B Input rise/fall time	tr, tf	0 to unlimited	ns	V_{CC} = 2.0 V
		0 to unlimited		V_{CC} = 4.5 V
		0 to unlimited		V_{CC} = 6.0 V
CD Input rise/fall time	tr, tf	0 to 1000	ns	V_{CC} = 2.0 V
		0 to 500		V_{CC} = 4.5 V
		0 to 400		V_{CC} = 6.0 V

HD74HC540, HC541

Item	Symbol	Rating	Unit	Condition
A Input rise/fall time	tr, tf	0 to unlimited	ns	V_{cc} = 2.0 V
		0 to unlimited		V_{cc} = 4.5 V
		0 to unlimited		V_{cc} = 6.0 V
$\overline{G}$ Input rise/fall time	tr, tf	0 to 1000	ns	V_{cc} = 2.0 V
		0 to 500		V_{cc} = 4.5 V
		0 to 400		V_{cc} = 6.0 V

Table 1 EIA/JEDEC Format for High-Speed CMOS Specifications

Parameters			Symbol	V_{CC}(V)	Limits +25˚C min	Limits +25˚C max	Limits –40 to +85˚C min	Limits –40 to +85˚C max	Unit	Test Conditions	
Input voltage		HC Series	V_{IH}	2.0	1.5	—	1.5	—	V		
				4.5	3.15	—	3.15	—			
				6.0	4.2	—	4.2	—			
		HCT Series		4.5 to 5.5	2.0	—	2.0	—			
		HC Series	V_{IL}	2.0	—	0.3	—	0.3	V		
				4.5	—	0.9	—	0.9			
				6.0	—	1.2	—	1.2			
		HCT Series		4.5 to 5.5	—	0.8	—	0.8			
Output voltage	HC Series	Standard type	V_{OH}	2.0	1.9	—	1.9	—	V	Vin = V_{IH} or V_{IL}	Iout = –20 µA
				4.5	4.4	—	4.4	—			
				6.0	5.9	—	5.9	—			
				4.5	3.98	—	3.84	—			Iout = –4.0 mA
				6.0	5.48	—	5.34	—			Iout = –5.2 mA
		Bus driver type		2.0	1.9	—	1.9	—		Vin = V_{IH} or V_{IL}	Iout = –20 µA
				4.5	4.4	—	4.4	—			
				6.0	5.9	—	5.9	—			
				4.5	3.98	—	3.84	—			Iout = –6.0 mA
				6.0	5.48	—	5.34	—			Iout = –7.8 mA
	HCT Series	Standard type		4.5	4.4	—	4.4	—		Vin = V_{IH} or V_{IL}	Iout = –20 µA
				4.5	3.98	—	3.84	—			Iout = –4.0 mA
		Bus driver type		4.5	4.4	—	4.4	—		Vin = V_{IH} or V_{IL}	Iout = –20 µA
				4.5	3.98	—	3.84	—			Iout = –6.0 mA
	HC Series	Standard type	V_{OL}	2.0	—	0.1	—	0.1	V	Vin = V_{IH} or V_{IL}	Iout = 20 µA
				4.5	—	0.1	—	0.1			
				6.0	—	0.1	—	0.1			
				4.5	—	0.26	—	0.33			Iout = 4.0 mA
				6.0	—	0.26	—	0.33			Iout = 5.2 mA
		Bus driver type		2.0	—	0.1	—	0.1		Vin = V_{IH} or V_{IL}	Iout = 20 µA
				4.5	—	0.1	—	0.1			
				6.0	—	0.1	—	0.1			

Parameters			Symbol	V_{CC}(V)	Limits +25°C min	+25°C max	–40 to +85°C min	–40 to +85°C max	Unit	Test Conditions	
Output voltage	HC Series	Bus driver type		4.5	—	0.26	—	0.33	V	Vin = V_{IH} or V_{IL}	Iout = 6.0 mA
				6.0	—	0.26	—	0.33			Iout = 7.8 mA
	HCT Series	Standard type		4.5	—	0.1	—	0.1		Vin = V_{IH} or V_{IL}	Iout = 20 µA
				4.5	—	0.26	—	0.33			Iout = 4.0 mA
		Bus driver type		4.5	—	0.1	—	0.1		Vin = V_{IH} or V_{IL}	Iout = 20 µA
				4.5	—	0.26	—	0.33			Iout = 6.0 mA
Input leakage current		HC Series	I_I	6.0	—	±0.1	—	±1.0	µA	Vin = V_{CC} or GND	
		HCT Series		5.5	—	±0.1	—	±1.0			
Analog switch off-state current		HC Series	$I_{S(off)}$	6.0	—	±0.1	—	±1.0	µA	Vin = V_{IH} or V_{IL}	
		HCT Series		5.5	—	±0.1	—	±1.0		$\|V_S\|$ = V_{CC} or V_{CC} – V_{EE}	
3-state output off-state current		HC Series	I_{OZ}	6.0	—	±0.5	—	±5.0	µA	Vin = V_{IH} or V_{IL}	
		HCT Series		5.5	—	±0.5	—	±5.0		Vout = V_{CC} or GND	
Quiescent supply current	HC Series	SSI	I_{CC}	6.0	—	2.0	—	20	µA	Vin = V_{CC} or GND	
		FF		6.0	—	4.0	—	40		Iout = 0 µA	
		MSI		6.0	—	8.0	—	80			
	HCT Series	SSI		5.5	—	2.0	—	20			
		FF		5.5	—	4.0	—	40			
		MSI		5.5	—	8.0	—	80			

Table 2 Hitachi High-Speed CMOS Series Specifications

					Limits					
					+25˚C		–40 to +85˚C			
Parameters			**Symbol**	**V_{CC}(V)**	**min**	**max**	**min**	**max**	**Unit**	**Test Conditions**
Input voltage		HC Series	V_{IH}	2.0	1.5	—	1.5	—	V	
				4.5	3.15	—	3.15	—		
				6.0	4.2	—	4.2	—		
		HCT Series		4.5 to 5.5	2.0	—	2.0	—		
		HC Series	V_{IL}	2.0	—	0.5	—	0.5	V	
				4.5	—	1.35	—	1.35		
				6.0	—	1.8	—	1.8		
		HCT Series		4.5 to 5.5	—	0.8	—	0.8		
Output voltage	HC Series	Standard type	V_{OH}	2.0	1.9	—	1.9	—	V	Vin = V_{IH} or V_{IL} I_{OH} = –20 µA
				4.5	4.4	—	4.4	—		
				6.0	5.9	—	5.9	—		
				4.5	4.18	—	4.13	—		I_{OH} = –4.0 mA
				6.0	5.68	—	5.63	—		I_{OH} = –5.2 mA
		Bus driver type		2.0	1.9	—	1.9	—		Vin = V_{IH} or V_{IL} I_{OH} = –20 µA
				4.5	4.4	—	4.4	—		
				6.0	5.9	—	5.9	—		
				4.5	4.18	—	4.13	—		I_{OH} = –6.0 mA
				6.0	5.68	—	5.63	—		I_{OH} = –7.8 mA
	HCT Series	Standard type		4.5	4.4	—	4.4	—		Vin = V_{IH} or V_{IL} I_{OH} = –20 µA
				4.5	4.18	—	4.13	—		I_{OH} = –4.0 mA
		Bus driver type		4.5	4.4	—	4.4	—		Vin = V_{IH} or V_{IL} I_{OH} = –20 µA
				4.5	4.18	—	4.13	—		I_{OH} = –6.0 mA
	HC Series	Standard type	V_{OL}	2.0	—	0.1	—	0.1	V	Vin = V_{IH} or V_{IL} I_{OL} = 20 µA
				4.5	—	0.1	—	0.1		
				6.0	—	0.1	—	0.1		
				4.5	—	0.26	—	0.33	V	Vin = V_{IH} or V_{IL} I_{OL} = 4.0 mA
				6.0	—	0.26	—	0.33		I_{OL} = 5.2 mA
		Bus driver type		2.0	—	0.1	—	0.1		Vin = V_{IH} or V_{IL} I_{OL} = 20 µA
				4.5	—	0.1	—	0.1		
				6.0	—	0.1	—	0.1		

Parameters			Symbol	V_{CC}(V)	Limits +25˚C min	+25˚C max	–40 to +85˚C min	–40 to +85˚C max	Unit	Test Conditions	
Output voltage	HC Series	Bus driver type	V_{OL}	4.5	—	0.26	—	0.33	V	Vin = V_{IH} or V_{IL}	I_{OL} = 6.0 mA
				6.0	—	0.26	—	0.33			I_{OL} = 7.8 mA
	HCT Series	Standard type		4.5	—	0.1	—	0.1		Vin = V_{IH} or V_{IL}	I_{OL} = 20 µA
				4.5	—	0.26	—	0.33			I_{OL} = 4.0 mA
		Bus driver type		4.5	—	0.1	—	0.1		Vin = V_{IH} or V_{IL}	I_{OL} = 20 µA
				4.5	—	0.26	—	0.33			I_{OL} = 6.0 mA
Input leakage current		HC Series	I_I	6.0	—	±0.1	—	±1.0	µA	Vin = V_{CC} or GND	
		HCT Series		5.5	—	±0.1	—	±1.0			
Analog Switch Off-state Current		HC Series	I_S(off)	6.0	—	±0.1	—	±1.0	µA	Vin = V_{IH} or V_{IL}	
		HCT Series		5.5	—	±0.1	—	±1.0		$\|V_S\|$ = V_{CC} or V_{CC} – V_{EE}	
3-state output Off-state Current		HC Series	I_{OZ}	6.0	—	±0.5	—	±5.0	µA	Vin = V_{IH} or V_{IL}	
		HCT Series		5.5	—	±0.5	—	±5.0		Vout = V_{CC} or GND	
Quiescent Supply Current	HC Series	SSI	I_{CC}	6.0	—	1.0	—	10	µA	Vin = V_{CC} or GND	
		FF		6.0	—	2.0	—	20		Iout = 0 µA	
		MSI		6.0	—	4.0	—	40			
	HCT Series	SSI		5.5	—	1.0	—	10			
		FF		5.5	—	2.0	—	20			
		MSI		5.5	—	4.0	—	40			

Symbols and Terms Defined for HD74HC Series

1. Explanation of Symbols Used in Electrical Characteristics and Recommended Operating Conditions

1.1 DC characteristics

Symbol	Term	Description
V_{IH}	"H" level input voltage	"H" level input voltage to ensure that a logic element operates under some constraint.
V_{IL}	"L" level input voltage	"L" level input voltage to ensure that a logic element operates under some constraint.
V_{OL}	"L" level output voltage	Output voltage in effect when, under the input condition for bringing the output Low, the rated output current is allowed to flow to the output terminal.
V_{OH}	"H" level output voltage	Output voltage in effect when, under the input condition for bringing the output High, the rated output current is allowed to flow to the output terminal.
V_T^+	Forward input threshold voltage	Input voltage in effect when the operation of a logic element varies as the input is allowed to go up from a voltage level lower than the forward input threshold voltage V_T^-.
V_T^-	Reverse input threshold voltage	Input voltage in effect when the operation of a logic element varies as the input is allowed to go up from a voltage level lower than the reverse input threshold voltage V_T^+.
V_H	Hysteresis voltage	Differnce between forward input threshold voltage V_T^+ and reverse threshold voltage V_T^-.
I_{OH}	"H" level output current	Output current that flows out when, under the condition for bringing the output High, the rated output voltage VOUT is applied to the output terminal.
I_{OL}	"L" level output current	Output current that flows out when, under the condition for bringing the output High, the rated output voltage V_{OUT} is applied to the output terminal.
I_{IN}	Input leakage current	Input current that flows in when the rated maximum input voltage is applied to the input terminal.
I_{IH}	"H" level input current	Input current that flows in when the rated "H" level voltage is applied to the input.
I_{IL}	"L" level input current	Input current that flows out when the rated "L" level voltage is applied to the input.
I_{OZ}	Off-state output current (high impedance)	Current that flows to the 3-state output of an element under the input condition for briging the output to High impedance.
Is(off)	Analog switch off-state current	Current that flows to the analog switch of an element under the input condition for bringing the switch to off-state.
I_{CC}	Quiescent supply current	Current that flows to the supply terminal (V_{CC}) under the rated input condition.

1.2 AC characteristics

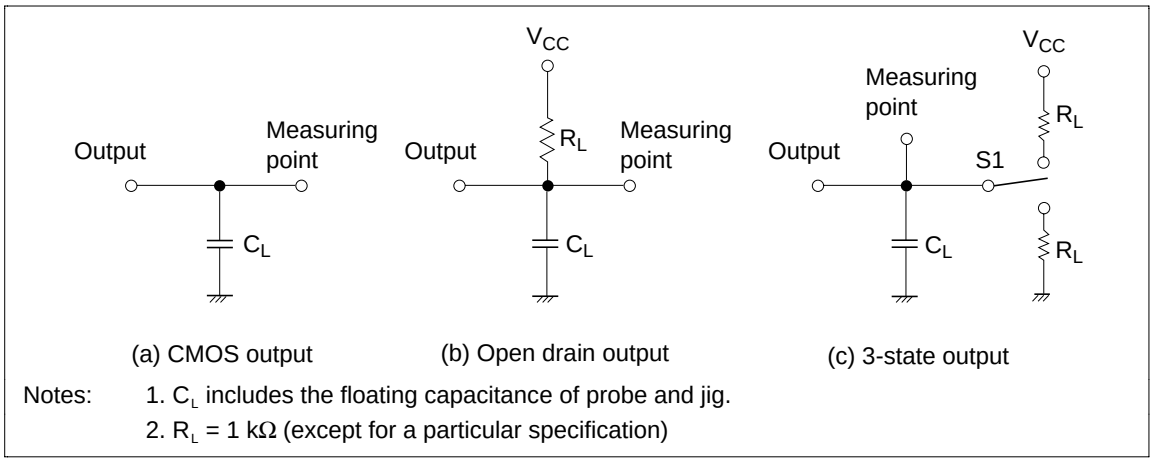
Symbol	Term	Description
f_{max}	Maximum clock frequency	Maximum clock frequency that maintains the stable changes in output logic level in the rated sequence under the I/O condition allowing clock pulses to change the output state.
t_{TLH}	Rise (transient) time	Rated time from “L” level to “H” level of a waveform during the defined transient period changing from “L” level to “H” level.
t_{THL}	Fall (transient) time	Rated time from “H” level to “L” level of a waveform during the defined transient period changing from “H” level to “L” level.
t_{PLH}	Output rise propagation delay time	Delay time between the rated voltage levels of an I/O voltage waveform under a defined load condition, with the output changing from “L” level to “H” level.
t_{PHL}	Output fall propagation delay time	Delay time between the rated voltage levels of an I/O voltage waveform under a defined load condition, with the output changing from “H” level to “L” level.
t_{HZ}	3-state output disable time (“H” level)	Delay time between the rated voltage levels of an I/O voltage waveform under a defined load condition, with the 3-state output changing from “H” level to the high impedance state.
t_{LZ}	3-state output disable time (“L” level)	Delay time between the rated voltatge levels of an I/O voltage waveform under a defined load condition, with the 3-state output changing from “L” level to the high impedance state
t_{ZH}	3-state output enable time (“H” level)	Delay time between the rated voltage levels of an I/O voltage waveform under a defined load condition, with the 3-state output changing from the high impedance state to “H” level.
t_{ZL}	3-state output enable time (“L” level)	Delay time between the rated voltage levels of an I/O voltage waveform under a defined load condition, with the 3-state output changing from the high impedance state to “L” level.
t_w	Pulse width	Duration of time between the rated levels from a leading edge to a trailing edge of a pulse waveform.
t_h	Hold time	Time in which to hold date at the specified input terminal after a change at another related input terminal (e.g., clock input).
t_{su}	Setup time	Time in which to set up and keep data at the specified input terminal before a change at another related input terminal (e.g., clock input).
t_{rm}	Removal time	Time period between the time when data at the specified input terminal is released and the time when another related input terminal (e.g., clock input) can be changed.
C_{in}	Input capacitance	Capacitance between GND terminal and an input terminal to which 0 V is applied.

2. Explanation of Symbols Used in Function Table

Symbol	Description
H	High level (in steady state; noted "H" or “H” level in sentences)
L	Low level (in steady state; noted "L" or “L” level in sentences)
⎍	Transition from L level to H level
⎎	Transition from H level to L level
X	Either H or L
Z	3-state output off (high impedance)
a·····h	Input level of steady state for each of inputs A-H
Q_0	Q level immediately before the indicated input condition is established
$\overline{Q}_0$	Complement of Q
Q_n	Q level immediately before the latest active change (⎍ or ⎎) occurs
⎍⎎	Single H level pulse
⎎⎍	Single L level pulse
TOGGLE	Each output is changed to the complement of the preceding state by an active input change (⎍ or ⎎)

Measuring Method of AC Characteristics

Loading Circuit



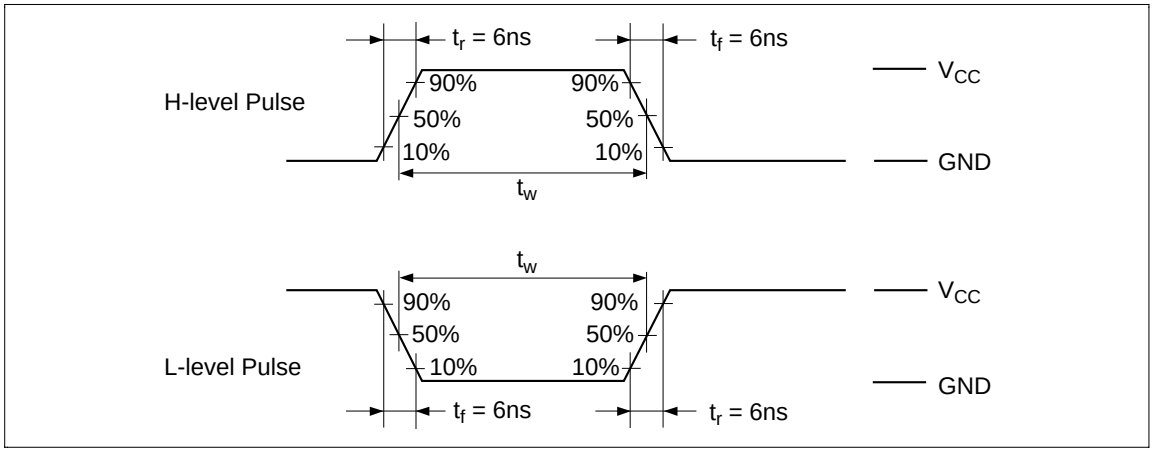
(a) CMOS output (b) Open drain output (c) 3-state output

Notes: 1. C_L includes the floating capacitance of probe and jig.
2. R_L = 1 kΩ (except for a particular specification)

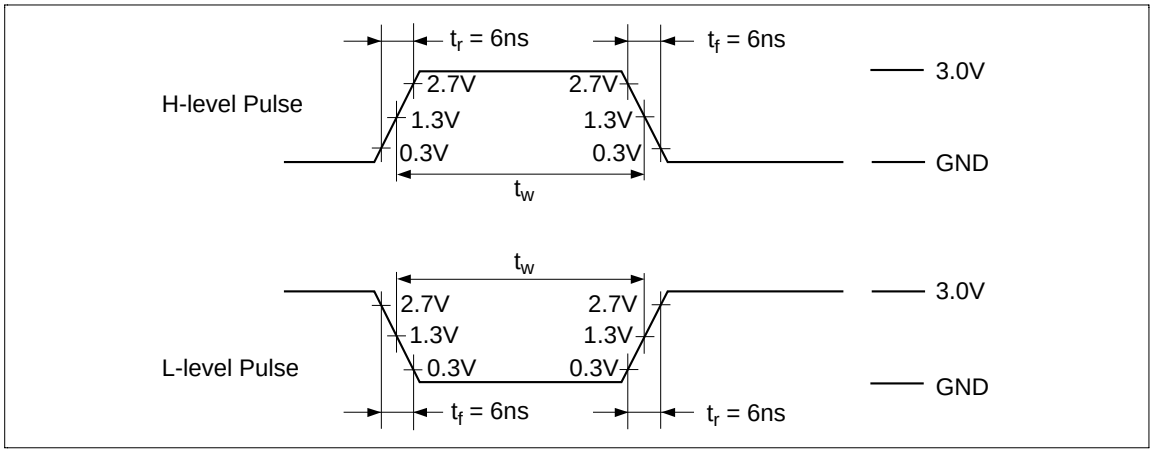
Waveforms (Mutual relationship of waveforms)

Pulse Width (T_W)

74HC Series

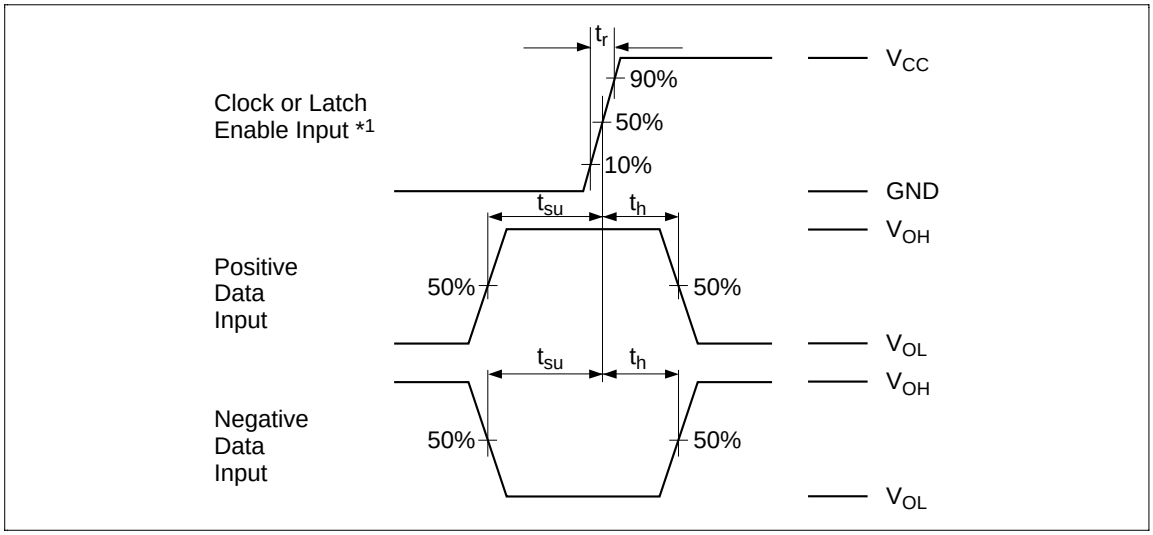


74HCT Series

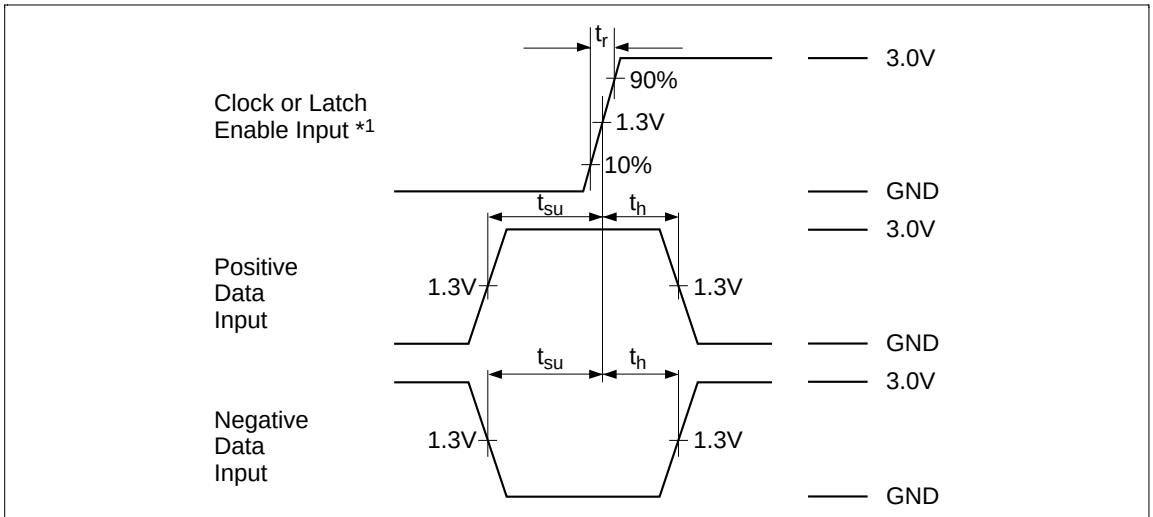


Setup Time and Hold Time

74HC Series



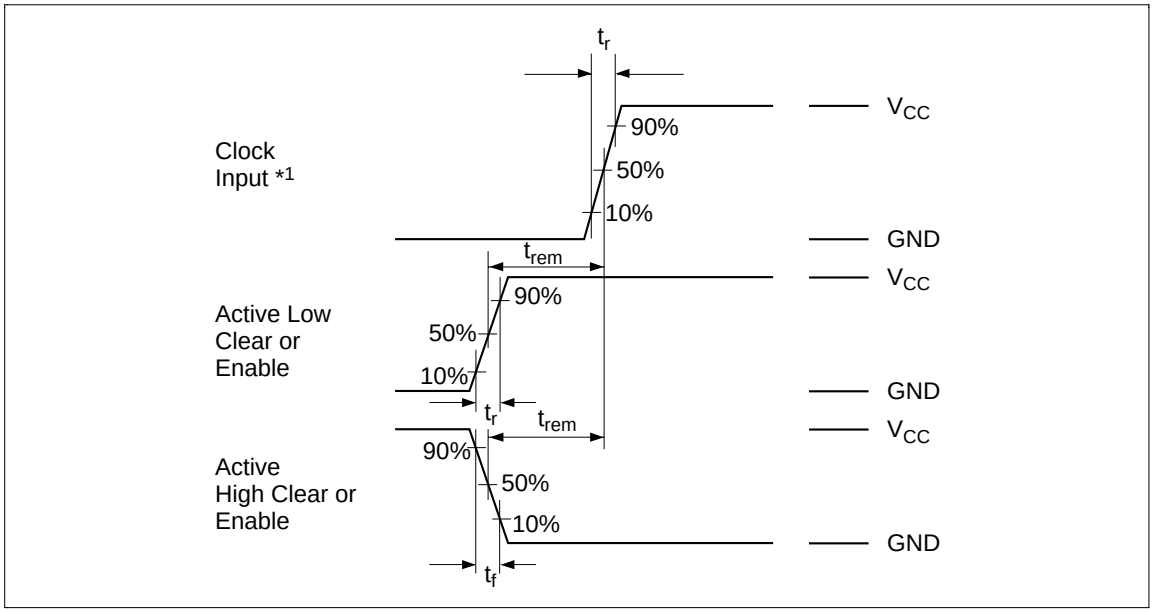
74HCT Series



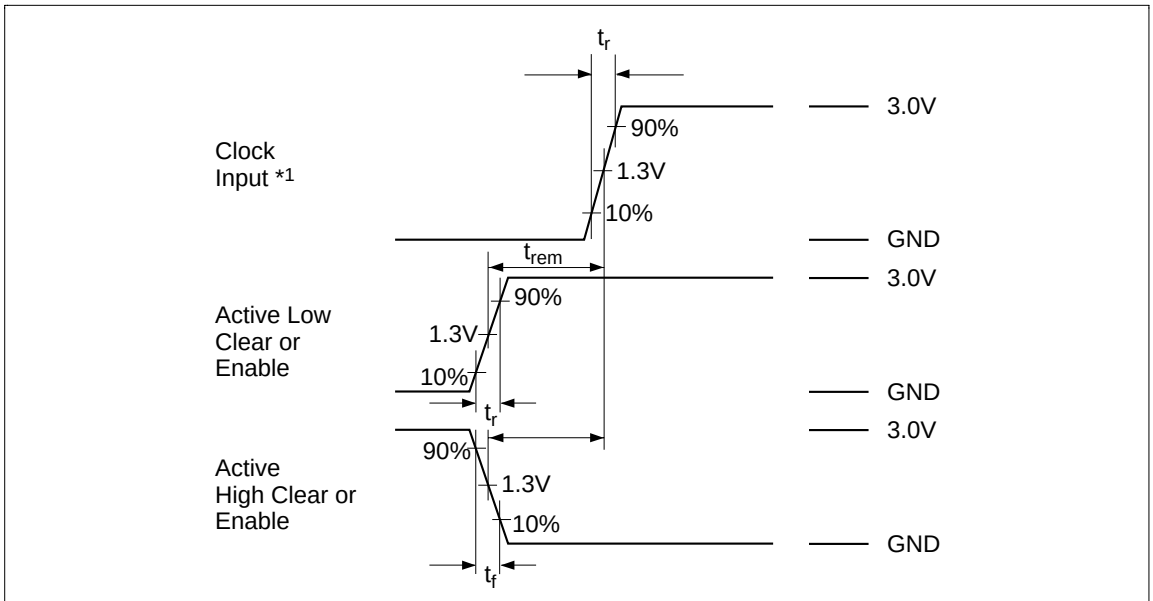
Note: Waveform for negative edge sensitive circuits will be inverted.

Removal Time

74HC Series



74HCT Series

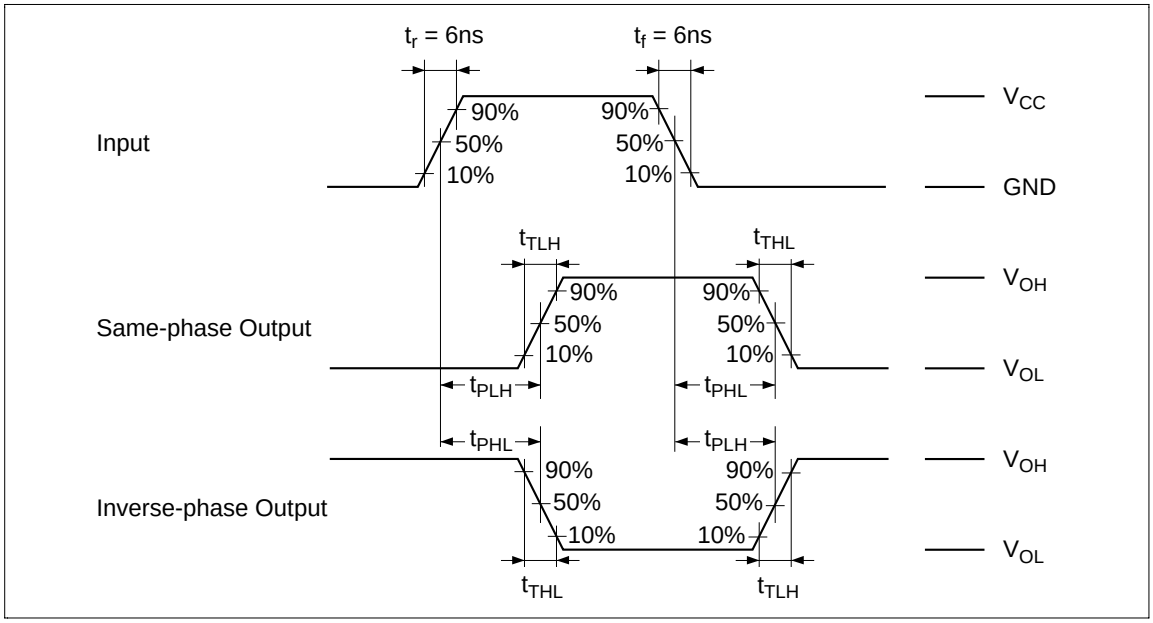


Note: Waveform for negative edge sensitive circuits will be inverted.

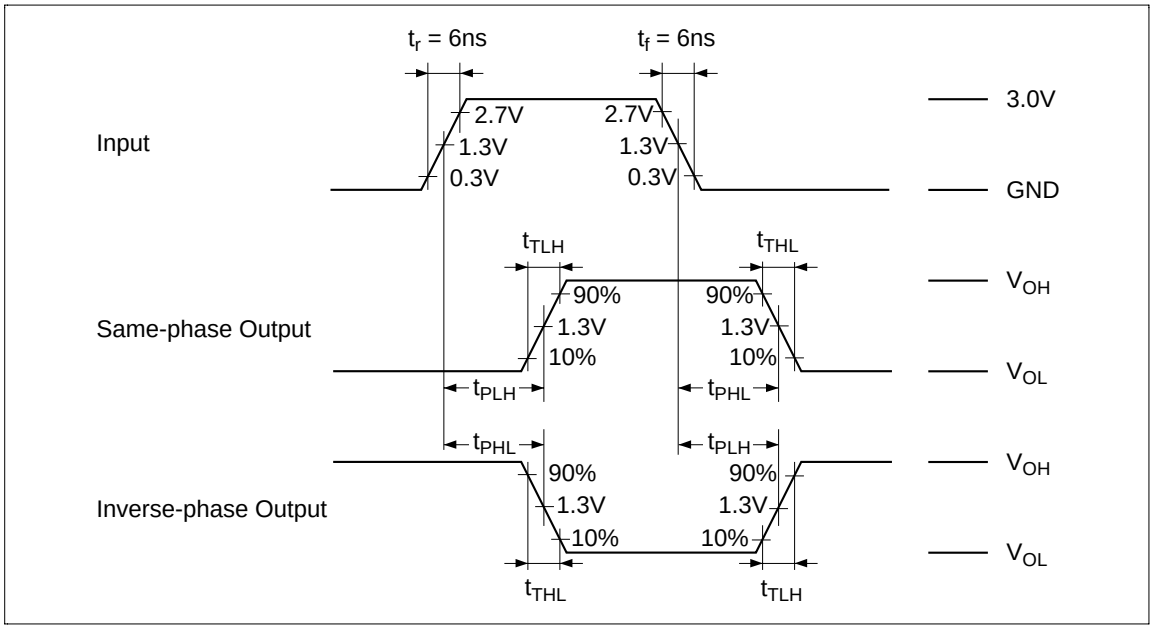
Waveforms (Mutual relationship of waveforms)

Propagation Delay Time, Output Rise Time and Output Fall time

74HC Series



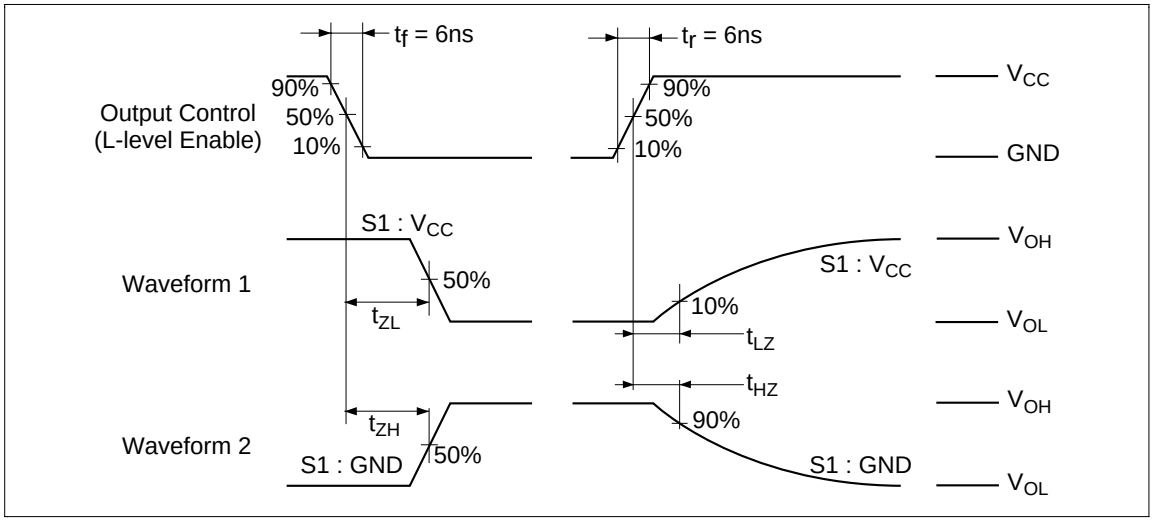
74 HCT Series



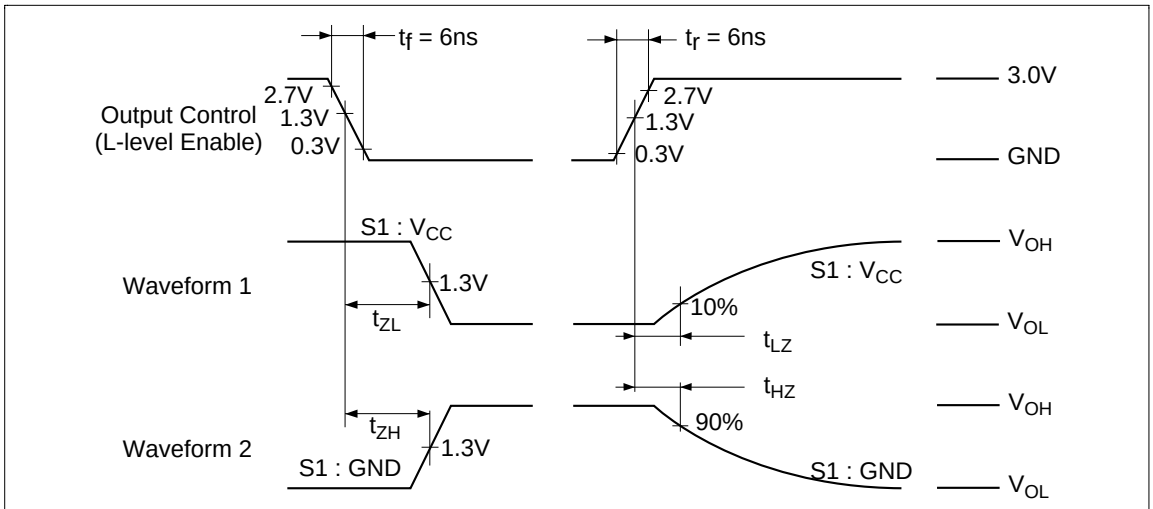
Waveforms (Mutual relationship of waveforms)

Three-state Output, Enable Time and Disable Time

74HC Series



74HCT Series



Notes: 1. Waveform 1 is an output under the internal condition like “L” except for the output disabled by the output control.

2. Waveform 2 is an output under the internal condition like “H” except for the output disabled by the output control.

Precautions in System Design

In the system design, the problems to be considered are described in the following items:

1. Transfer Characteristics

Since the transfer characteristics of gate circuit varies with the number of working inputs, care must be taken to the noise margin. In the multiple input NOR gate, the P channel MOS is connected to V_{CC} in series and the N channel MOS is connected to GND in parallel. In the NAND gate, the connection is reverse. The output voltage V_{OUT} in the transition area becomes a value obtained by distributing the supply voltage at a split ratio according to the ON resistance of P channel MOS and N channel MOS. In the multiple input NOR and NAND gates, the fall of transfer characteristic, that is, V_{IN}(voltage noise margin) that enters in the transition area changes according to the number of inputs as shown in Figure 1.

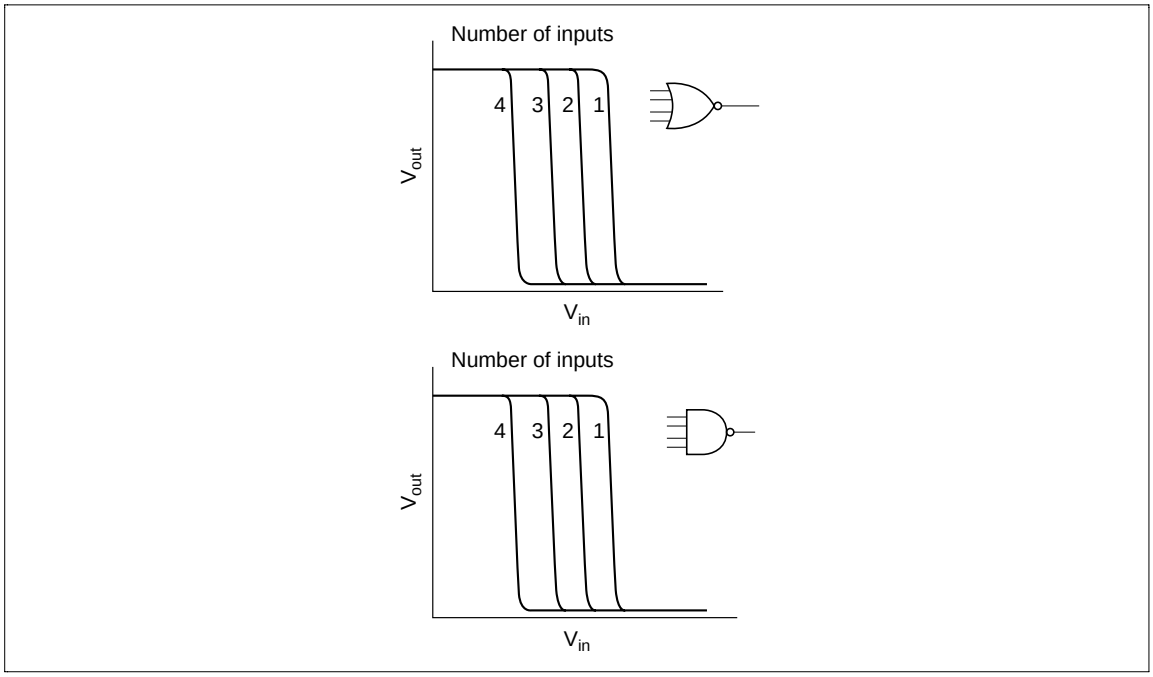


Figure 1

As seen from the above, it becomes clear that:

- In the NOR gate, “0” level noise margin V_{NL} decreases, and “1” level noise margin V_{NH} increases according to the number of working inputs.
- In the NAND gate, the noise margins are fully reversed.

2. Output Impedance

The output impedance of CMOS logic gate is influenced by the circuit configuration, the number of working inputs, logical state and supply voltage. There are two regions of output impedance depending on the operation:

- Constant impedance area in which P and N channel MOS' operate in the nonsaturated state.
- Constant current area in which P and N channel MOS' operate in the pinch-off state.

In designing a system including an interface circuit, the above must be considered.

3. Output Short-Circuit

Because no protective circuitry is provided to limit the output current, an output inadvertently shorted to V_{CC} or GND on the HS-CMOS logic IC is limited to the current value determined by the pinch-off effect of the P-channel MOS and N-channel MOS for the output. Notice that such output short-circuit current, if allowed to flow for a long time, could result in increased power dissipation or in a melted wire due to excessive current density through metalization or other performance failures. For operating stability and reliability, the maximum output current should remain within the maximum rating.

4. Unused Inputs

As shown in Figure 2, unused inputs must be:

(1) Directly connected to V_{CC} for NAND gate circuits.
(2) Directly connected to GND for NOR gate circuits.
(3) Connected to V_{CC} or GND through a proper resistor (10 kΩ or 100 kΩ.).

This is required because the extremely high input impedance of CMOS logic makes it subject to noise. This noise causes the output logic level to be unstable. Furthermore, in some cases, if a gate is not used or a flip-flop is not used, both p-channel MOS and n-channel MOS may conduct, causing I_{CC} to flow.

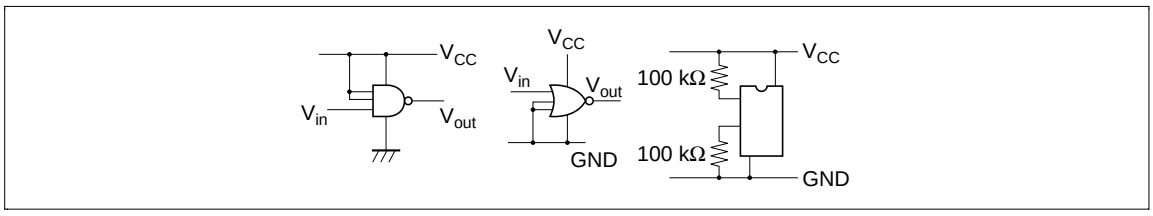


Figure 2 Examples of Handling Unused Inputs

5. Input Impedance

Since all the input protective diodes are biased reversely in the ordinary operations, the input impedance of CMOS logic IC is extremely high. When converted into a leak current, it is about several tens (pA) at a temperature of 25˚C or about one (nA) even at 100˚C. Thus, the matching for operating the CMOS logic IC has only to be considered at a voltage level. In the actual interface to other IC's, however, remember that fan-out is limited according to a capacitance value because inputs measured in capacity.

6. Parallel Connection of Gate Circuits

If it is necessary to increase source or sinking current, the same type gate circuits can be connected in parallel as shown in Figure 3.

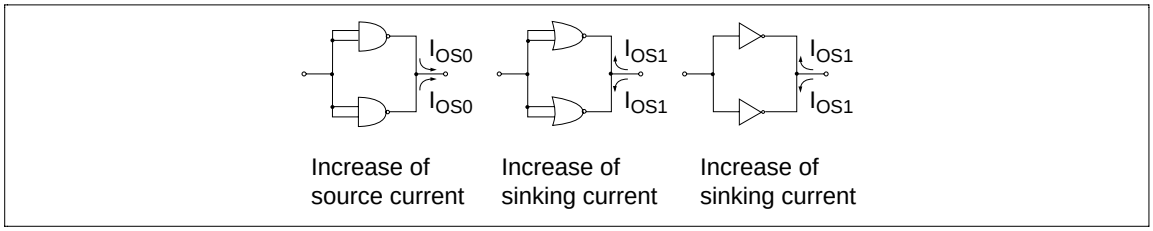


Figure 3 Examples of Parallel Connection

The switching speed improved at the same time. The source and sinking current capacities also increase in proportion to the number of inputs.

7. Wired OR Connection

The wired OR connection is unrecommendable and shall not be used in CMOS logic IC's. The reason is that if the two gate outputs are connected with A = B = 0 and C = D = 1 as shown in Figure 4, the output voltage is a value with which the supply voltage is divided by each of the resistance values of active P and N channel MOS', on an about half level (V_{CC} - GND).

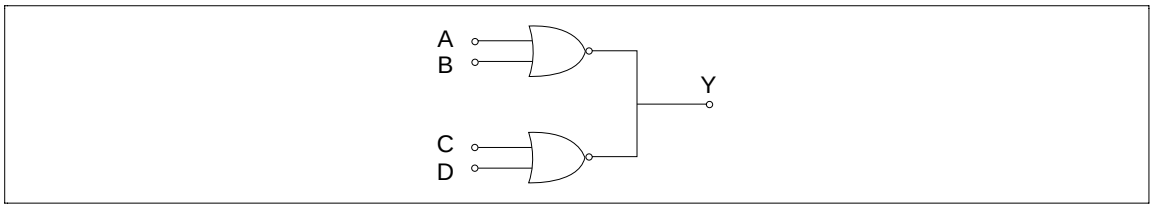


Figure 4 Wired OR Connection

Precautions in System Design

8. Input Capacitance

In the CMOS logic IC, there is capacitance between the input and the GND. In addition to the major capacitance between the gate and the substrate, the capacitance of package, leads and input protection circuit are also included. The change input capacitance depending on the input voltage results mainly from the capacitance between the gate and the substrate. This input capacitance has an advantage of temporarily storing date in it by opening/closing the transmission gate. On the other hand, however, remember that the input capacitance may slow down switching speed of mutually connected gate and also may increase the power dissipation. The input capacitance is usually about 5 (pF) as specified in the standard.

9. Output Capacitance

The whole output capacitance of CMOS logic IC is the sum of the drain capacitance of output MOS and the external load capacitance. It may be considered that the former is about 10 (pF) per output. The propagation delay time increases linealy in proportion to the increase of external load capacitance as described previously. The power dissipation also increases according to it. Especially, be careful in attaching a large capacity of around 1 (1μF) outside.

The peak current at the gate transition, as described previously, is limited by the output characteristics of P and N channel MOS'. In the buffer circuit, the peak current may increase (to 100 mA or more).

Pay sufficient attention to the fact that the rise of temperature in the chip may cause metal migration on the metal wiring layer. If the peak current for gate circuit is set to about 50 mA and the one for buffer circuit is set to about 100 mA, no consideration is required.

10. Features of 3-state Output Circuit

In a system that requires bus configuration, the 3-state output element is brought from the necessity to place unnecessary circuits in the high output impedance state through control input to operate necessary circuit selectively when tow or more circuit is connected to one bus line. Figure 5 shows the typical 3-state circuit. When the Disable input of control terminal is at "1" level, the output is at low impedance by the switch operation. When at "0" level, the output is at extremely high impedance of 10^4 (MΩ) at a room temperature. Remember that the number of 3-state elements connectable to one bus line is limited by the switching speed and supply voltage.

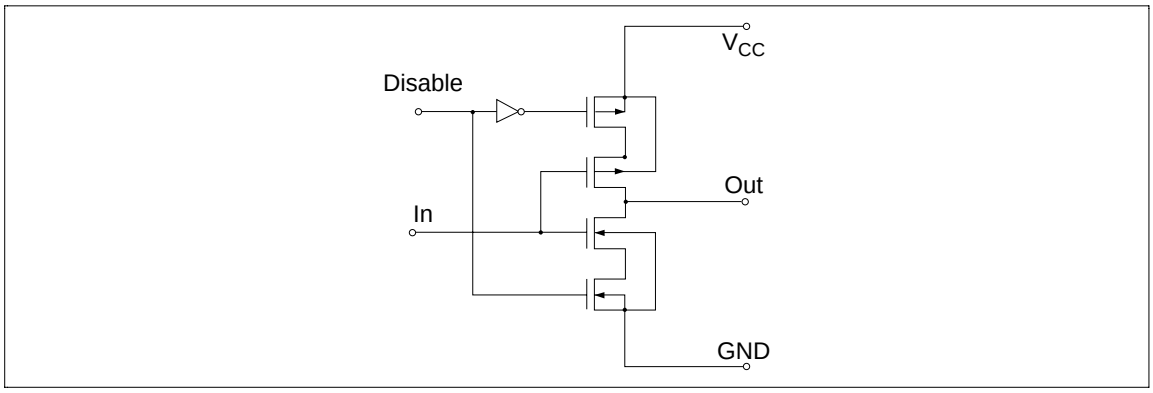


Figure 5 3-state Output Circuit

Precautions in System Design

11. Static Power Dissipation

In the CMOS logic IC, the P channel MOS and N channel MOS are mutually connected each other. Therefore, either P channel or N channel is cut off in the input potential level static state. There is no path in which the current from the power supply flows. Actually, the reverse bias leak current in all the P-N junction in the chip including parasitic P-N junction flows only. The supply current in this state is referred to as static current consumption, and the power dissipation as static power dissipation. The static current consumption is a total of leak currents, and its values are extremely small as listed in Table 1. Thus, the static current consumption is almost proportional to the supply voltage and increases exponentially in proportion to temperature.

Table 1

			Static Current Consumption $I_{CC(max)}$	
Type		**V_{cc}**	**+25˚C**	**–40 to +85˚C**
HC series	SSI	6.0 V	1.0 µA	10 µA
	FF		2.0 µA	20 µA
	MSI		4.0 µA	40 µA
HCT series	SSI	5.5 V	1.0 µA	10 µA
	FF		2.0 µA	20 µA
	MSI		4.0 µA	40 µA

12. Dynamic Power Dissipation

Assuming that the square pulse waves (tr = t_f = 0) as shown in Figure 7 are applied to the input of the inverter shown in Figure 6, the output steps from “0” level to “1” level in response to the input fall from “1” level to “0” level.

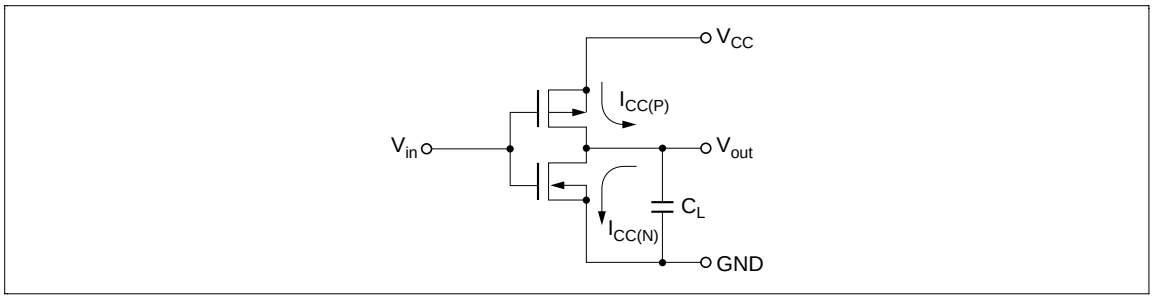


Figure 6 Inveter circuit

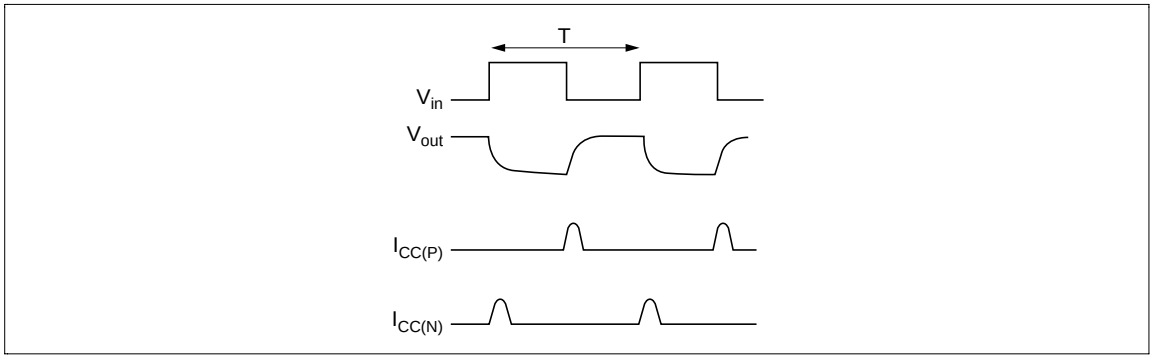


Figure 7 Operating Voltage and current of inverter circuit

Actually, V_{OUT} is not converted into square waveforms. The reason is that the sum total C_L of the outputs such as external load capacitance and drain capacitance are inverted by charging them from 0 to V_{CC}. For charging, supply current $I_{CC(P)}$ flows through the active P channel MOS from V_{CC}. Contrary to this, when the input goes from "0" level to "1" level, C_L discharges and $I_{CC(N)}$ flows into GND through the N channel MOS. The supply current caused by the charge/discharge is dynamic current dissipation, and the power dissipation is dynamic power dissipation. If the average power dissipation is taken as P_T, it is obtained theoritically as follows:

The power dissipation when $I_{CC(P)}$ flows into the P channel MOS in Figure 6 is $I_{CC(P)}$ (V_{CC} - V_{OUT}). If an average is taken by the one cycle of input pulse, the average power dissipation P_{TP} of P channel MOS is:

$$P_{TP} = 1/T \int_0^T I_{CC(P)} \cdot (V_{CC} - V_{OUT})\, dt$$

$$I_{CC}(P) = C_L \cdot d(V_{CC} - V_{OUT})/dt$$

In the same manner, the average power dissipation of N channel MOS is:

$$P_{TN} = 1/T \int_0^T I_{CC(N)} \cdot (V_{OUT} - GND)\, dt$$

$$I_{CC(N)} = C_L \cdot d(V_{OUT} - GND)/dt$$

Thus, the average dynamic power dissipation P_T is:

$$P_T = P_{TP} + P_{TN}$$
$$= 1/T \cdot C_L \cdot V_{CC}^2$$
$$= f \cdot C_L \cdot V_{CC}^2$$

f : Input pulse frequency

It is clear that the dynamic power dissipation varies with the frequency, load capacitance and supply voltage.

Figure 8 shows the aspect.

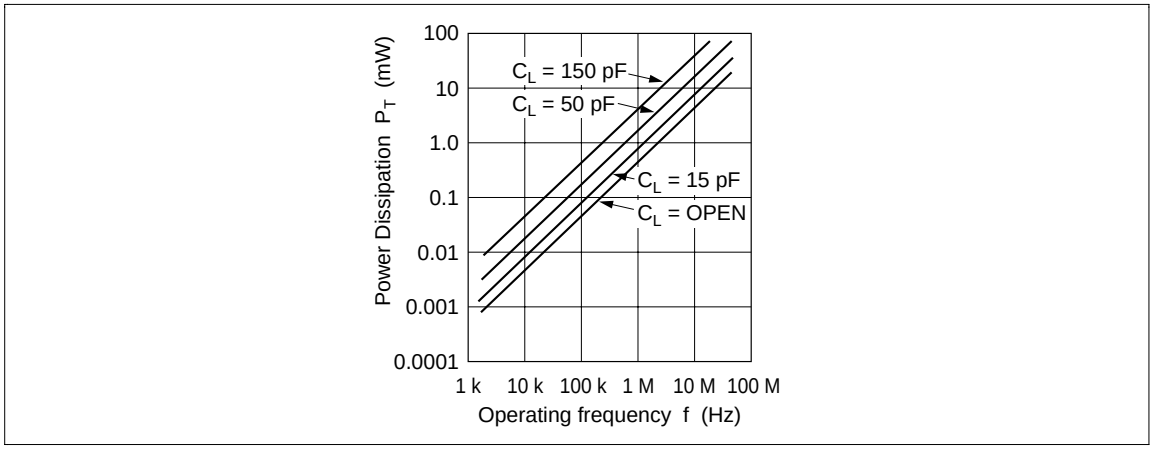


Figure 8 Power Dissipation VS. Operating Frequency

This relation shows a case where the square wave input with tr = tf = 0 is assumed. In an actual case, the input pulse is considered a trapezoidal waveform. Thus, remember that the transition state in which both P channel MOS and N channel MOS are simultaneously activate and DC current flows from V_{CC} into GND during this time. If input is used at an intermediate level, such as crystal oscillator circuit and a linear amplifier, and if the circuits such as a differentiation circuit, an integration circuit and an oscillation circuit process gentle waveforms, pay attention to the increase of power dissipation.

13. Caution of Supply Voltage

To decouple noises, the capacitance of 0.01 to 0.1 (μF) should be attached externally between V_{CC} and GND.

14. Caution of Fan-out

The number of fan-outs of CMOS logic IC is virtually unlimited in terms of DC. The reason is that the input current is the P-N junction leak current of input protection circuit at most and its value is actually approximate to 0 because the input is connected to the gate electrodes and insulated from the substrate.

Therefore, the number of fan-outs is not a problem in terms of DC. In AC, there is a slightly different circumstance. Since the input has a capacity of about 5 (pF), the output capacitance increases if the input is connected to the output. If the input capacitance is taken as 5 (pF), for example, the whole load capacitance C_L (pF) at the time the number of fan-outs is n and load capacitance is C_O (pF) is:

$C_L = 5 \cdot n + C_O$ (pF)

On the other hand, the propagation delay time increases in proportion to the output load capacitance C_L. The operating speed decreases according to the number of inputs (fan-outs) connected to the output. Therefore, remember that the number of fan-outs is fairly limited if a high-speed operation is required.

15. Cautions on Actual Operation

(1) The rise time and fall time of input waveforms should be 500 ns or less. Since the voltage gain is very high near the threshold, the slightest ripples on the input voltage may cause the output to produce a corresponding waveform, making the output operation unstable.

(2) The power line should be sufficiently filtered for the device. The input threshold voltage of the IC varies with the supply voltage. A ripple on the power line may change the input threshold, causing the same malfunction as noted in (1) above.

(3) Beware of a ringing (waveform distortion). Because the switching from “1” level to “0” level on vice versa is very fast, the load capacitance plus the wiring inductance may cause a ringing. Care should be taken to arrange the circuit configuration, PCB layout and wiring appropriately.

1. Input Protection Circuit

An Si-gate process is applied to Hitachi's high-speed CMOS logic ICs.They have a thinner gate oxide compared to conventional Al-gate CMOS logic ICs and are composed into finer patterns.

Therefore, an input protection circuit is necessary for the gate to be protected from surges at the input pins.

Since Al-gate CMOS logic ICs use a diffusion resistor as the input protection resistor (as shown in Figure 1a), input over-current flows directly to the power supply and the destruction of the protection diode may occur.

On the other hand, using polysilicone as its input protection resistor (shown in Figure 1b), high-speed CMOS logic ICs take the role of a current limiter to counter input over voltage.

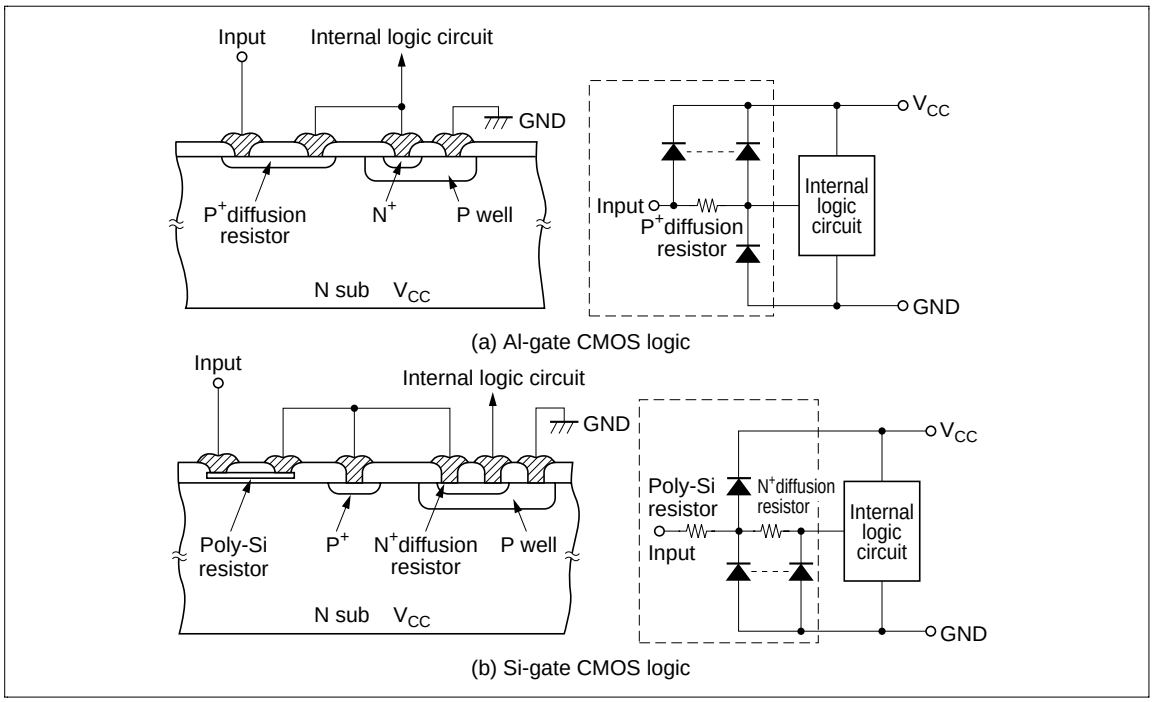


Figure 1 Input Protection Deevice and Equivalent Circuit

2. Electric Static Discharge Immunity (ESD Immunity)

ESD immunity is evaluated by the capacitor discharge method shown in the test circuit of Figure 2. The capacitor is 200 pF, accounting for the electrostatic capacitance of human bodies. Figure 3 shows an example of ESD immunity of integrated circuits for each products series.

The ESD for high-speed CMOS logic is over ±200 V, which is the same level or better than LS-TTL.

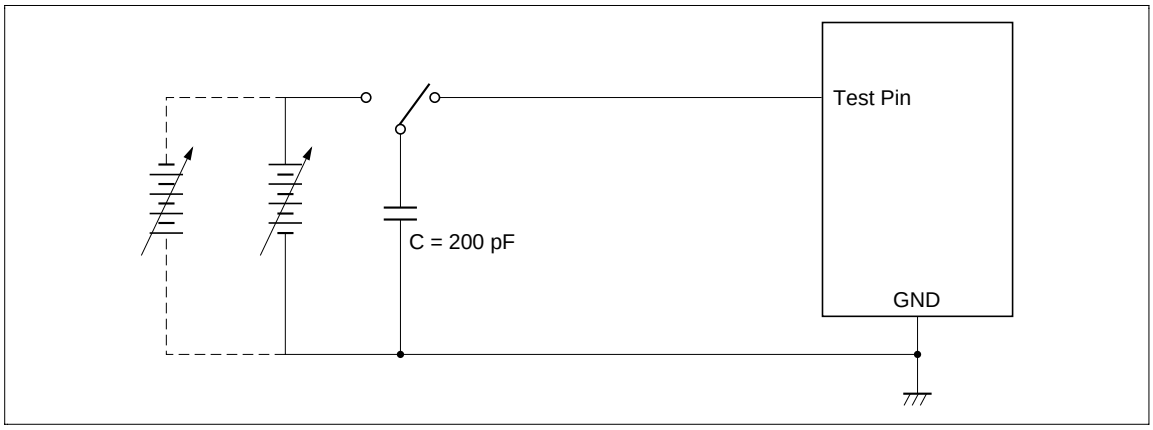


Figure 2 ESD Immunity Test Circuit

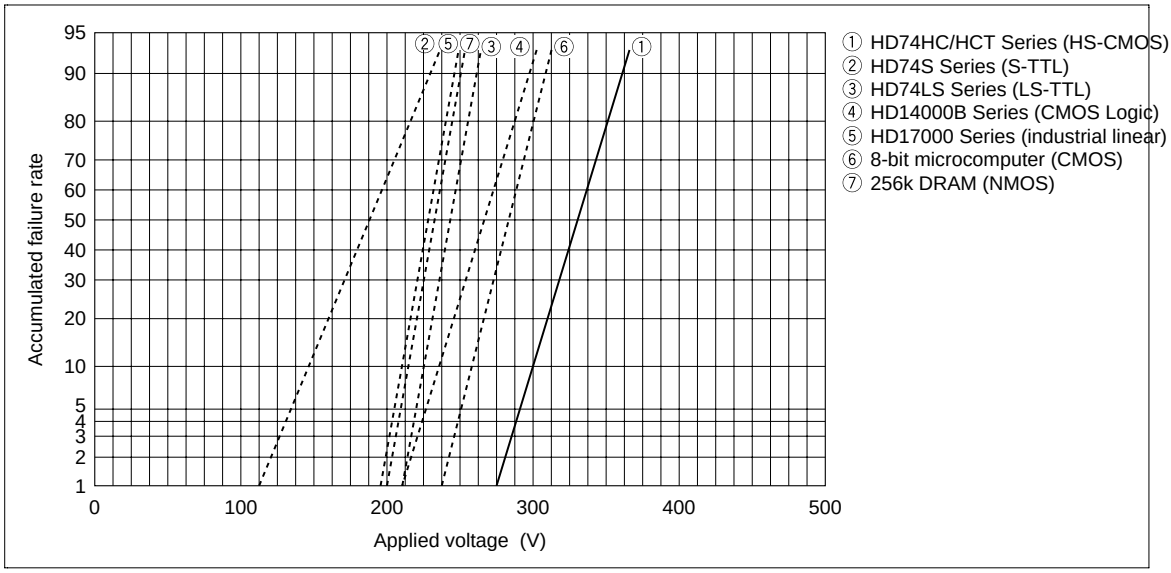


Figure 3 ESD Immunity for Each Series

3. Latch-Up

3.1 Latch-up

Latch-up is an inevitable phenomenon occurring from the basical structure of CMOS logic ICs.

Since CMOS has PMOS and NMOS on one chip, NPN and PNP transistors are made. These two types of transistors are combined into a PNPN structure, in which a parasitic thyristor is formed (see Figure 4).

If excessive noise is applied to the input or output pins when the IC is operating, the parasitic thyristor will turn on and the abnormal current will flow through the power supply pin to ground.

If the power supply is turned off, the IC will be restored to its normal state, however, the internal AI wiring of the IC may melt thus causing the IC to be destroyed.

There are countermeasures to prevent latch-up as listed below

(1) Separate PMOS from NMOS.
(2) Shut down electrical paths between PNP and NPN transistors which form parasitic thyristors by its layout pattern.
(3) Isolate each MOS transistor with an insulator to prevent the formation of parasitic thyristors.

Hitachi's high-speed CMOS logic utilizes method (2)

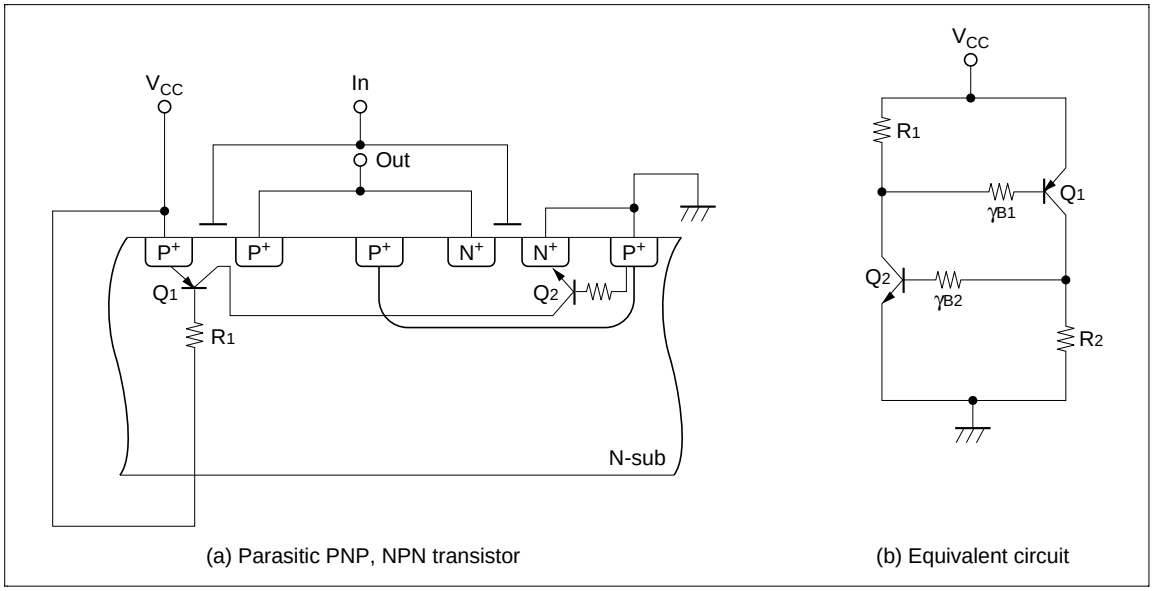


Figure 4 Parasitic Thyristor

3.2 Latch-Up immunity

Latch-up immunity is evaluated by the test circuit shown in Figure 5.

Table 1 lists the test results of latch-up immunity of Hitachi's high-speed CMOS logic.

The starting voltage of high-speed CMOS logic is over ±300 V which causes almost no problems for practical use.

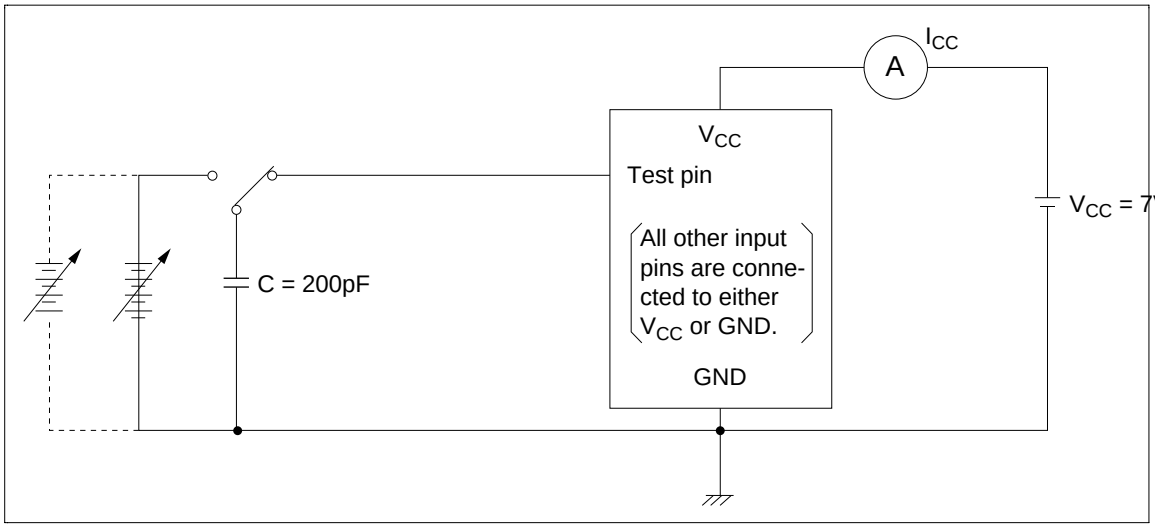


Figure 5 Latch-Up Immunity Test Circuit

Table 1 Latch-Up Starting Voltage Test Results

	Latch-up starting voltage
Positive	Over 300 V
Negative	Over 300 V

Measured samples

HD74HC00

HD74HC02

HD74HC04

HD74HC08

HD74HC14

HD74HC32

HD74HC74

HD74HC138

HD74HC139

HD74HC157

HD74HC158

HD74HC175

HD74HC273

HD74HC373

HD74HC533

5 pieces per type

4. Electrical Characteristics

4.1 DC characteristics

(1) Logic threshold voltage (V_{TH})

The Logic threshold voltage (V_{TH}) of Hitachi's high-speed CMOS logic ICs (HD74HC Series) is at half the level of V_{CC} in order to set up the widest noise margin possible.

(2) Output current characteristics

Hitachi's high-speed CMOS logic ICs have symmetrical characteristics between I_{OH} and I_{OL}. Thus, the balance between t_{PLH} and t_{PHL} is mostly kept even when connecting with a comparatively large load capacitance.

Figures 7 and 8 show the output current characteristics.

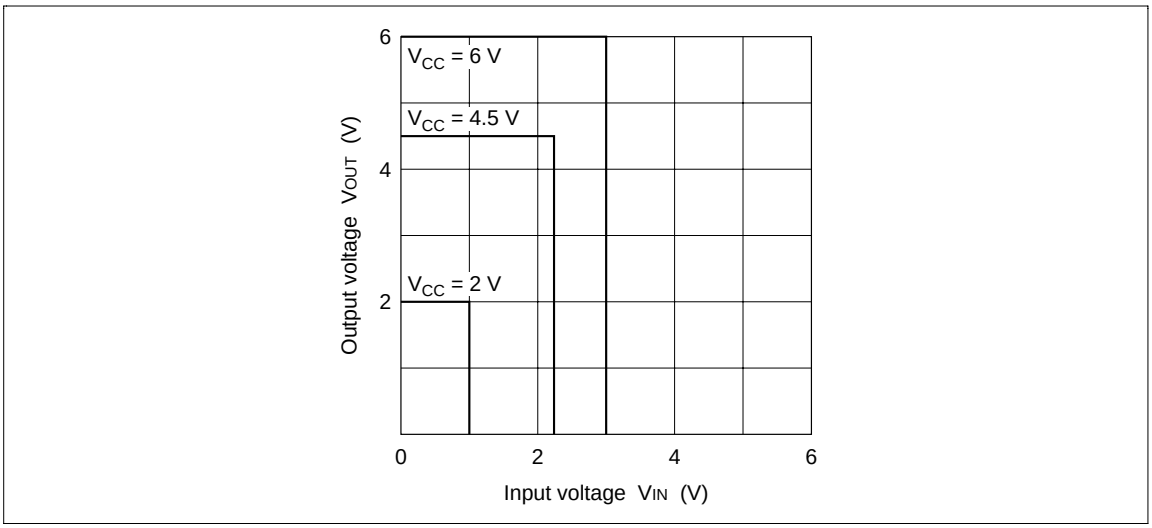


Figure 6 Output Voltage vs Input Voltage

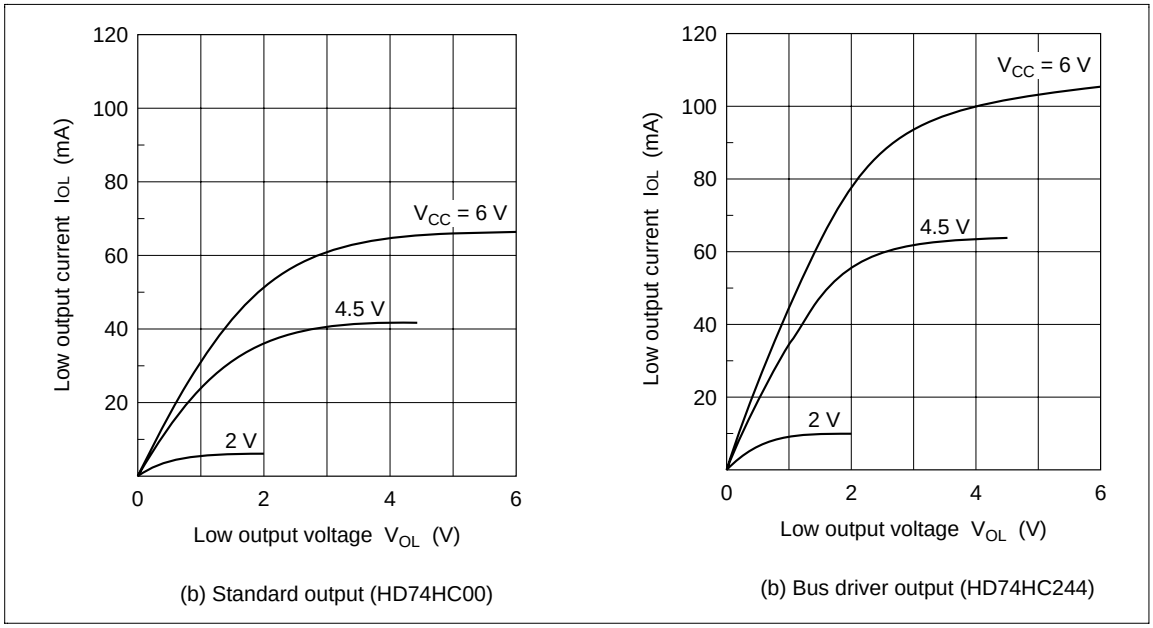


Figure 7 Output Current vs Voltage (Low Level)

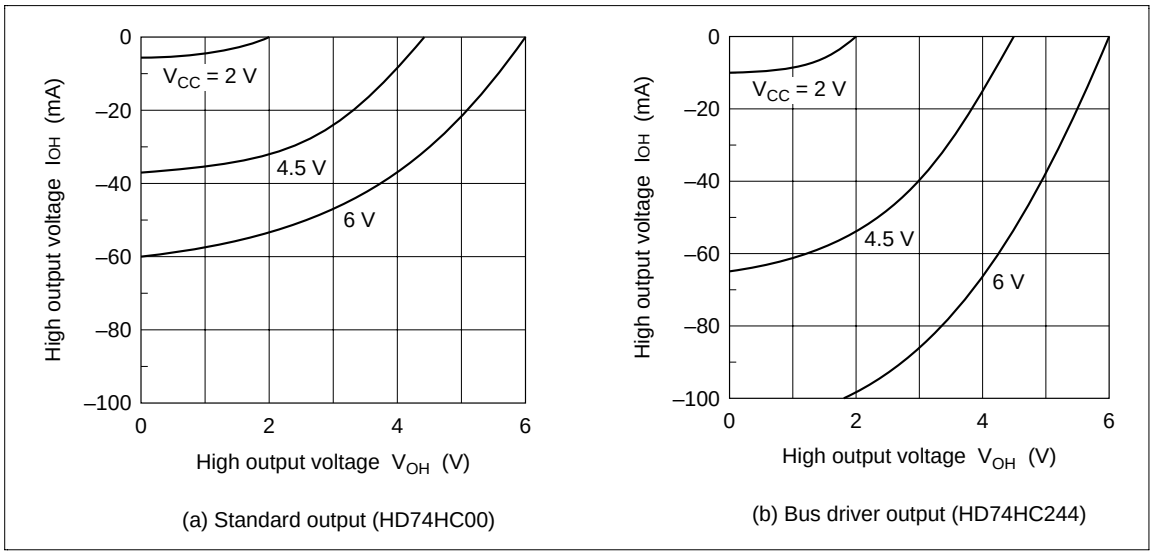


Figure 8 Output Current vs Voltage (High Level)

4.2 AC characteristics

t_{PLH} and t_{PHL} of Hitachi's high-speed CMOS logic ICs are set up to be about the same to simplify system timing design.

(1) Propagation delay time, output rise and fall time vs supply voltage characteristics.

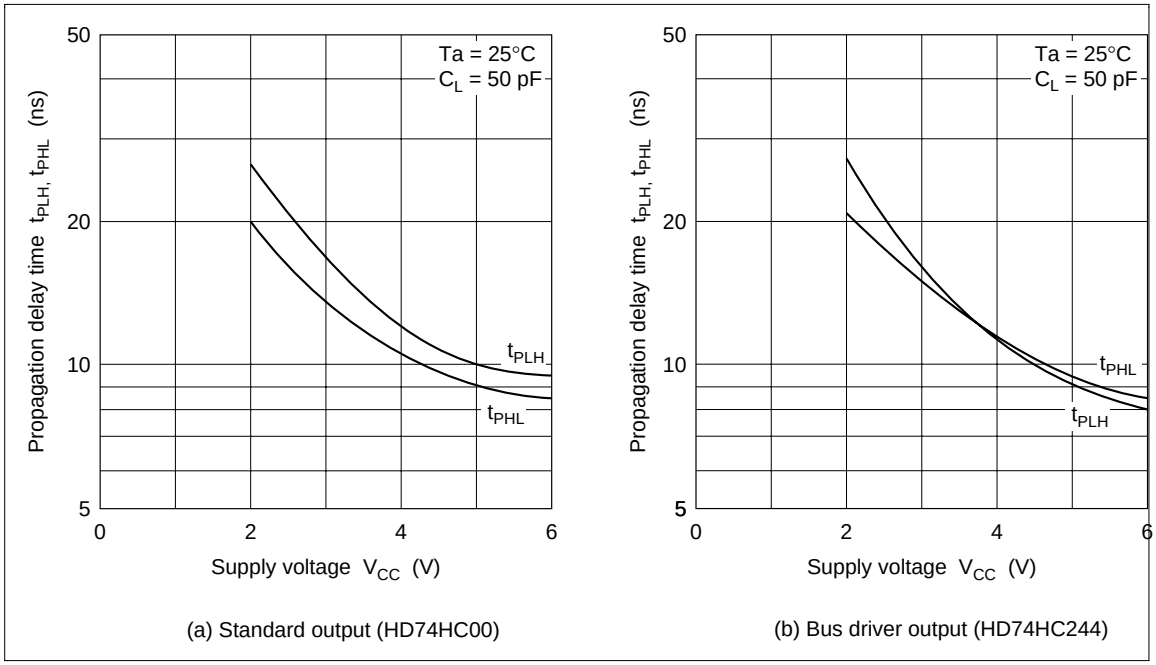


Figure 9 Propagation Delay Time vs Supply Voltage

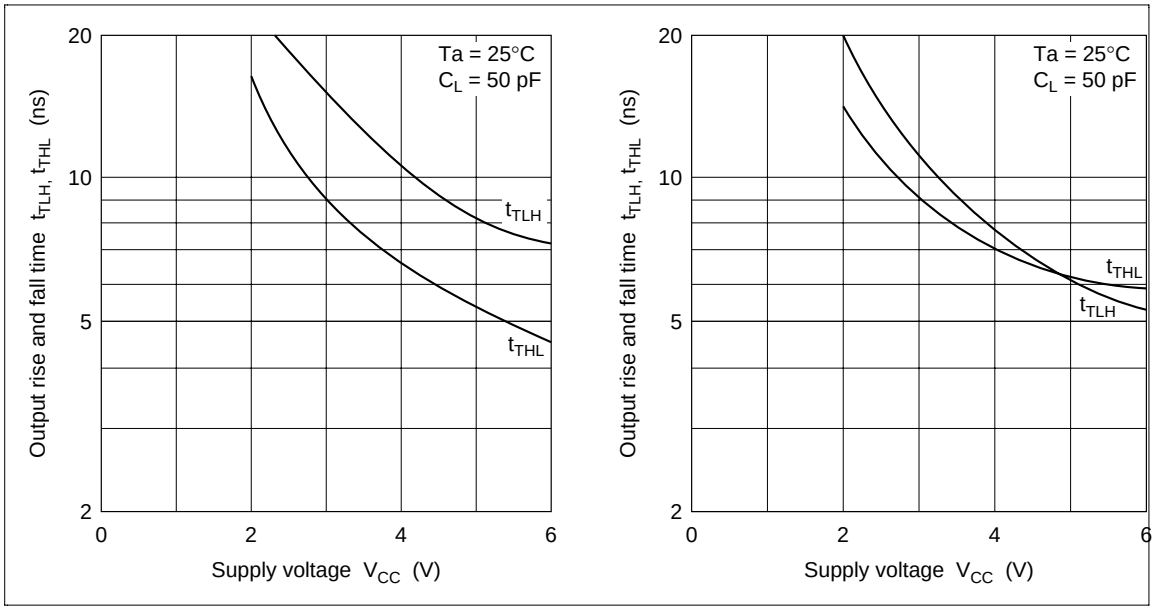


Figure 10 Output Rise and Fall Time vs Supply Voltage

(2) Propagation delay time, output rise and fall time vs load capacitance characteristics.

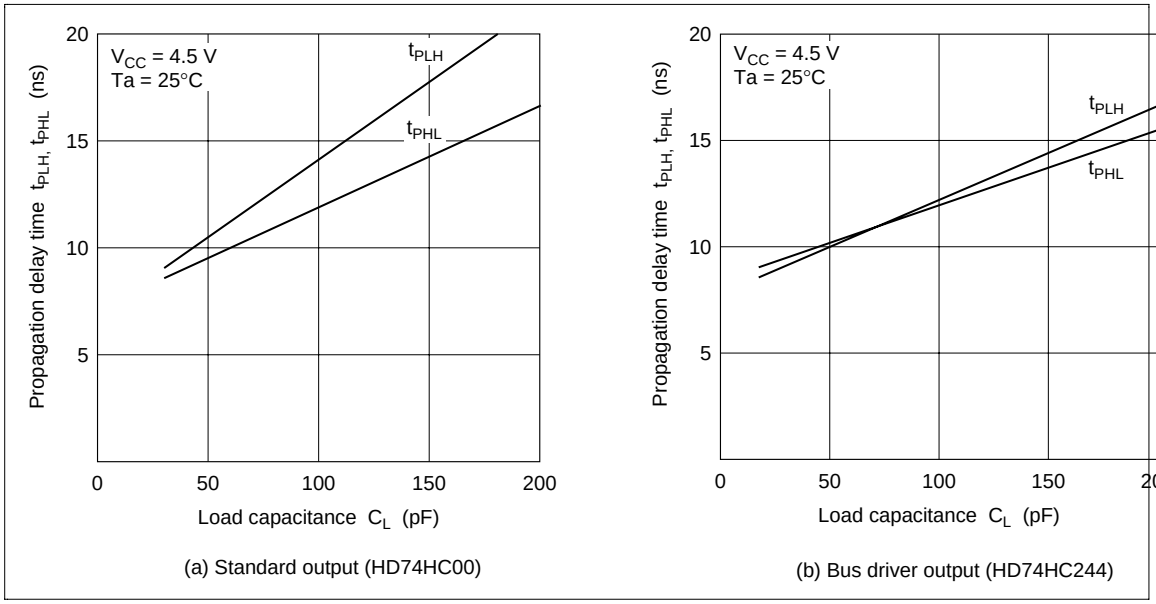


Figure 11 Propagation Delay Time vs Load Capacitance

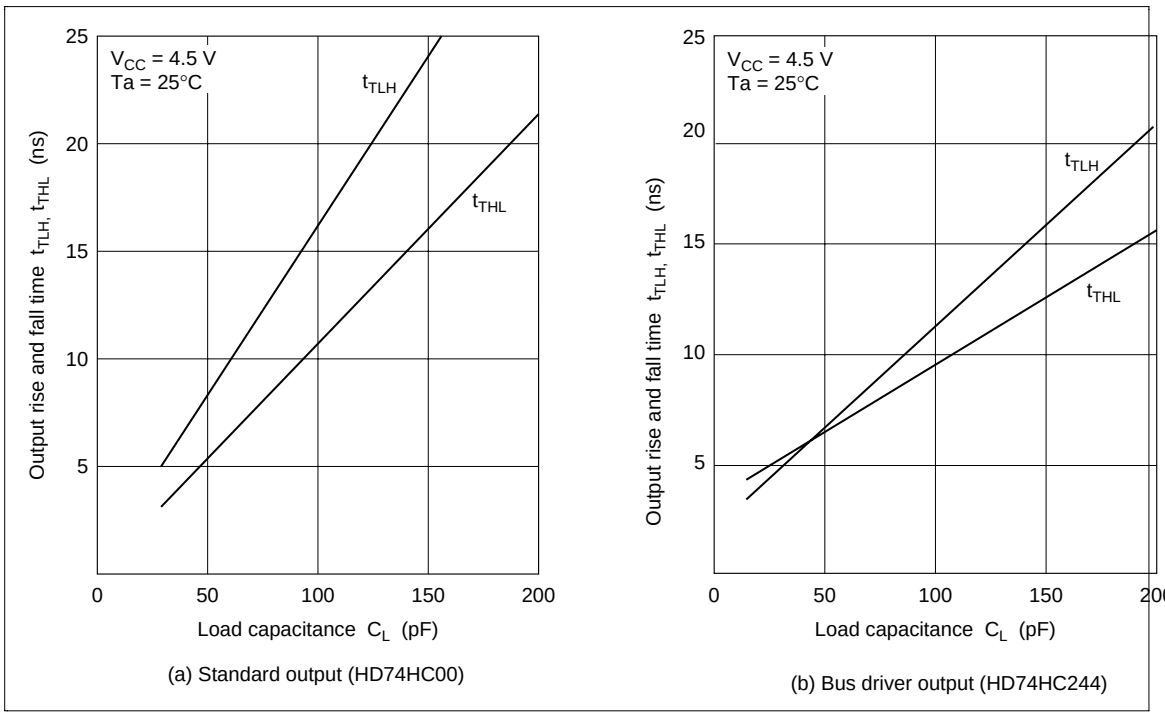


Figure 12 Output Rise and Fall Time vs Load Capacitance

5. Power Dissipation

5.1 Calculating the power dissipation

The power dissipation P_T of high-speed CMOS logic can be calculated by (1). From this equation, the power dissipation depends on the load capacitance, frequency and supply voltage.

$$P_T = (C_L + C_{PD}) \cdot f \cdot V_{CC}^2 \qquad (1)$$

Figure 13 shows examples of the operating frequency with the power supply current.

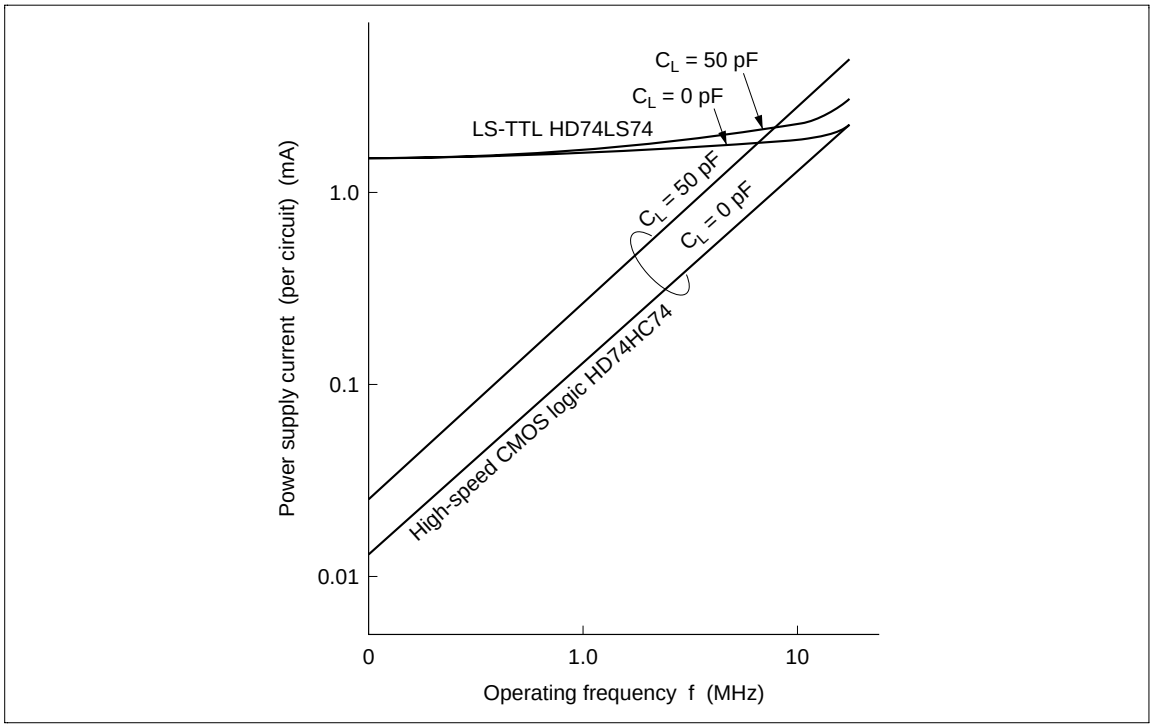


Figure 13 Operating Frequency vs Power Supply Current

5.2 Power dissipation capacitance

Power dissipation capacitance (C_{pd}) can be calculated by the following equations,

$$P_{T1} = C_{PD} \cdot V_{CC}^2 \cdot f_1 = I_{CC1} \cdot V_{CC} \qquad (2)$$

$$P_{T2} = C_{PD} \cdot V_{CC}^2 \cdot f_2 = I_{CC2} \cdot V_{CC} \qquad (3)$$

therefore,

$$C_{PD} = \frac{P_{T2} - P_{T1}}{V_{CC}^2 \cdot (f_2 - f_1)} = \frac{I_{CC}^2 - I_{CC}^1}{V_{CC} \cdot (f_2 - f_1)} \qquad (4)$$

then,

- I_{CC1} : Supply current at frequency f_1
- I_{CC2} : Supply current at frequency f_2

Table 2 lists the power dissipation capacitance of Hitachi's high-speed CMOS logic.

Furthermore, the power dissipation capacitance differs according to the input conditions.

Table 3 shows typical examples.

Table 2 Power Dissipation Capacitance of High-Speed CMOS

Function		Product part no.	Note 1	Power dissipation capacitance typ. (pF)
Gate		HD74HC00	*	27
		HD74HC04	*	24
Flip-Flop	D-type	HD74HC74	*	41
	J-K-type	HD74HC76	*	49
COMPARATOR		HD74HC85	P	48
DECORDER		HD74HC138	P	90
COUNTER		HD74HC161	P	57
BUFFER		HD74HC240	*	42
MULTIPLEXER		HD74HC258	P	78
LATCH		HD74HC373	P	57

Notes: 1. *:Per circuit; P:Per package.
2. Measurement circuit is shown in figure 14.

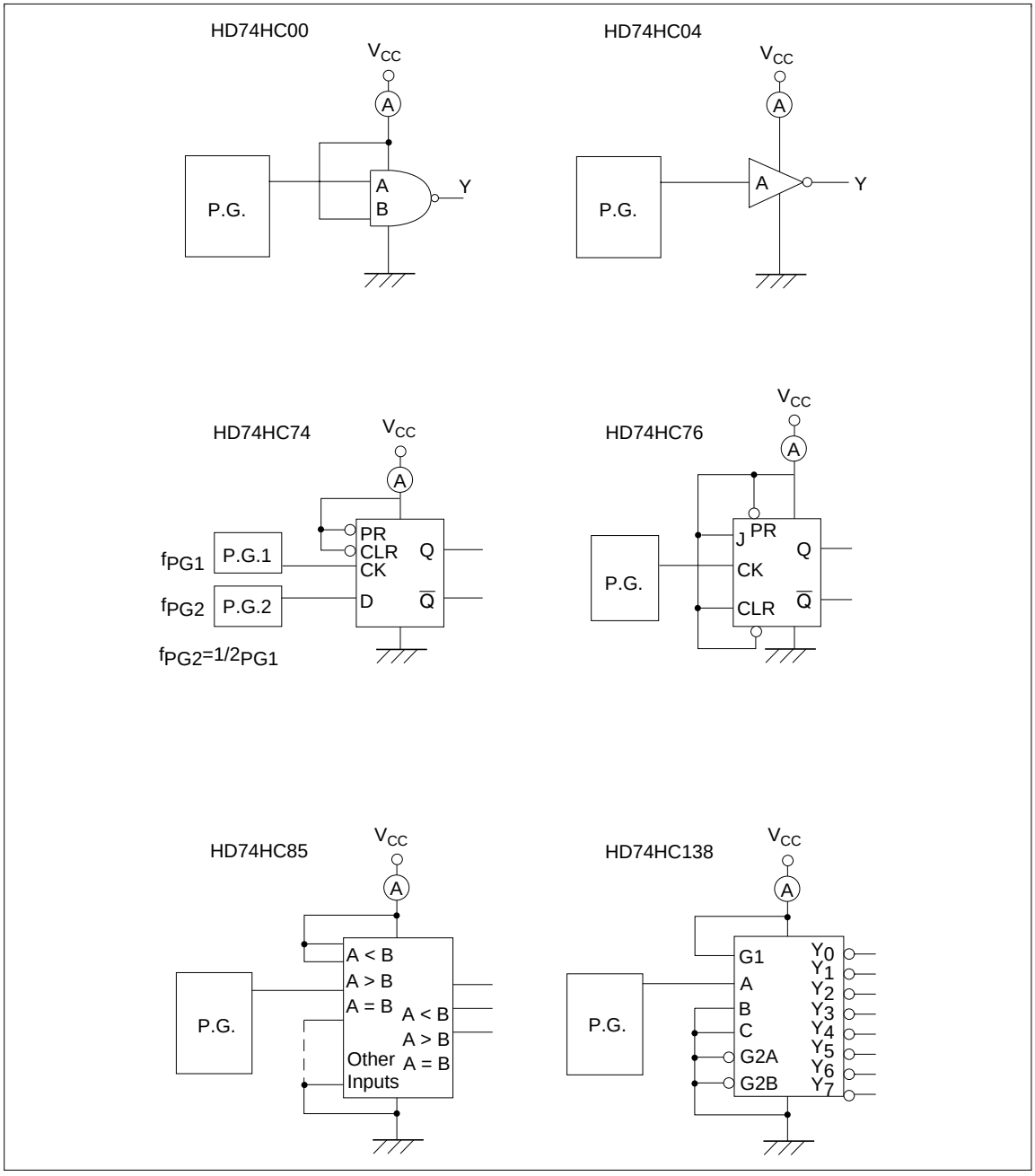


Figure 14 Measurement Circuits for Dynamic Power Supply Current

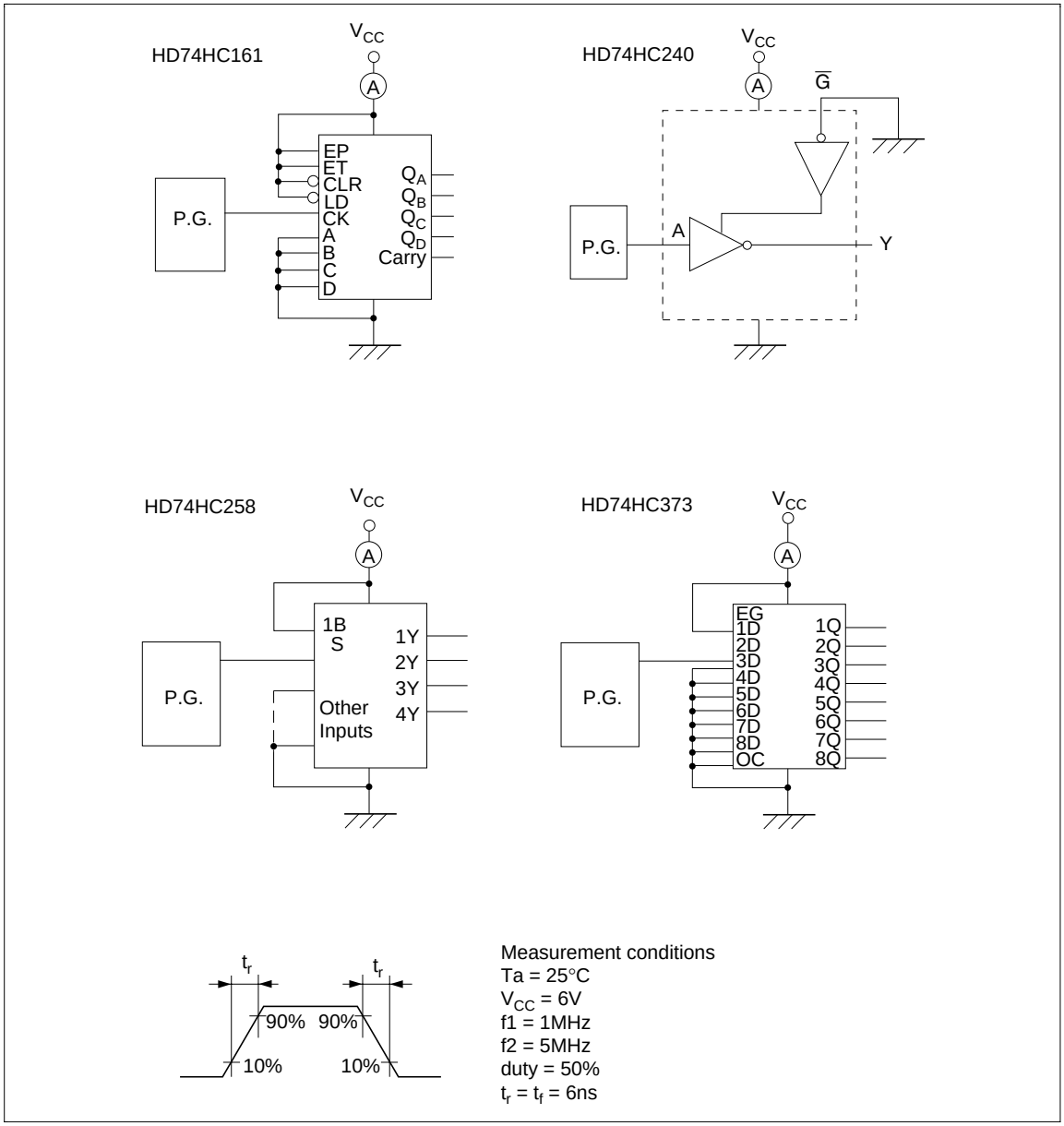
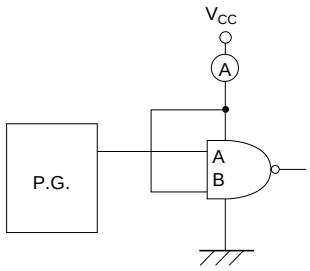
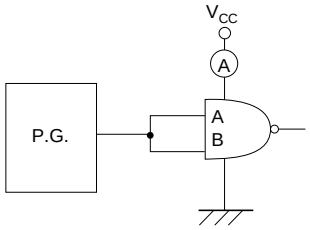
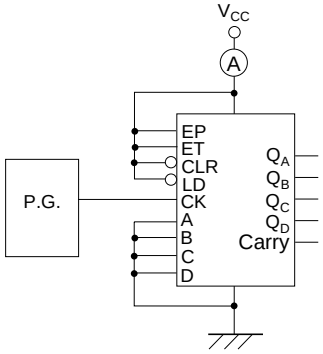
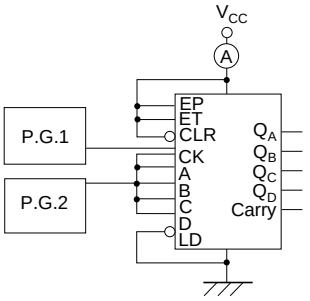


Figure 14 Measurement Circuits for Dynamic Power Supply Current (cont)

Table 3 Power Dissipation Capacitance by Input Conditions

Product part no.	Input conditions	Power dissipation capacitance (pF)
HD74HC00	Single input	27
		
	Double input	27
		
HD74HC161	Counting operation	57
		
	Preset operation	113
		

6. Decoupling

CMOS logic ICs have current spikes when switching. These spikes are produced by the repeated charging and discharging of the output capacitance when charging the output level from low to high or high to low.

Because of the current spikes the potentials of V_{CC} and GND change, and large current spikes flow when switching. Therefore ringing is produced at the output. (See Figure 15 a.)

To prevent this, decoupling capacitors must be provided externally between V_{CC} and GND.

This is proven to be useful in instantly absorbing the current and ringing at the output as shown in Figure 15 b.

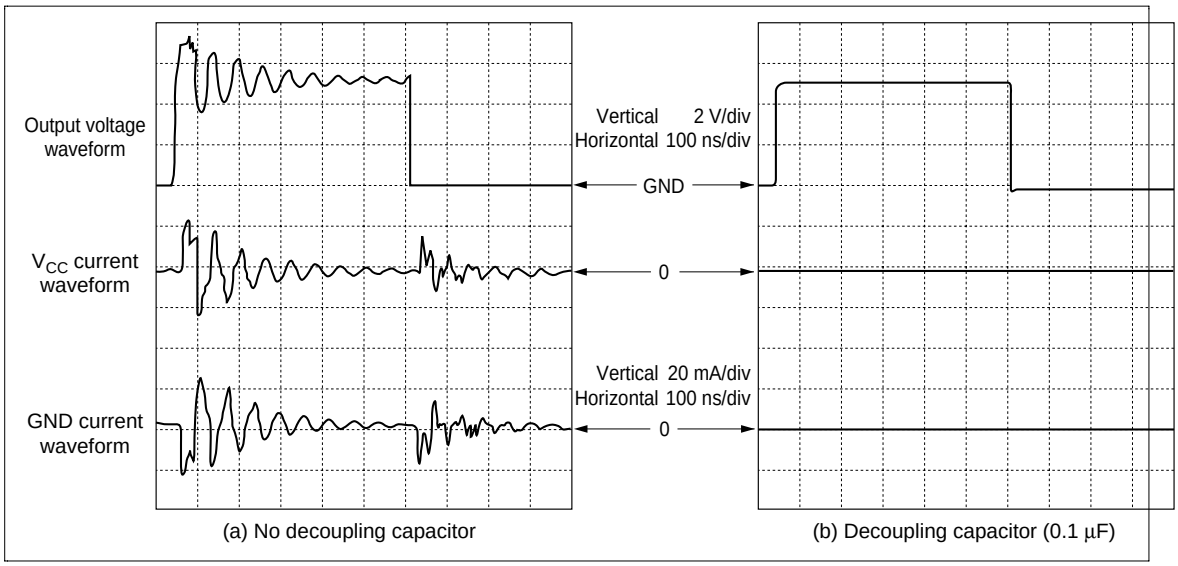


Figure 15 HD74HC00 Spike Current Waveform

7. Precautions on Board Design

High-speed CMOS logic has different electrical characteristics, such as switching speed and output current drivability, from the conventional standard logics (Al-gate CMOS, LS-TTL). The system design requires an application technique for high-speed CMOS logic.

Here an interfacing technique between high-speed CMOS logic and LS-TTL will be explained.

7.1 Transmission line reflection

(1) Analysis of transmission signals by the Bergeron diagram The Bergeron diagram is commonly used for the analysis of transmission signals in high-speed digital systems.

Figure 17 is the analysis result of an actual transmission model which is shown in Figure 16.

As for the analysis conditions, $Z_0 = 125\ \Omega$ considering the standard system board, and the wiring length (l) is 1.5 m.

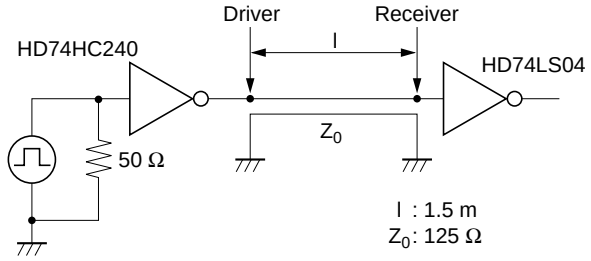
The output impedance of the HD74HC04, which operates as a driver becomes the I_{OH} - V_{OH} characteristic curve when the output is high, and the input impedance of the HD74LS04 which operates as a receiver becomes the I_{IH} - V_{IH} characteristic curve.

On the other hand, when the output level of the HD74HC04 is low, the output impedance becomes the I_{OL} - V_{OL} characteristic curve and the input impedance becomes the I_F - V_F characteristic curve.

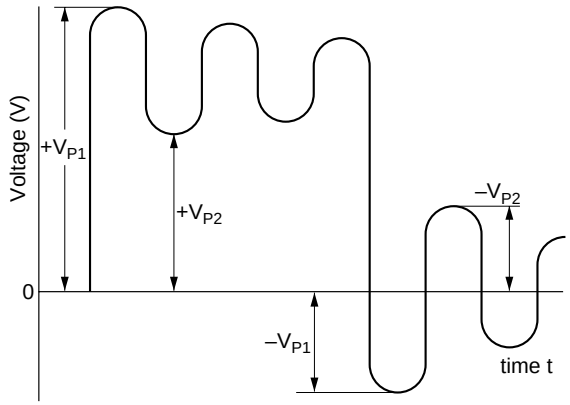
The drawing of load line Z_0 as these input/output impedance curves enables the reflection of the transmission signal to be analyzed.

The intersection coordinates in Figure 17 shows the voltage and current values at the drive end of 2T (T being the propagation delay from the driver end to the receiver end) intervals when the coordinates are even numbers (2T, 4T) or zero, or the voltage and current values at the receiver end when the coordinates are odd numbers (T, 3T, 5T).

Figure 18 shows the analysis result of the voltage waveform at the receiver end.



(a) Digiral signal transmission model circuit



(b) Receiver waveform model

Note: The model circuit above (Figure 16a) is used for analysis when the high-speed CMOS logic HD74HC240 is connected as a driver, and the LS-TTL HD74LS04 as a receiver
The waveform model for overshoot and undershoot at the receiver end is shown in Figure 16b.

Figure 16 Digital Signal Transmission

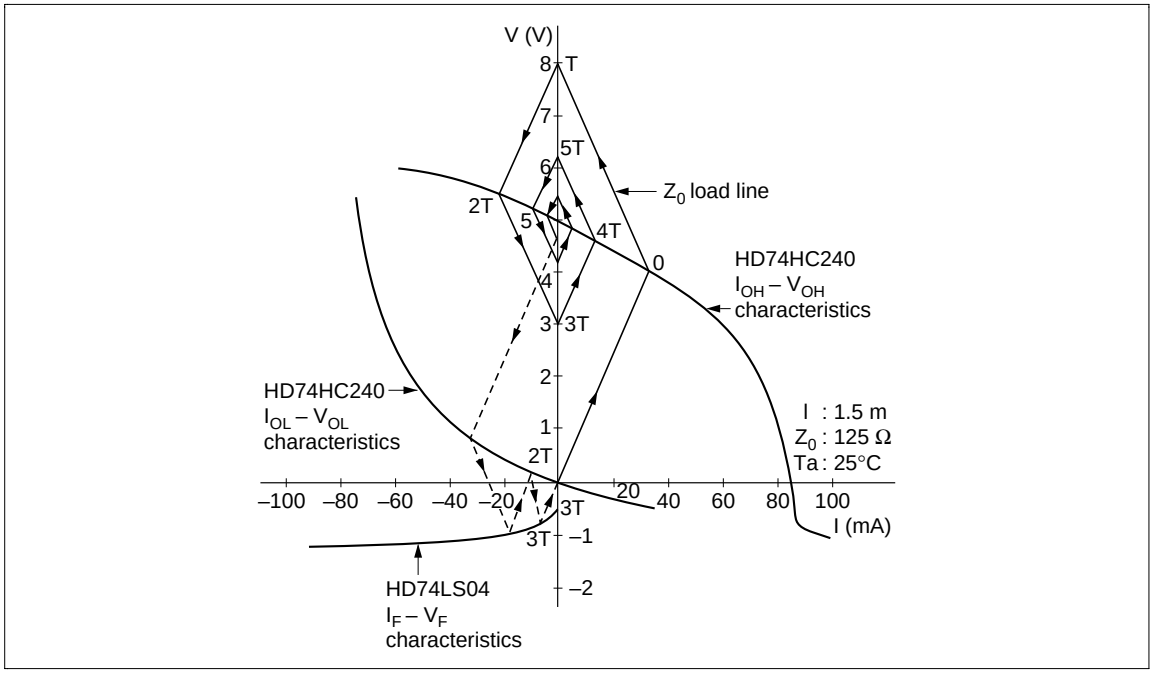


Figure 17 Bergeron Diagram Analysis of the Transmission Model

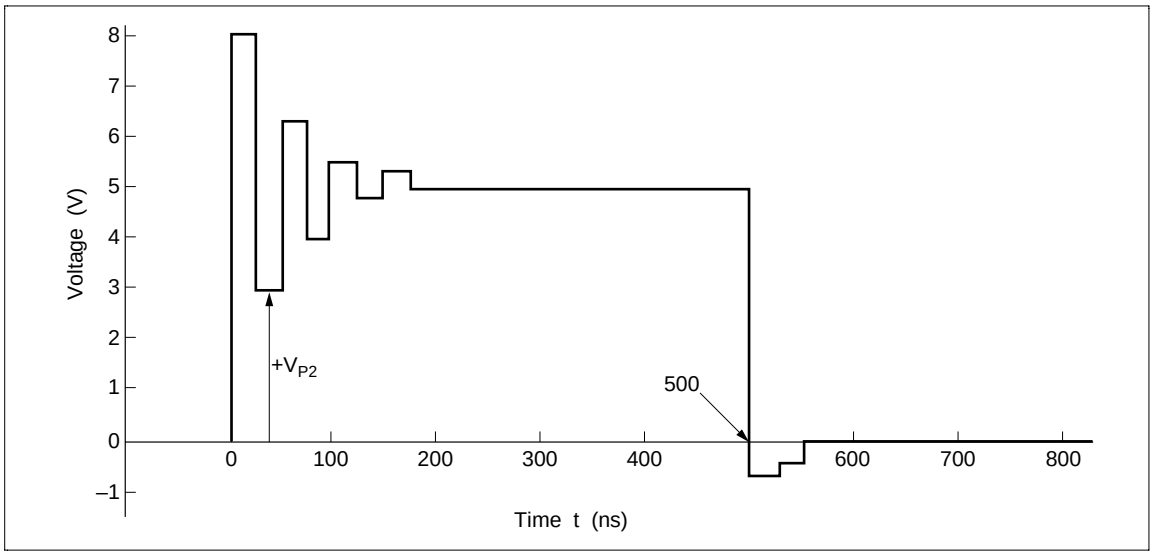
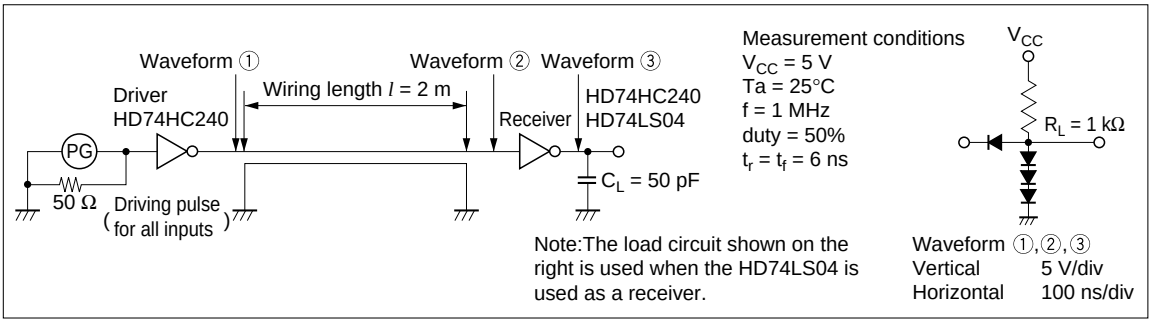


Figure 18 Analysis Results of the Waveform at the Receiver End

(2) An example for measuring the reflection on the transmission line Figure 19 shows the measured results of the reflection of the transmission line using three types of transmission line media such as 1) coaxial cable (Z_0 = 50 Ω), 2) twisted pair cable (Z_0 = 120 Ω), and 3) single lead wire (Z_0 = 150 to 200 Ω).

Figure 19 shows that the drivers and receivers operate normally with a wiring length of up to 2 m.

However, careful precautions should be taken when considering impedance in practical system designing.



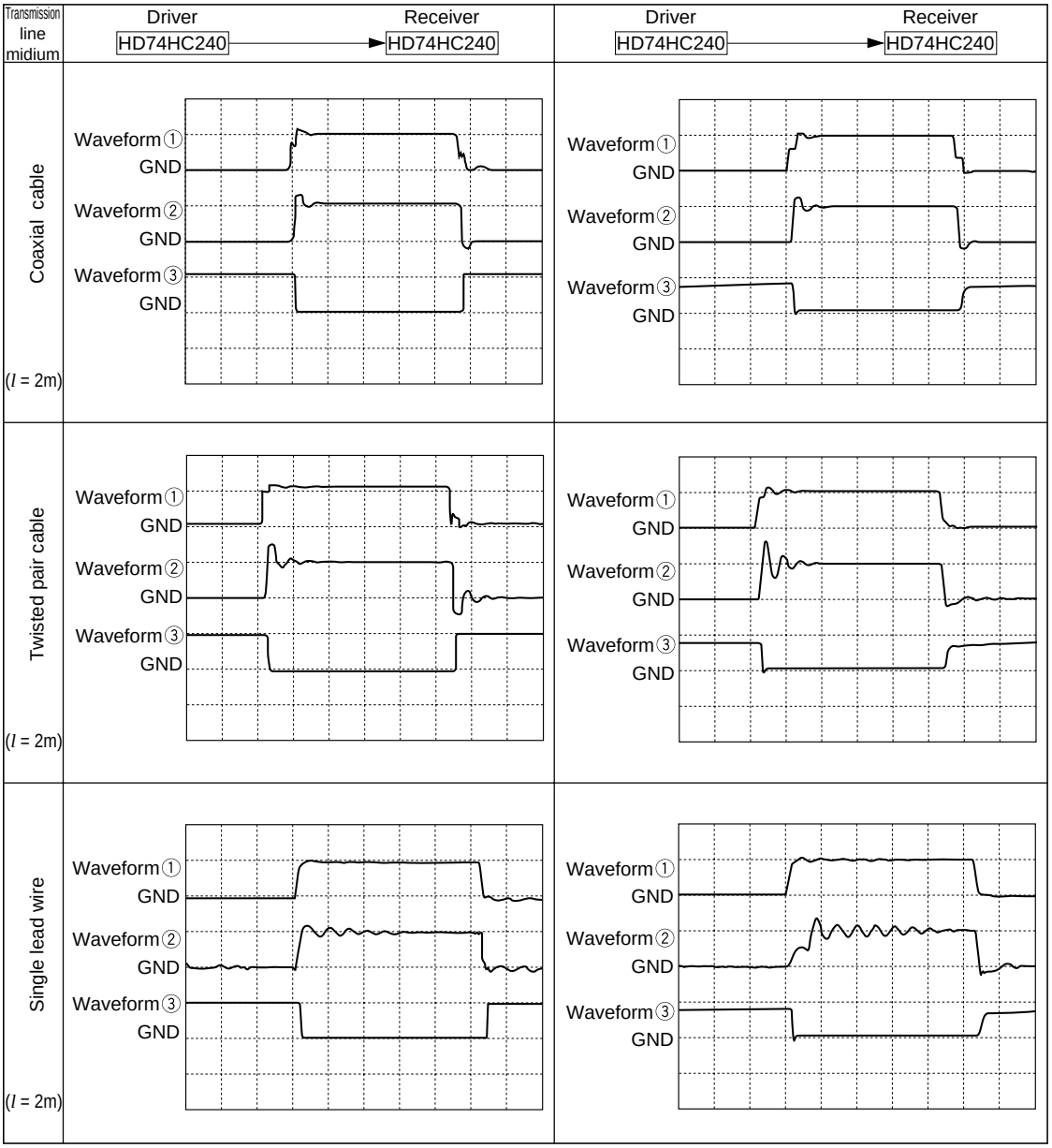


Figure 19 Reflection Ringing Waveforms (Driver: HD74HC240)

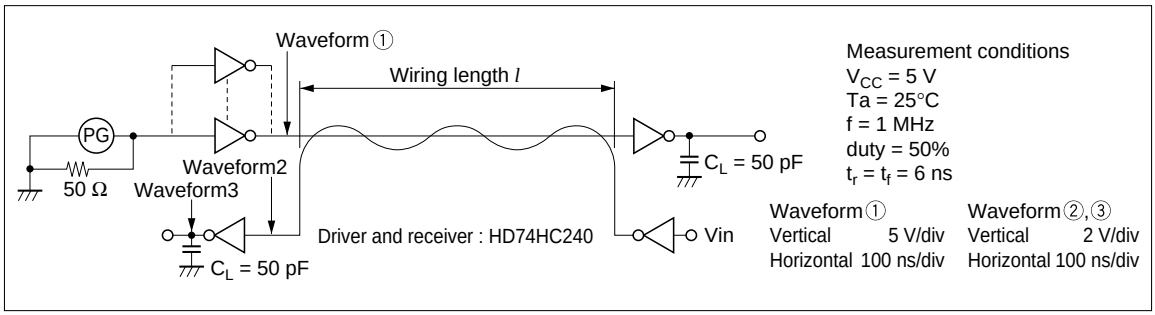
7.2 Crosstalk

Crosstalk is the capacitative coupling of signals from one line to another.

Figure 20 shows an example of crosstalk noise levels using a twisted pair cable.

Figure 20 also shows that the wiring length beyond 1 m causes malfunction.

Careful precautions should be taken especially when the spacing between circuits is narrow.



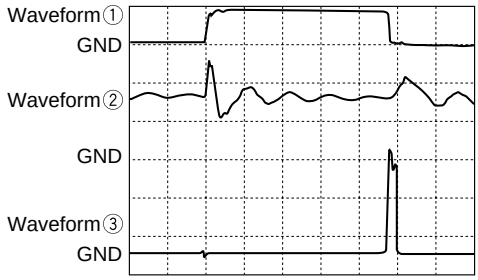
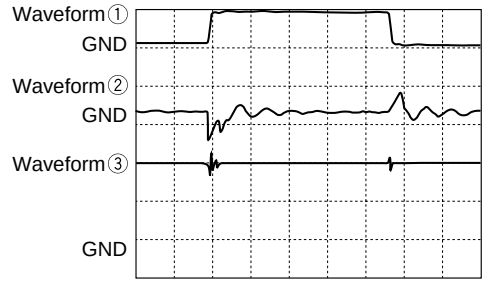
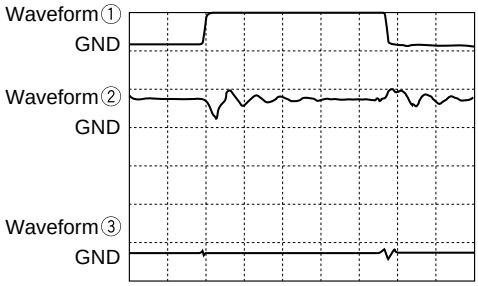
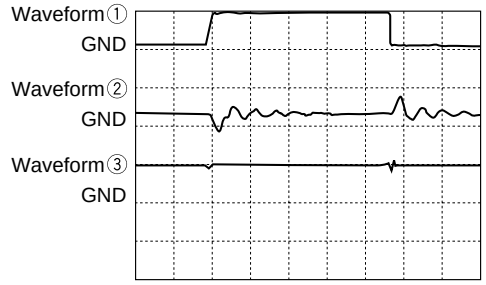
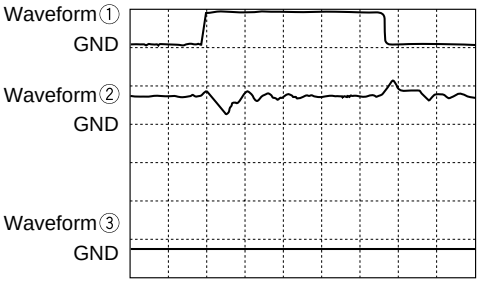
Wiring lenght	Vin = Low	Vin = High
l = 2m		
l = 1m		
l = 0.5m		

Figure 20 Crosstalk Noise Waveform (Driver: HD74HC240)

8. Multivibrator

The output pulse width (t_{wq}) of a multivibrator is determined by the external capacitance (c_{ext}) and external resistor (R_{ext}), and calculated by the equation $t_{wq} = K \cdot R_{ext} \cdot C_{ext}$.

The value of constant K determines the part number according to the JEDEC committee as listed in Table 4.

Hitachi has 4 types of high-speed CMOS logic, HD74HC123A, 221, 423A, 4538.

Constant K changes from the values of Table 4 when C_{ext} is less than 0.01 µF.

Figure 21 and 22 graph the output pulse width vs external capacitance, constant K vs power supply voltage characteristics of the HD74HC123A.

Table 4 JEDEC SP of Multivibrators

Product part no.	Output pulse width
74HC123	$t_{WQ} = 0.45 \cdot (Rext) \cdot (Cext)$
123A*	$t_{WQ} = 1.0 \cdot (Rext) \cdot (Cext)$
74HC221*	$t_{WQ} = 0.7 \cdot (Rext) \cdot (Cext)$
221A	$t_{WQ} = 1.0 \cdot (Rext) \cdot (Cext)$
74HC423	$t_{WQ} = 0.45 \cdot (Rext) \cdot (Cext)$
423A*	$t_{WQ} = 1.0 \cdot (Rext) \cdot (Cext)$
74HC4538*	$t_{WQ} = 0.7 \cdot (Rext) \cdot (Cext)$

Note: *Presently under mass production at Hitachi.

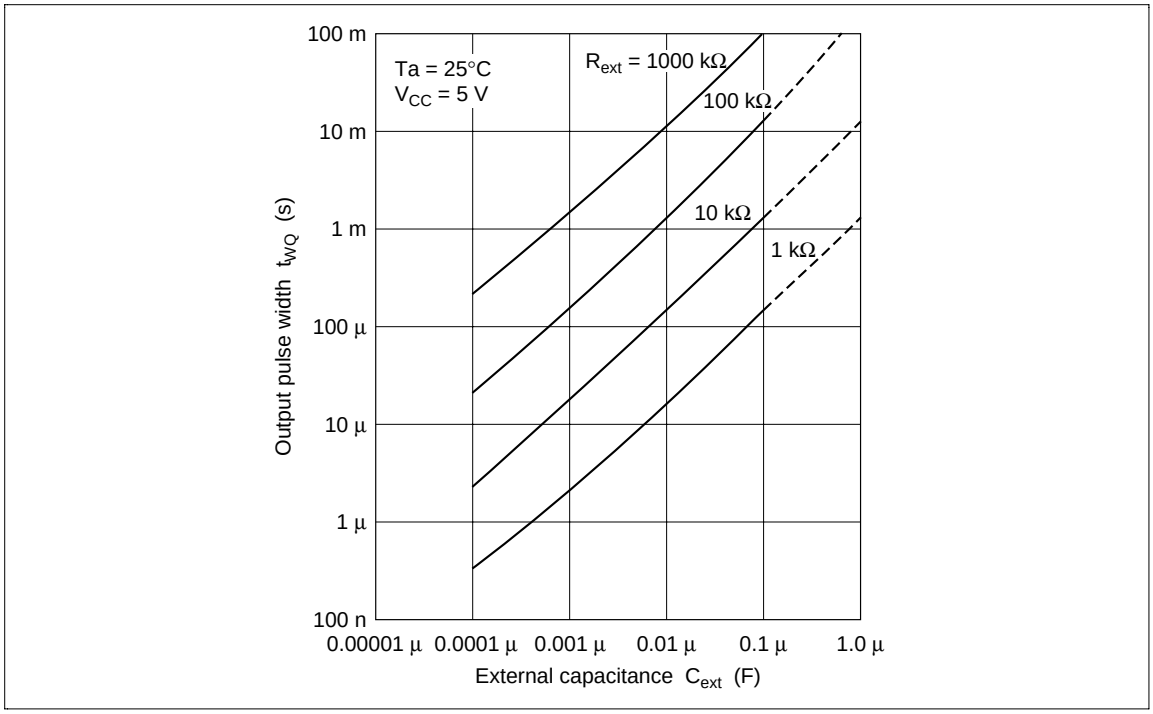
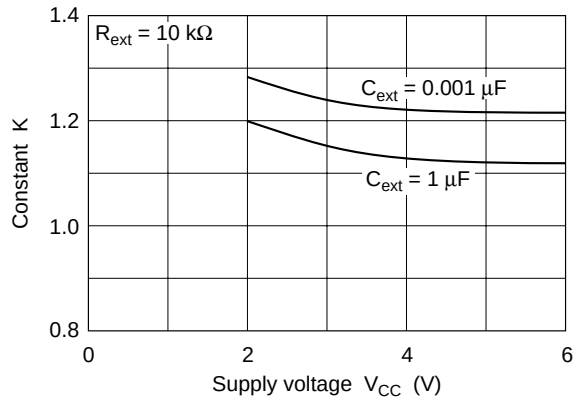


Figure 21 Output Pulse Width vs External Capacitance and Resistance



Note: In order to prevent any malfunctions due to noise, connect a high-frequency performance capacitor between V_{CC} and GND, and keep the wiring between the external components and Cext, Rext/Cext pins as short as possible.

Figure 22 Constant K vs Supply Voltage

9. Interfacing

Hitachi's high-speed CMOS logic has two types of input voltage levels, 74HC and 74HCT.

The 74HC has a CMOS-type input level and the 74HCT has a TTL-type input level.

Interfacing from high-speed CMOS logic to LS-TTL

Since the output level of high-speed CMOS logic is of CMOS, the use of an interfacing circuit is not necessary.

This is the same case for a microcomputer and memory IC with TTL input levels.

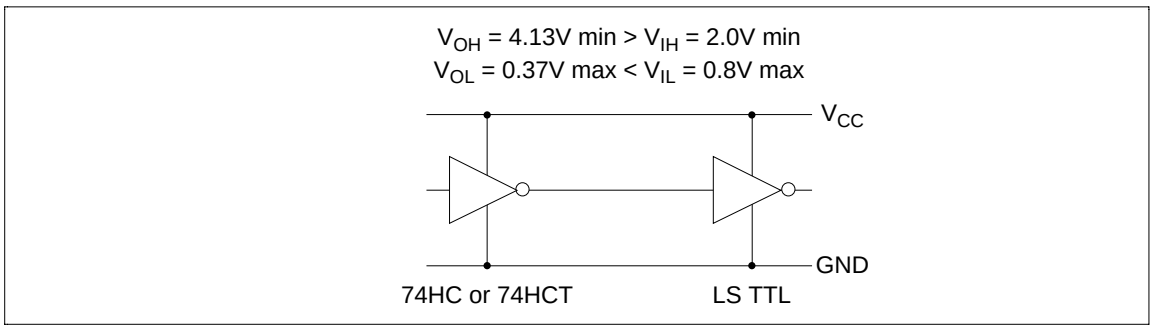


Figure 23 Interfacing HS-CMOS to LS-TTL

Interfacing from LS-TTL to high-speed CMOS logic (74HCT type)

An interfacing circuit is not necessary.

This is the same case for a microcomputer and memory IC with TTL output levels.

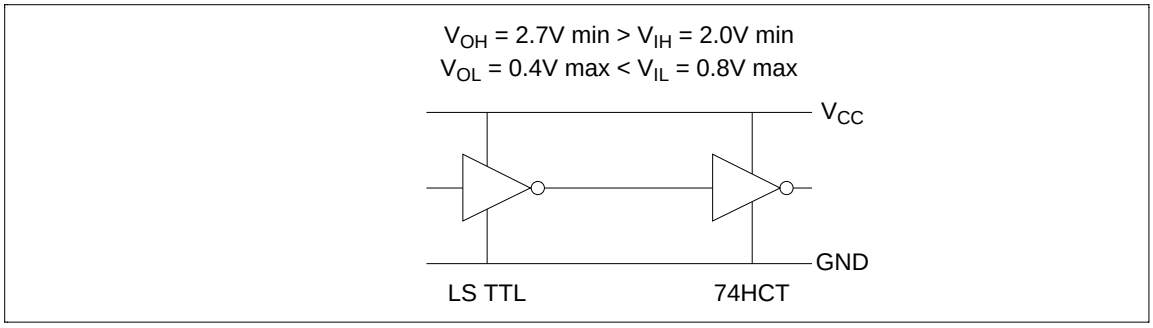


Figure 24 Interfacing LS-TTL to 74HCT

Interfacing from LS-TTL to high-speed CMOS logic (74HC type)

A pull-up resistor should be added as shown in Figure 25.

The output voltage of LS-TTL (V_{OH}) is 2.7 V (min), where as the input voltage of 74HC (V_{IH}) is 3.15 V (min.).

This implies that LS-TTL cannot drive 74HC types directly.

This is the same case for a microcomputer and memory ICs with TTL output levels.

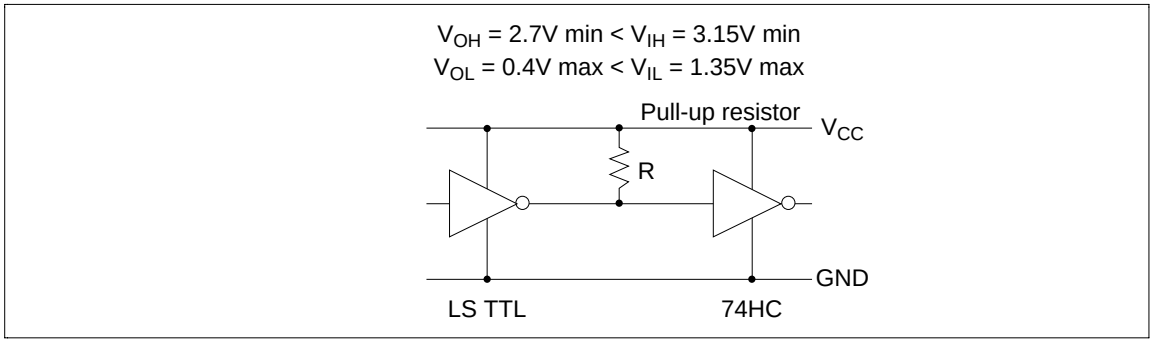


Figure 25 Interfacing LS-TTL to 74HC

Interfacing from LS-TTL with 3-state output to high-speed CMOS logic.

A pull-up or pull-down resistor should be added as shown in Figure 26.

When the output of a LS-TTL is in the high-impedance state, the input of the high-speed CMOS becomes unstable.

This is the same case for all devices with a tri-state output structure.

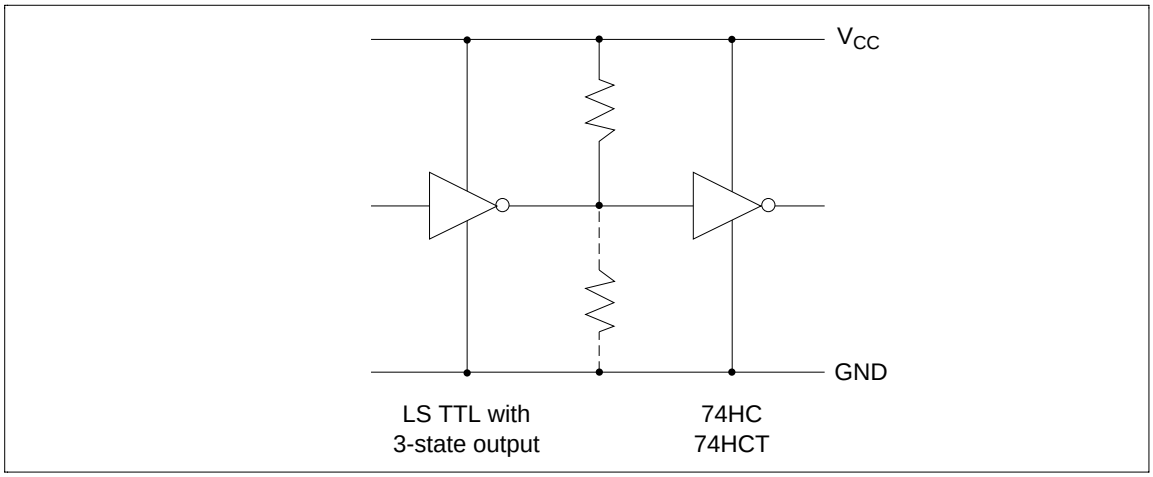


Figure 26 Interfacing LS-TTL with 3-state Output to 74HC or 74HCT

10. Surface Mount Package

10.1 Mounting small outline packages (SOP, TSSOP)

The explanation on the mounting of SOPs describes the characteristics and reliabilities of the small IC package.

(1) Dip Soldering

Initially, the package is temporarily fixed on to the board by an adhesive.

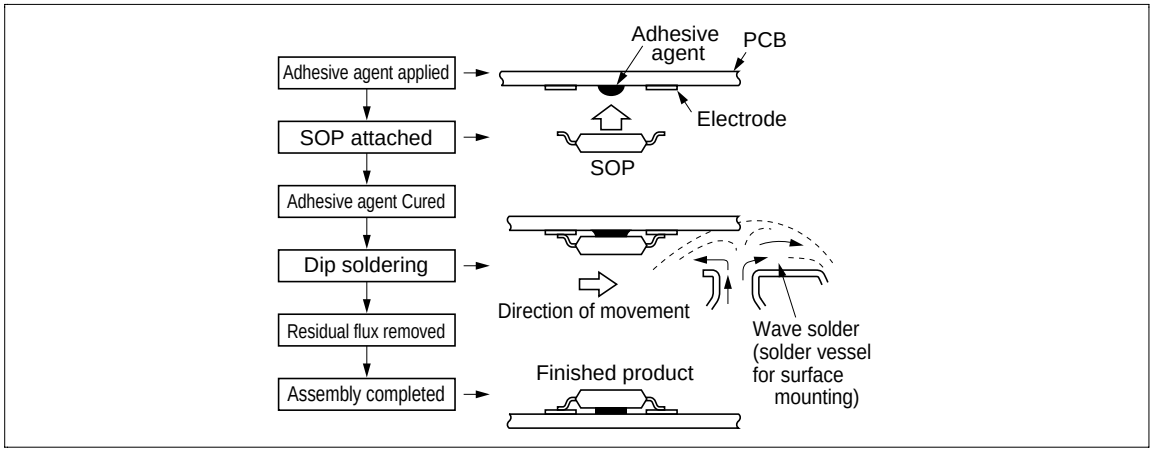


Figure 27 Process Flow for Dip Soldering SOP

With the component side of the board downward, the package is then passed through molten solder. Figure 27 depicts the process flow for dip soldering SOP. As compared with reflow methods, this method exerts an extremely high thermal stress on the semiconductor chips. The adverse effects from this thermal should be avoided by providing a preheating zone to lessen the thermal shock and by minimizing the soldering time. Figure 28 shows a typical temperature profile for dip soldering.

The dip soldering temperature is 260˚C maximum at a period of 10 seconds maximum (2 to 4 seconds is recommended).

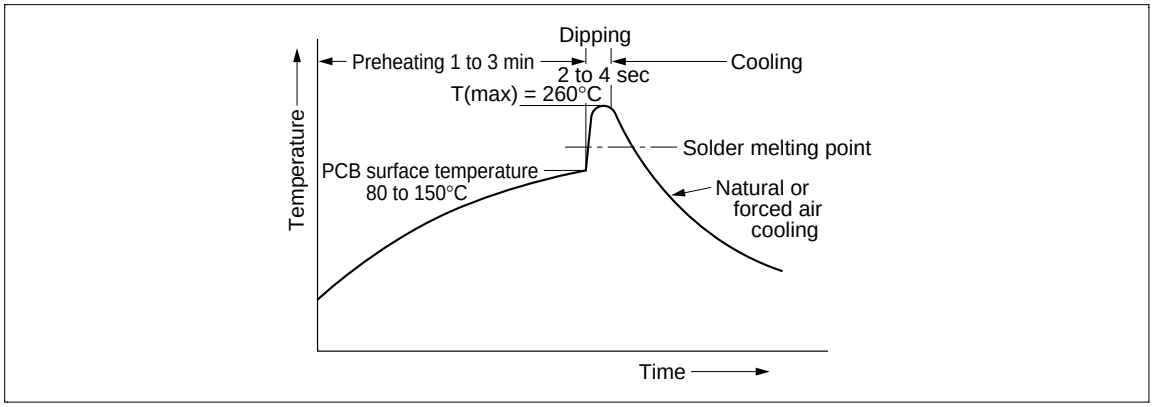


Figure 28 Temperature Profile of Dip Soldering

(2) Reflow Soldering

Reflow soldering is the basic method of mounting the SOP on to a board.

The solder composition to be used is Sn63/Pb37 or Sn62/Pb36/Ag2 with a melting point of 183˚C to 193˚C.

A recommended pasty flux is solder cream SP210-2 by Tamura Kaken. A pasty flux and organic solvent are also used during the process.

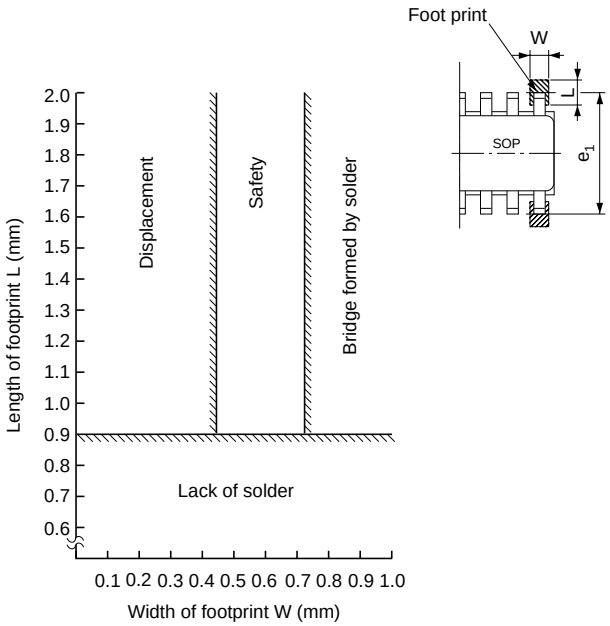
Be careful to reflow solder at a low temperature for short periods of time. The recommended conditions are shown below. The allowable board temperature is 230˚C maximum and the maximum heating time is 15 sec.

(3) Footprint dimension vs solderability

The failure rate of soldering is affected by footprint dimensions. Figure 29 shows the soldering failure with the footprint dimension.

The recommended dimensions are within the safety zone of this figure.

When reflow sordering SOPs, the recommended thickness of a footprint is 0.2 mm min.

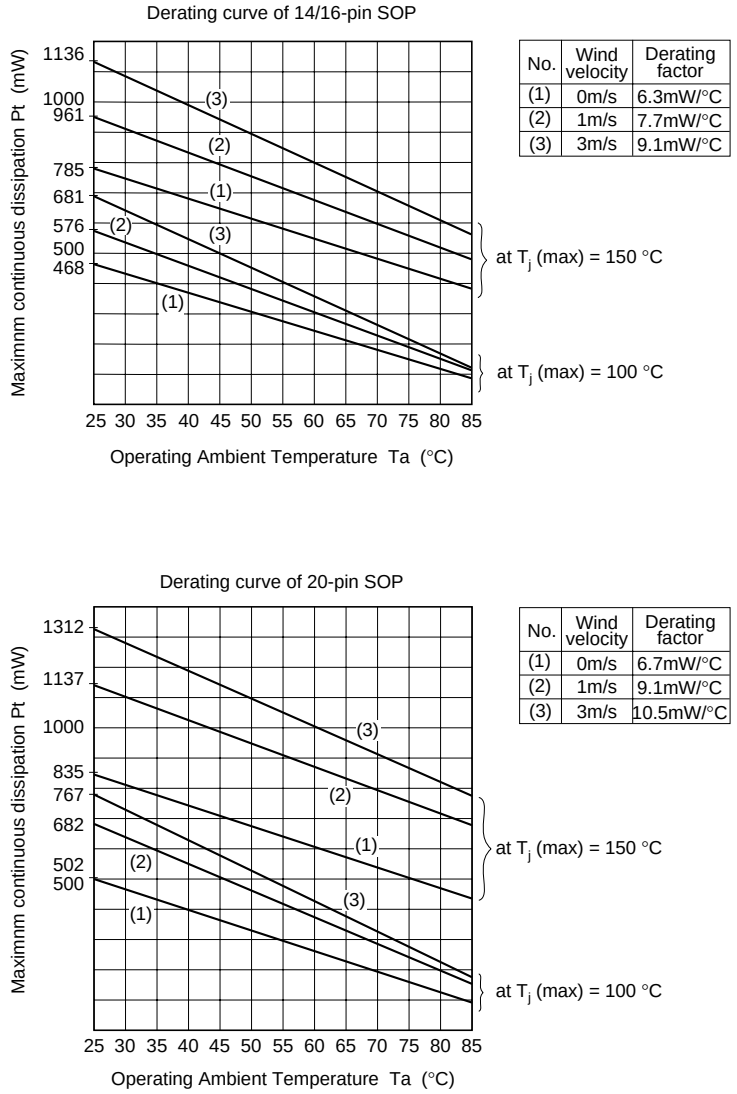


Notes:
1. Pin pitch = 1.27 mm
2. Recommended spacings between footprint centers.
   e_1 = 7.62 mm (SOP-14, 16)
   e_1 = 9.53 mm (SOP-20)
3. Both W and L are footprint dimensions based on the lead direction of the SOP.

Figure 29 Recommended Dimension of Footprint

(4) Thermal Resistance of SOP

Figure 30 shows the derating curves for SOPs of high-speed CMOS logic, and Table 6 lists the thermal resistance ($\theta_{j\text{-}a}$) for SOPs.



Note: When Ta is below 25˚C, P_T becomes the same value as at Ta = 25˚C being independent of Ta.

The data above was measured by using the ΔV_{BE} method on a glass-epoxy board (40×40×1.0 mm) with wiring density of 10%.

Careful considerations are required for input and load conditions, Ta, cooling, etc., during actual use.

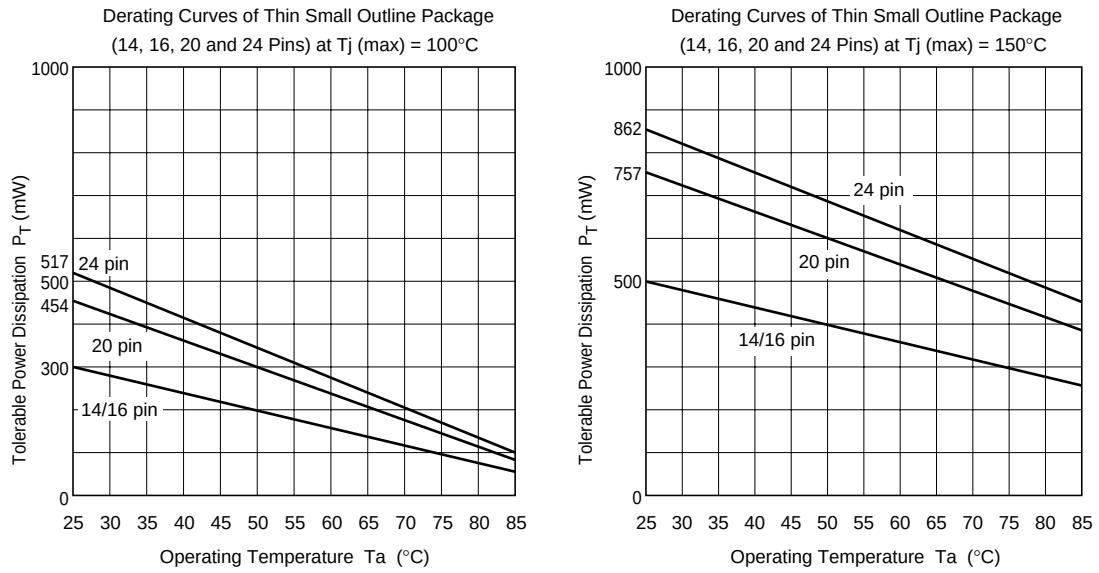
Figure 30 Derating Curves of SOP

Table 6 Thermal Resistance of SOPs

				Maximum continuous dissipation Ta = 25˚C	
Number of pins	**Wind velocity**	**Derating factor**	**Thermal resistance**	**T_j(max) = 150˚C**	**T_j(max) = 100˚C**
14	0 m/s	6.3 mW/˚C	160 ˚C/W	785 mW	468 mW
16	1 m/s	7.7 mW/˚C	130 ˚C/W	961 mW	576 mW
	3 m/s	9.1 mW/˚C	110 ˚C/W	1136 mW	681 mW
20	0 m/s	6.7 mW/˚C	150 ˚C/W	835 mW	502 mW
	1 m/s	9.1 mW/˚C	110 ˚C/W	1137 mW	682 mW
	3 m/s	10.5 mW/˚C	95 ˚C/W	1312 mW	787 mW

(5) Thermal Resistance of TSSOP

Figure 31 shows the derating curve of TSSOP with HD74BC/AC/HC devices, table 7 shows the thermal resistance (θ_{j-a}) and figure 32 shows the mounting method.



Note: Fore the ambient temperature less than 25˚C, the power dissipation at 25˚C is applied. The data above are measured by ΔV_{BE} method mounting on glass epoxy board ($40 \times 40 \times 1.6$ mm) with 10% of wiring density. In the actual application, using conditions, ambient temperature and forced air-cooling conditions should be sufficiently examined.

Figure 31 Derating Curve of TSSOP

Table 7 Thermal Resistance of TSSOP Package

Number of pins	Wind velocity	Derating factor	Thermal resistance	Tolerable power dissipation at T_j(max) = 150˚C	Tolerable power dissipation at T_j(max) = 100˚C
14	0 m/s	4.0 mW/˚C	250˚C/W	500 mW	300 mW
16					
20	0 m/s	6.1 mW/˚C	165˚C/W	757 mW	454 mW
24	0 m/s	6.9 mW/˚C	145˚C/W	862 mW	517 mW

(6) TSSOP Solder Mounting

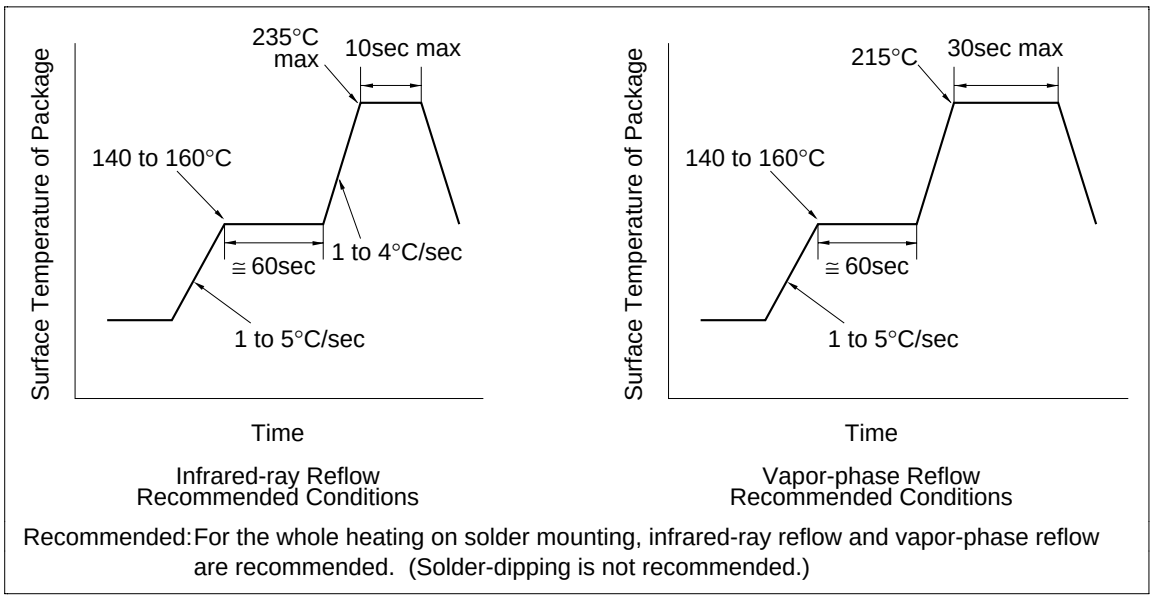
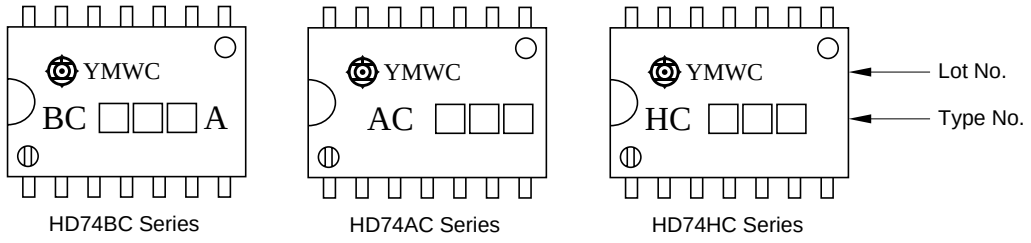


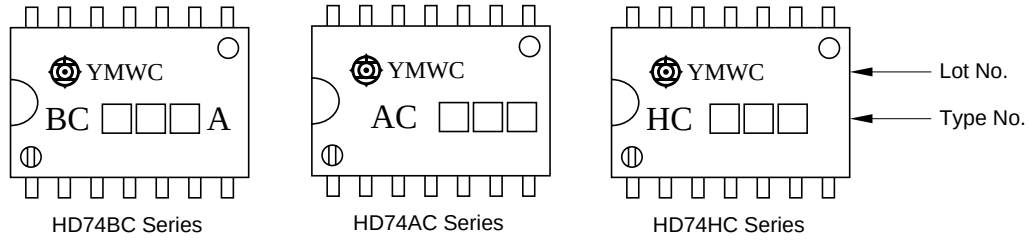
Figure 32 Mounting Method of TSSOP

(7) Marking on Package

(a) Small outline Package (EIAJ) 14, 16, 20 pins



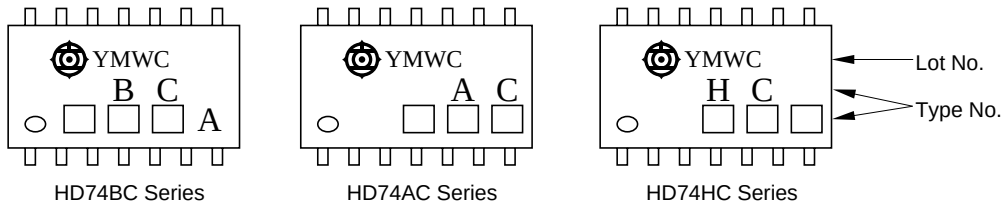
(b) Small outline Package (JEDEC) 14, 16, 20 pins



Note: Meaning of marking on package example device name:
HD74BC245AT
Y: Year code (the last digit of year)
M: Month code
W: Week code
C: Control code
Type No.: delete HD74 and package code (T) from device name

(c) Thin Shrink Small outline Package 14, 16, 20 pins

• 14, 16, 20 pins



Note: Meaning of marking on package example device name:
HD74BC245AT
Y: Year code (the last digit of year)
M: Month code
W: Week code
C: Control code
Type No.: delete HD74 and package code (T) from device name